Design Considerations for VRM Transient Response Based on the Output Impedance

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***Abstract*—This paper discusses the transient response of voltage regulator modules (VRMs) based on the small-signal models. The concept of constant resistive output impedance design for the VRM is proposed, and its limitations in applications are analyzed. The impacts of the output filter and the feedback control bandwidth show that there is an optimal design that allows the VRM to achieve fast transient response, small size and good efficiency. Simulations and experimental results prove the theoretical analysis.**

***Index Terms*—Output impedance, transient analysis, voltage regulator.**

I. Introduction

As THE clock speed of microprocessors is developed to be faster than 1 GHz, a lower operation voltage is better for data processing efficiency. Currently, the supply voltage level is about 1.5 V, and it will decrease further in the future. For such a low value, the allowable difference between the maximum and minimum voltages is very small. For example, a Pentium IV allows only a tolerance of about 130 mV [1]. Conversely, the microprocessor is more power-hungry because of the high-density semiconductor integration. The supply current is already more than 50 A for a Pentium IV, and it will be even larger for the next generation of microprocessors. The large supply current not only poses a stringent challenge on efficiency, but also heavily burdens the transient response. One reason for these difficulties is the large current step; another is the very fast current slew rate (50 A/μs now, and much higher in the future). Simply put, as a special power supply for the microprocessor, the voltage regulator module (VRM) must maintain a low output voltage within a tight tolerance range during operation with large current step change and high slew rate.

To meet such transient requirements, the VRM must use many output capacitors, which increase its size and cost. At the beginning when the VRM emerged, the feedback control kept the output voltage at the same level for the entire load range. As a result, the output voltage spike during the transient must be smaller than half of the voltage tolerance window. If the output voltage level is a little higher than the minimum value at full load and a little lower than the maximum value at light load, the whole voltage tolerance range can be used for the voltage jump or drop during the transient. This is the concept of adaptive voltage position (AVP) design [2], [3]. Fig. 1 shows the transient comparison between non-AVP and AVP designs. It is very clear that the AVP design allows the use of fewer output capacitors, and hence reduces the VRM cost. Another benefit of the AVP design is that the VRM output power at full load is reduced, which greatly facilitates the thermal design.

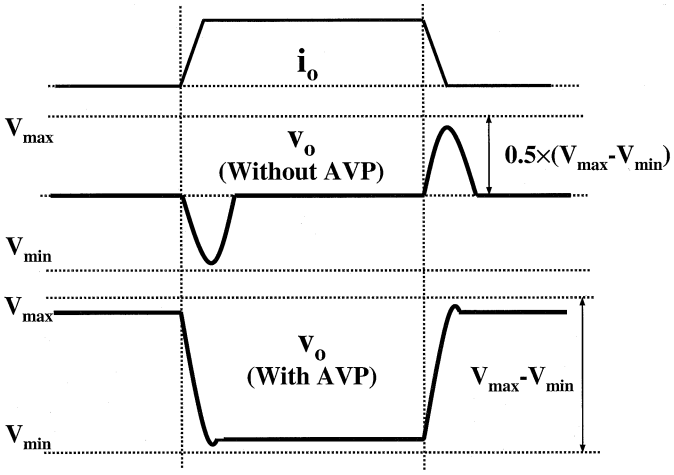
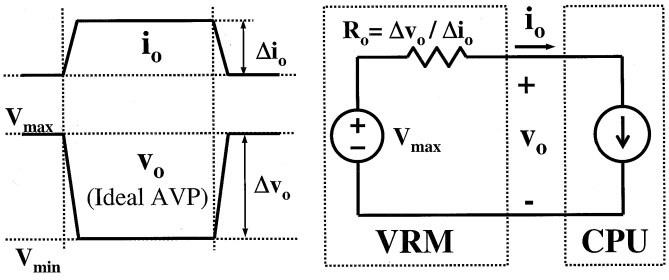


Fig. 1. Transient without and with AVP designs.



(a) (b)

Fig. 2. (a) Ideal AVP design and (b) the equivalent circuit of the VRM.

The AVP is related to the steady-state operation of the VRM. If the transients between the two steady-state stages have no spikes and no oscillations, as is the situation shown in Fig. 2(a), the AVP design is optimal. The transient can take advantage of the entire voltage tolerance window. The comparison between the current and the related output voltage waveforms reveals that the VRM equals an ideal voltage source in series with a resistor R_o

$$R_o = \Delta v_o / \Delta i_o. \tag{1}$$

Fig. 2(b) shows the equivalent circuit of the VRM.

Manuscript received October 10, 2003; revised June 3, 2003. Recommended by Associate Editor G. Walker. This paper was presented in part at APEC'02, Dallas, TX, March 10–14, 2002. This work was supported by Intel, Texas Instruments, National Semiconductors, Intersil, TDK, Hitachi, Hipro, Power-One, Delta Electronics, ERC shared facilities, and the National Science Foundation under Award EEC-9731677.

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Digital Object Identifier 10.1109/TPEL.2003.818824

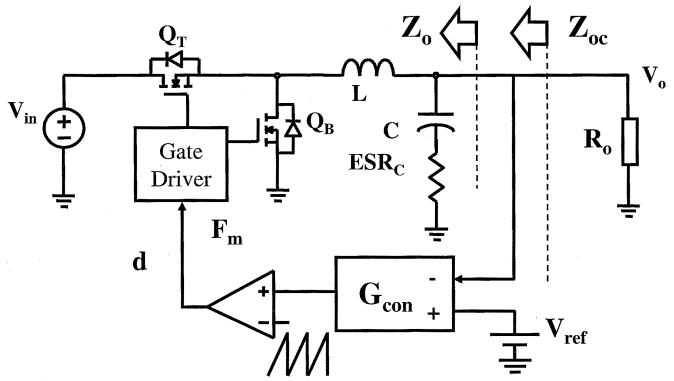


Fig. 3. Output impedance analysis using a buck converter.

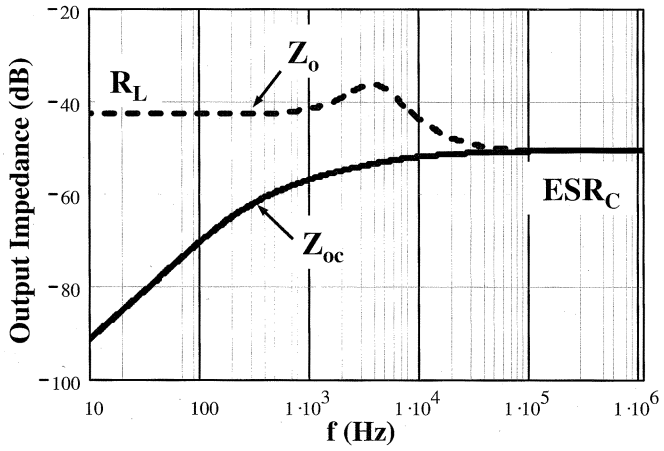


Fig. 4. Output impedance with open and closed loops.

Now it is very clear that the constant resistive output impedance design for the VRM is an optimal design for the transient. Actually, improving the dynamic regulation of a converter based on the output impedance consideration is an old concept [4]–[7]. However, not every converter can achieve constant resistive output impedance. Additionally, it is not clear how to design the feedback control loop. This paper clarifies these issues. Section II proposes a simple method for realizing the constant output impedance. Both the voltage-mode and current-mode controls are discussed. Section III investigates the limitation of the constant output impedance design based on the small-signal analysis method. Finally, Section IV shows an example of optimal design.

II. Constant Output Impedance Design

Currently, the multiphase synchronous buck converter is widely used for VRMs. The small-signal model can be simplified as a single-phase buck converter in continuous-current mode [8]. As a result, a simple buck converter, shown in Fig. 3, is used to analyze the output impedance with an open loop and with a closed loop. The equivalent series inductor (ESL) of the output capacitor is ignored here since the high-frequency ceramic capacitors in parallel greatly reduce its effect.

Based on the small-signal analysis method [9]–[11], it is easy to derive the open-loop output impedance Z_o and the closed-loop output impedance Z_{oc}

$$Z_o(s) = R_L \frac{(1+s/\omega_C)\cdot(1+s/\omega_L)}{1+s/(Q\cdot\omega_o)+s^2/\omega_o^2}, \tag{2}$$

$$Z_{oc}(s) = \frac{Z_o(s)}{1+T(s)}, \quad \text{and} \tag{3}$$

$$\omega_c = \frac{1}{C\cdot \mathrm{ESR}_C}, \quad \omega_L = \frac{L}{R_L},$$

$$\omega_o \approx \frac{1}{\sqrt{C\cdot L}}, \quad Q \approx \frac{\sqrt{L/C}}{R_L + \mathrm{ESR}_C}. \tag{4}$$

Here, R_L includes the dc resistance of the inductor L, the conduction resistance R_{ds-on} of the MOSFETs Q_T and Q_B, and the parasitic resistance of the traces. The ESR_C is the equivalent series resistance (ESR) of the output capacitor C. The ω_o is the power stage double pole, and the T(s) is the closed-loop gain.

Fig. 4 shows the open-loop and closed-loop output impedance. At high frequencies, ESR_C determines the output impedance. No matter how the closed-loop gain T(s) is designed, Z_{oc} has the same value as Z_o beyond the bandwidth. Feedback control can attenuate the output impedance only in the low-frequency range. As a result, the ESR_C is the only value that is able to achieve constant output impedance.

The design method is simple. First, the closed-loop output impedance Z_{oc} is derived, which is a function of the compensator transfer function $G_{con}(s)$. Then, $G_{con}(s)$ can be derived by solving the equation $Z_{oc} = \mathrm{ESR}_C$. Finally, the compensator can be designed to be as close as possible to the ideal transfer function $G_{con}(s)$. Thus, some simple compensator designs can achieve approximately constant resistive output impedance. Both the voltage-mode and current-mode controls are discussed in the following sections.

A. Voltage-Mode Control

For voltage-mode control, the closed-loop output impedance is

$$Z_{oc}(s) = \frac{Z_o(s)}{1+T(s)} = \frac{Z_o(s)}{1+F_m\cdot G_{vd}(s)\cdot G_{con}(s)} \tag{5}$$

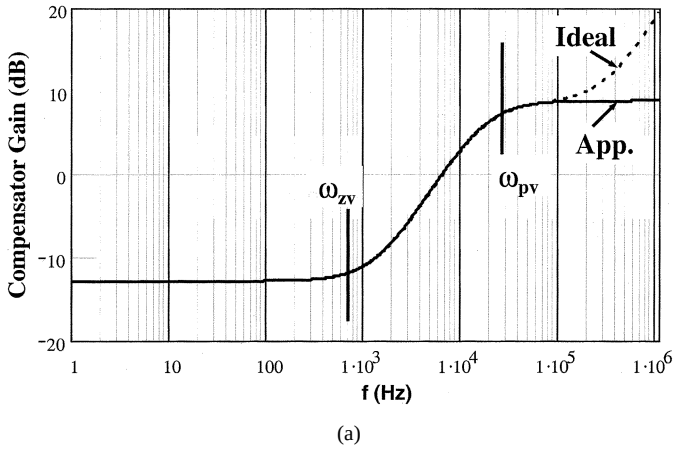
where F_m is the comparator gain, and $G_{vd}(s)$ is the transfer function of the output voltage Vo to the duty cycle d. Fig. 5 shows the ideal compensator transfer function necessary to achieve $Z_{oc} = \mathrm{ESR}_C$. Since the small-signal model is no longer effective beyond the half switching frequency, the real compensator design only needs to be accurate for the low-frequency range. A single pole and zero compensator can satisfy this requirement, such that

$$G_{con}(s) = K_V \frac{1+s/\omega_{zv}}{1+s/\omega_{pv}}. \tag{6}$$

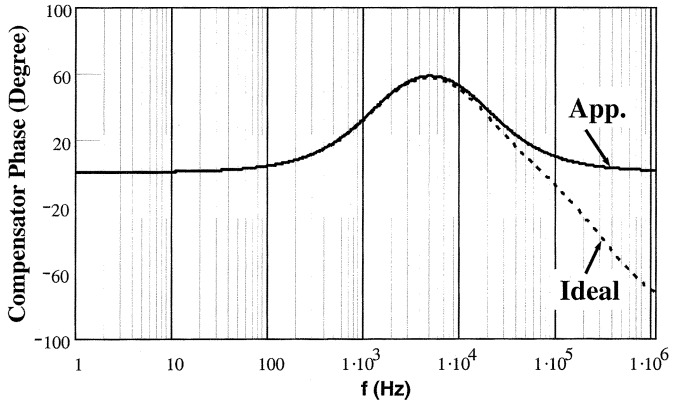
Further mathematical analysis shows the detailed values of the dc gain, pole and zero, as

$$K_v = \frac{R_L - \mathrm{ESR}_C}{\mathrm{ESR}_C\cdot V_{in}\cdot F_m} \tag{7}$$

$$\omega_{pv} = \omega_c \tag{8}$$



(a)



(b)

Fig. 5. Compensator design for voltage-mode control.

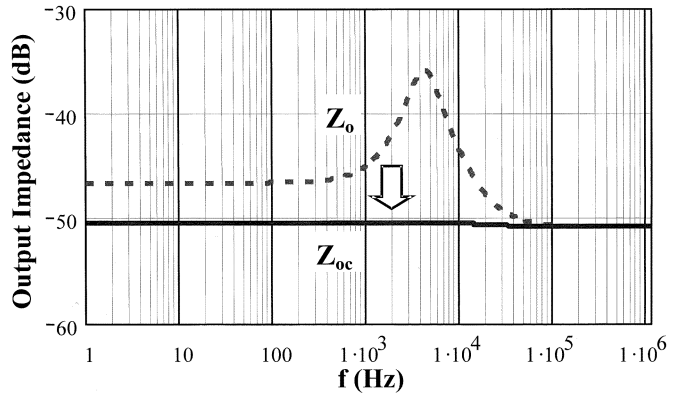


Fig. 6. Output impedance with voltage-mode control.

$$\omega_{zv} = \frac{b - \sqrt{b^2 - 4 \cdot a \cdot c}}{2 \cdot a} \tag{9}$$

$$a = \frac{R_L}{\omega_L \cdot \omega_c} - \frac{\mathrm{ESR}_C}{\omega_o^2},$$

$$b = R_L \cdot \left(\frac{1}{\omega_L} + \frac{1}{\omega_c}\right) - \frac{\mathrm{ESR}_C}{\omega_o \cdot Q},$$

$$c = R_L - \mathrm{ESR}_C. \tag{10}$$

Fig. 6 shows the closed-loop output impedance using this compensator design. It is almost constant. Simulation results given in Fig. 7 show the nearly perfect transient response with AVP control.

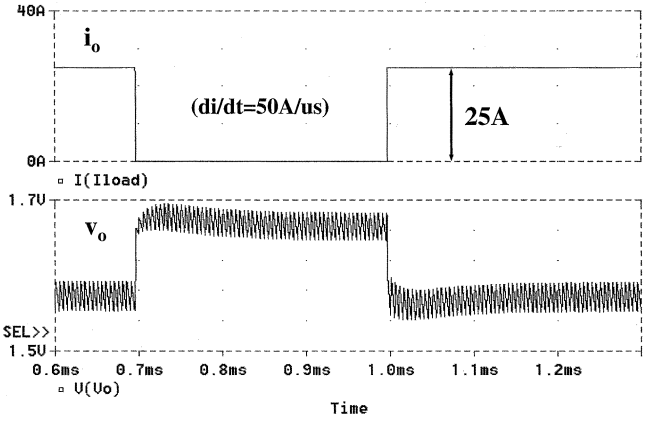


Fig. 7. Simulation results with voltage-mode control.

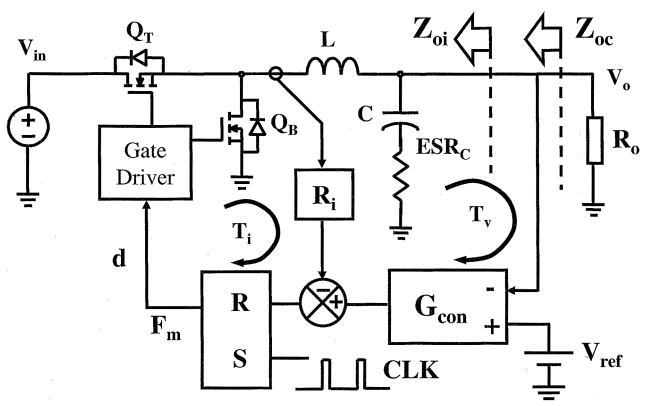


Fig. 8. Buck converter using current-mode control.

B. Current-Mode Control

For current-mode control, the analysis is slightly more complicated. Fig. 8 shows the dual-loop feedback control system. The peak-current-mode control is used as an example for this analysis. Since the current loop design is normally fixed according to the applied control chip, the major issue is how to design the voltage loop compensator.

With the current loop closed, the output impedance with the open voltage loop is

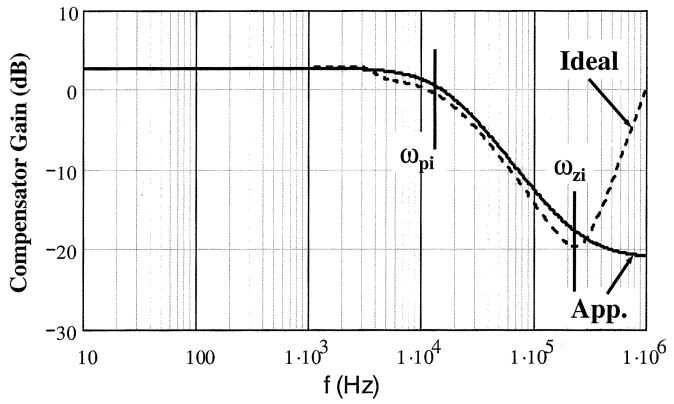
$$Z_{oi}(s) = Z_o(s) + \frac{T_i(s)}{1 + T_i(s)} \cdot \frac{G_{\mathrm{vd}}(s) \cdot G_{\mathrm{ii}}(s)}{G_{\mathrm{id}}(s)} \tag{11}$$

where $\mathrm{T_i(s)}$ is the current loop gain, $\mathrm{G_{ii}(s)}$ is the inductor current to the load current transfer function, and $\mathrm{G_{id}}$ (s) is the inductor current to the duty cycle transfer function.

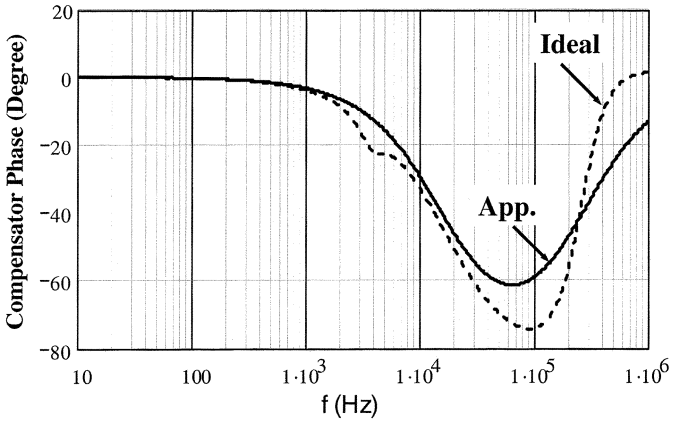
The output impedance with the both loops closed is

$$Z_{\mathrm{oc}}(s) = \frac{Z_{\mathrm{oi}}(s)}{1 + T_2(s)} = \frac{(1 + T_i(s)) \cdot Z_{\mathrm{oi}}(s)}{1 + T_i(s) + F_m \cdot G_{\mathrm{vd}}(s) \cdot G_{\mathrm{con}}(s)} \tag{12}$$

where $\mathrm{T_2(s)}$ is the outer loop gain, which determines the system bandwidth and phase margin.



(a)



(b)

Fig. 9. Compensator design for current mode-control.

Fig. 9 shows the ideal compensator transfer function necessary to achieve $\mathrm{Z_{oc}} = \mathrm{ESR_C}$. As is the case for voltage-mode control, a real compensator with one pole and one zero comes sufficiently close to the ideal design, as

$$G_{\mathrm{con}}(s) = K_i \frac{1 + s/\omega_{zi}}{1 + s/\omega_{pi}}. \tag{13}$$

Further mathematical analysis shows the detailed values of the dc gain, pole and zero, as

$$K_i \approx \frac{R_i}{\mathrm{ESR}_C} \tag{14}$$

$$\omega_{\mathrm{pi}} = \omega_c, \quad \text{and} \tag{15}$$

$$\omega_{\mathrm{zi}} = \pi \cdot f_s \tag{16}$$

where $\mathrm{R_i}$ is the current-sensing gain and $\mathrm{f_s}$ is the switching frequency. There is more physical meaning for the compensator design than existed in the case for voltage-mode control. A pole compensates the output capacitor ESR zero, and a zero compensates the double right-half-plane zero introduced by the current sample and hold effect.

Fig. 10 shows the closed-loop output impedance with this compensator design. It is almost constant. Simulation results given in Fig. 11 show the nearly perfect transient response with AVP control.

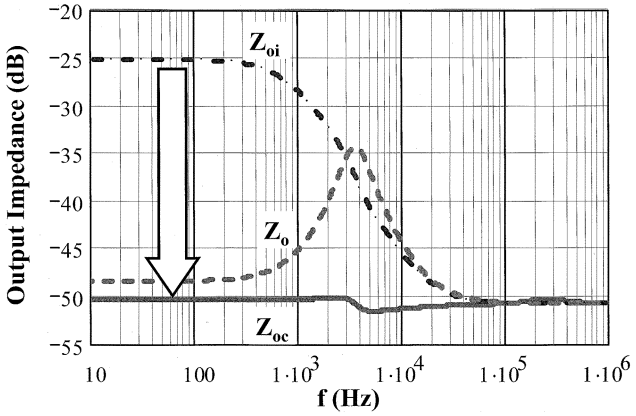


Fig. 10. Output impedance with current-mode control.

III. Limitation of the Constant Output Impedance Design

The previous section gives a simple design guideline for the compensator to achieve constant output impedance. However, the entire process is based on mathematical derivation. For a practical circuit design, there are many limitations.

A. Limitation of the Voltage-Mode Control

For voltage-mode control, if $\mathrm{R_L} < \mathrm{ESR_C}$, which is possible for VRM design, the dc gain will be negative, according to (7). This is impossible for a real design. Even with $\mathrm{R_L} > \mathrm{ESR_C}$, the dc gain is too low to attenuate the switching noise. Both the line and load regulations will have problems. Also, it is not easy to achieve current sharing between several channels with voltage-mode control.

The current-mode control is different. The closed current loop makes the converter operate like a current source, which has very high output impedance at low frequencies. The $\mathrm{Z_{oi}}$ in Fig. 10 shows this clearly. As a result, the outer loop $\mathrm{T_2}$ requires a high dc gain to attenuate the output impedance at low frequencies. The high dc gain eliminates all the problems that existed in the voltage-mode control. For practical designs, current-mode control is the only way to achieve constant output impedance.

B. Limitation Related to the Switching Frequency

Even with a current-mode control, there is a special requirement for the bandwidth to achieve constant output impedance. Mathematical analysis shows that the bandwidth is exactly on the ESR zero of the output capacitor, as

$$f_c = \frac{1}{2 \cdot \pi} \cdot \frac{1}{C \cdot \mathrm{ESR}_C}. \tag{17}$$

This is easy to understand, since the open-loop output impedance $\mathrm{Z_{oi}}$ (voltage loop open, but current loop closed) has a zero exactly on that point. Fig. 12 shows the relationship clearly.

However, the bandwidth design is limited by the switching frequency. Normally, the bandwidth can be designed only within $1/6$ of the switching-frequency range. Fig. 12 shows that if the

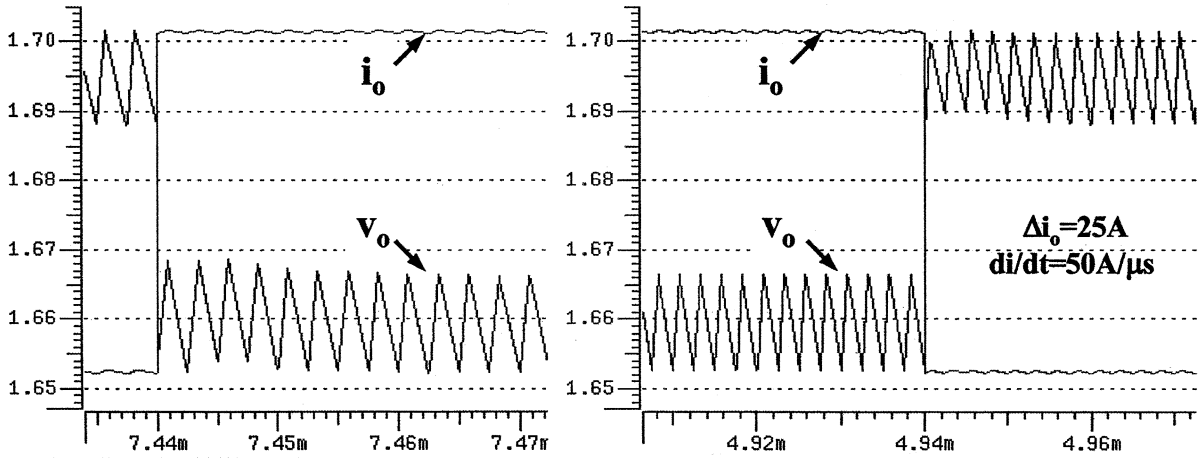


Fig. 11. Simulation results with current-mode control.

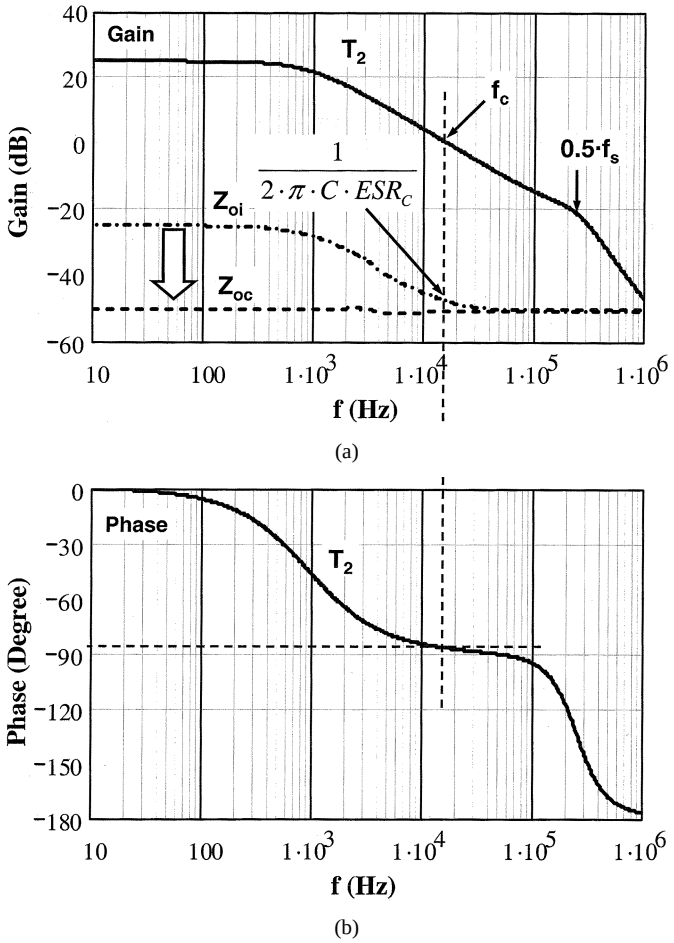


Fig. 12. Required outer-loop gain.

bandwidth is too near to half of the switching frequency, the system will not have sufficient phase margins and will become unstable. As a result, there is a special requirement for switching frequency in order to achieve constant output impedance design.

The ESR zeros of different kinds of output capacitors are different. Table I lists the ESR zeros of three major kinds of output capacitors for the VRM application. For the Oscon capacitor, there is no difficulty in achieving 16 KHz crossover frequency with 200–300 KHz switching frequency. The ESRE is a special kind of electrical film capacitor produced by Cornell Dubilier; its size is much smaller than that of the Oscon. However, a higher switching frequency is required to achieve the 40 KHz bandwidth. For the ceramic capacitor, a switching frequency of about 10 MHz is required to achieve the 1.1 MHz bandwidth.

TABLE I
ESR ZEROS FOR DIFFERENT KINDS OF CAPACITORS

Cap Type	Capacitance	ESR	ESR Zero
Oscon (SanYo)	820μF	12mΩ	16KHz
ESRE (CDE)	270μF	15mΩ	40KHz
Ceramic (TDK)	100μF	1.4mΩ	1.1MHz

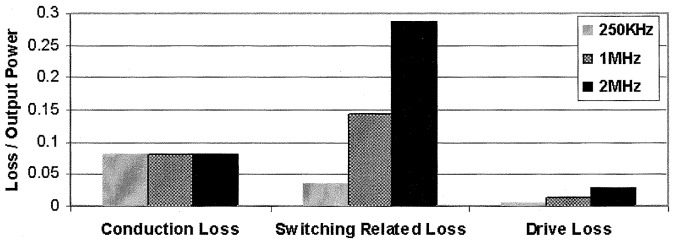


Fig. 13. Loss analysis for a synchronous buck converter.

However, the efficiency of VRMs limits the continuous increase of the switching frequency. Fig. 13 shows the loss analysis results for a 12 V-to-1.5 V/12.5 A synchronous buck converter, according to the method discussed in L. Spaziani's work [13]. The results can be scalable to multiphase higher output current conditions, for example, a four-phase 50 A VRM. The power devices are based on Siliconix's Si4842 (for top switch) and Si4442 (for bottom switch). Fig. 13 compares the conduction loss, switching-related loss and gate-drive loss at three different switching frequencies. To simplify the analysis, the inductor current ripples remain the same (25% of the load current) at different switching frequencies. As a result, at different switching frequencies, the conduction losses are the same, but the inductance values are different, as shown in the following:

$$L = \frac{V_0}{2 \cdot \Delta i_L \cdot f_c} \cdot (1 - D). \tag{18}$$

5 V-drive voltage level is used in the loss analysis. Although the drive loss is proportional to the switching frequency, it is still

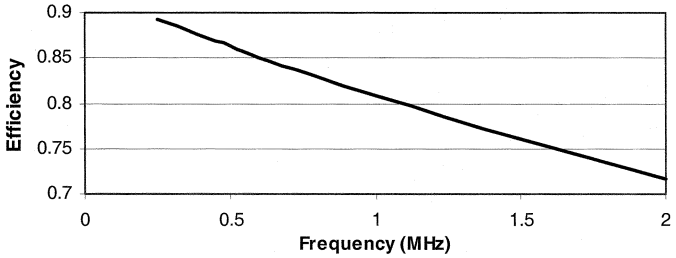


Fig. 14. Full load efficiency versus switching frequency.

not significant at 2 MHz switching frequency because of the low drive voltage level. But the switching-related loss is totally different. This portion of the loss includes power devices' turn-on and turn-off losses, bottom-switch body diode recovery loss, dead-time MOSFET body diode conduction loss, and MOSFET drain-source capacitor charging and discharging losses. All of these losses are proportional to switching frequency. At high frequencies, the switching-related loss dominates the entire power loss and causes a significant drop in efficiency. Fig. 14 shows this trend clearly.

The preceding analysis shows that in practical designs, there is a trade-off between the transient response and the efficiency. Designing for constant output impedance is the best way to achieve AVP control with the minimum number of the output capacitors. Only the ESR of the output capacitor determines the transient voltage spikes. However, for certain kinds of capacitors, such as ceramic capacitors, it is difficult to apply this concept for AVP design because of the limitation of switching frequency. There are other design methods for achieving AVP, but they require more output capacitors. Further discussion will be published in the future.

C. Limitation Related to the Inductor Design

The analysis in Section III is based on the small-signal model. If the duty cycle is saturated, the closed-loop output impedance can no longer be used for transient analysis. Instead, the open-loop output impedance is effective. Since the open-loop output impedance is much larger than that of the closed loop, the transient response of the former will be worse. To guarantee a good transient voltage waveform, the duty cycle should not become saturated.

The critical inductance concept [8], [12] reveals the point at which the duty cycle will go to saturation in a voltage-mode-controlled VRM. The crossover frequency determines the critical inductance value, above which the duty cycle will go to saturation, as

$$L_{\mathrm{cv}} = \frac{V_{\mathrm{in}}}{4 \cdot \Delta I_o \cdot f_c} \cdot \min(D, 1-D). \tag{19}$$

In the same way, a critical inductance value can be also derived for the current-mode control. Fig. 15 shows the current transfer function $\mathrm{G_{ii}(s)}$, and Fig. 16 shows the step-response inductor current (normalized to the load current $\Delta \mathrm{I_o}$) with peak-current-mode control. The inductor current with a closed loop responds to the step-load current change as a first-order system,

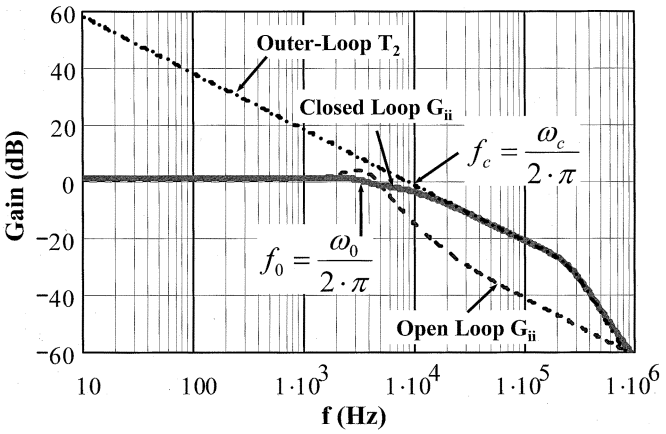


Fig. 15. Inductor current transfer function of current-mode control.

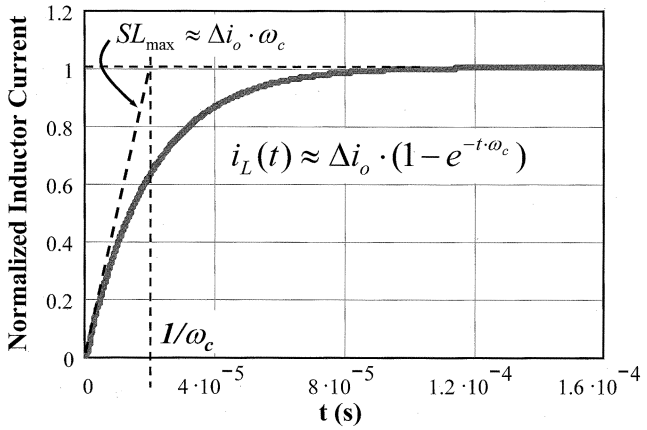


Fig. 16. Step-response of the inductor current.

in which the time constant is simply the bandwidth. The average inductor current during the transient is approximated as

$$i_L(t) \approx \Delta I_o \cdot (1 - e^{-t \cdot 2 \cdot \pi \cdot f_c}) \tag{20}$$

where f_c is the crossover frequency.

The inductor current slew rate with average small-signal model is approximated as

$$\mathrm{SL}_{i_L}(t) \approx \Delta I_o \cdot 2 \cdot \pi \cdot f_c \cdot e^{-t \cdot 2 \cdot \pi \cdot f_c}. \tag{21}$$

However, the maximum inductor current slew rate cannot exceed the Faraday Law limitation, in which $\mathrm{di/dt} = \mathrm{V_o/L}$ for step-down and $\mathrm{di/dt} = (\mathrm{V_{in}} - \mathrm{V_o})/\mathrm{L}$ for step-up. The larger value from (21) means the duty cycle is saturated and the small-signal model is no longer effective. The equivalent points give the critical inductance value

$$L_{\mathrm{ci}} = \frac{V_{\mathrm{in}}}{2 \cdot \pi \cdot \Delta I_o \cdot f_c} \cdot \min(D, 1-D). \tag{22}$$

As a result, in order to avoid duty-cycle saturation, the output filter inductor should be designed such that its value is not higher than the critical inductance. Since a larger inductance value can improve efficiency by reducing the current ripple, the critical inductance value is a good design point for both transient and efficiency considerations. The critical inductance is not an accurate value, but it can help the engineer design process. For

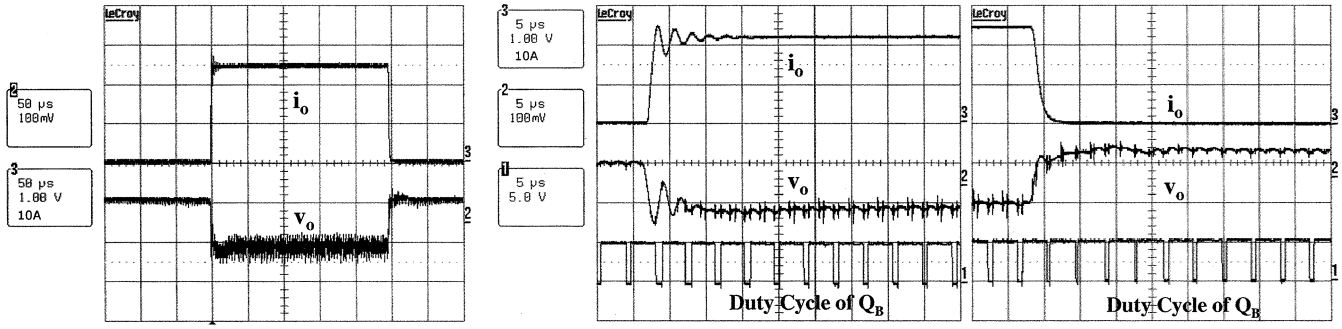


Fig. 17. (a) Experimental results for the transient, (b) extended waveform for step-up, and (c) extended waveform for step-down.

current-mode control, it is related only to the initial inductor current response speed. After that, the duty cycle will not saturate even with a larger inductance. As long as the inductor is designed according to the critical inductance value, it will not have too great impacts on the transient response even there is slight duty-cycle saturation when the transient begins.

IV. Design Example

Based on the understanding of the constant output impedance design and its related limitations, an optimal design for certain output capacitors can be achieved, which simultaneously considers VRM size, transient and efficiency. A design process is shown here for a 12 V-to-1.6 V/25 A VRM using the Oscon capacitor, which is listed in Table I. The required voltage tolerance is 100 mV.

With the constant output impedance design, the ESR of the output capacitor limits the transient voltage spike. In order to meet the 100 mV transient voltage spike requirement with a 25 A load current transient, the ESR of the output capacitors should be less than 4 mW. Although three capacitors in parallel can realize 4 mW output impedance, four are selected due to considerations given to the ESR tolerance and some soldering and trace impedance.

A commercial peak-current controller (SIL6560) for two-phase interleaving is selected for the VRM design. It can automatically achieve current-sharing, and the compensator can be designed (according to the discussion in Section II) to achieve constant output impedance. The outer-loop bandwidth is at exactly 16 KHz, which is the ESR zero of the Oscon capacitor.

Then, the output filter inductance can be determined based on the critical inductance value. 500 nH is selected according to (22) so that the inductance of each channel is 1 μH. This inductance value can guarantee that the duty cycle will not become saturated during the transient.

Finally, the switching frequency is selected according the bandwidth and the inductor current ripple. Here, a 250 KHz switching frequency is selected, which easily achieves 16 KHz crossover frequency with a stable system, and which is good enough to limit the inductor current ripple to 21% of the inductor dc current. Also, the switching frequency is not so high that the switching loss remains relatively small.

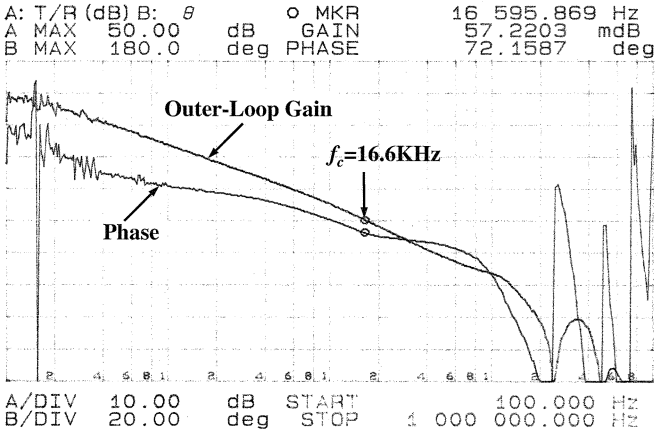


Fig. 18. Tested outer-loop gain and phase.

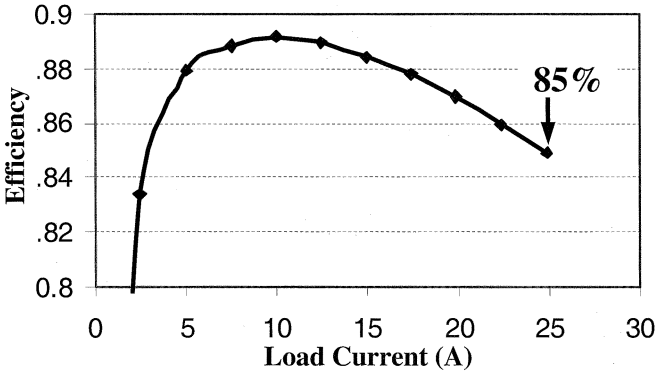


Fig. 19. Tested efficiency.

Two MOSFETs with SO-8 packages are used in each channel; one for the top switch Q_T and another for the bottom switch Q_B. Si4842 is selected for Q_T because of its low gate charge, and Si4442 is selected for Q_B because of its low R_{ds_on}. The gate driver LM2726 is selected for its fast driving capability and very small dead time. Vishay's surface-mounted inductor IHLP-5050CE is used for its small size and low profile.

Fig. 17(a) shows the tested transient response waveform with the constant output impedance design. Perfect AVP is achieved. Figs. 17(b) and (c) show the extended transient waveforms during the step-up and step-down periods. With the critical inductance design, the duty cycle is not saturated during the transient response. The tested outer-loop bandwidth

in Fig. 18 shows that the crossover frequency is exactly on the ESR zero of the output capacitor. Fig. 19 shows the high efficiency achieved by using only four SO-8 MOSFETs, based on the optimal design process.

V. Conclusion

This paper discusses the constant output impedance design method utilized to achieve perfect AVP for the VRM transient response. Both the voltage-mode and current-mode controls can achieve constant output impedance. The limitation of voltage-mode control is discussed. For current-mode control, the bandwidth is on the ESR zero of the output capacitor, such that the output capacitor determines the feasibility of the constant output impedance design method. Also, the limitation of the small-signal model shows the design guideline for the output filter inductance. Finally, an optimal design process is proposed, and a design example is given that achieves small size, high efficiency and good transient response. Simulation and experimental results prove that the use of the constant output impedance is a good design method.

References

[1] *VRM 9.0 DC-DC Converter Design Guidelines*, Apr. 2001. Intel document.

[2] M. Zhang, "Powering Intel Pentium 4 processors," in *Proc. Intel Technol. Symp.*, 2000.

[3] A. Waizman and C. Y. Chung, "Resonant free power network design using extended adaptive voltage positioning (EAVP) methodology," *IEEE Trans. Adv. Packag.*, vol. 24, pp. 236–244, Aug. 2001.

[4] R. Redl and N. O. Sokal, "Near-optimum dynamic regulation of DC-DC converters using feed-forward of output current and input voltage with current-mode control," *IEEE Trans. Power Electron.*, vol. 1, pp. 181–192, July 1986.

[5] G. K. Schoneman and D. M. Mitchell, "Output impedance considerations for switching regulators with current-injected control," *Proc. IEEE PESC*, pp. 324–335, 1987.

[6] L. D. Varga and N. A. Losic, "Synthesis of zero-impedance converter," *IEEE Trans. Power Electron.*, vol. 7, pp. 152–170, Jan. 1992.

[7] R. Redl, B. P. Erisman, and Z. Zansky, "Optimizing the load transient response of the buck converter," *Proc. IEEE APEC*, pp. 170–176, 1998.

[8] P. L. Wong, "Performance improvements of multi-channel interleaving voltage regulator modules with integrated coupling inductors," Ph.D. dissertation, Virginia Tech., Blacksburg, VA, Mar. 2001.

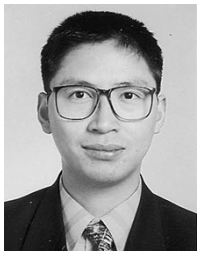
[9] R. Tymerski, V. Vorperian, F. C. Lee, and W. T. Baumann, "Nonlinear modeling of the PWM switch," *IEEE Trans. Power Electron.*, vol. 4, pp. 225–233, Apr. 1989.

[10] R. B. Ridley, B. H. Cho, and F. C. Lee, "Analysis and interpretation of loop gains of multiloop-controlled switching regulators," *IEEE Trans. Power Electron.*, vol. 3, pp. 489–498, Oct. 1988.

[11] R. B. Ridley, "A new continuous-time model for current-mode control," *IEEE Trans. Power Electron.*, vol. 6, pp. 271–280, Apr. 1991.

[12] P. L. Wong, F. C. Lee, P. Xu, and K. Yao, "Critical inductance in voltage regulator modules," *Proc. IEEE APEC*, 2002.

[13] L. Spaziani, "A study of MOSFET performance in processor targeted buck and synchronous rectifier buck converters," *Proc. HFPC'96 Conf.*, pp. 123–137, 1996.



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