Feedback design for the Buck Converter

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Abstract

In this paper we explore two compensation topologies for the Buck DC to DC power converter, dominant pole and dominant pole with zero compensation. These feedback systems are developed and implemented with an Op-Amp circuit design, and each system is tested with a step disturbance at the system input voltage. Each system response is compared to the uncompensated converter through simulation and Bode plot analysis.

Introduction

The Buck converter, shown in Figure 1, is a simple converter topology that has several applications in DC to DC power conversion. The aim of this report is to explore the behavior of this converter in response to step disturbances to the system input, and explore a few compensation techniques to improve the converter's response to those input disturbances. Particularly, different varieties of dominant pole compensation will be explored involving two implementations of Proportional Integral (PI) compensation.

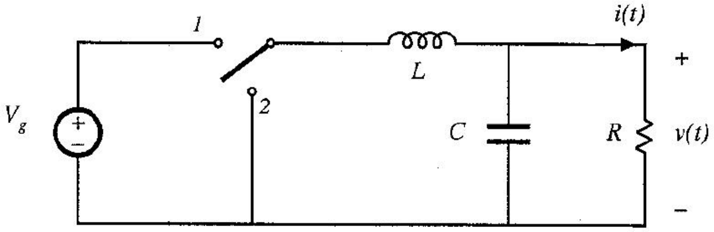

Figure 1: The ideal Buck converter (Source: Erickson)

Section one will explore the uncompensated Buck converter, and how the system responds to a voltage step at the input. Section two will describe a dominant pole compensation technique, which will act to decrease the effect of the step response at the output. In section three, a zero will be added to the system at the corner frequency of the Buck converter and section four will reduce the peaking of the system. Each technique has it's advantages, and each will be explored.

1) The Uncompensated Buck Converter

Figure 1 shows the topology of the Buck converter. Using Steady-State analysis techniques, the output of the converter can be calculated to be equal to DV_g, the duty cycle of the switch multiplied by the input voltage. Typically, a Pulse Width Modulated (PWM) signal is used to drive the switch in the circuit. Figure 2 [1] shows a basic buck converter PWM control loop. For the purpose of this analysis, the circuit is designed to operate in continuous conduction mode, with the input to the system as a step response from $28V \Rightarrow 30V \Rightarrow 28V$.

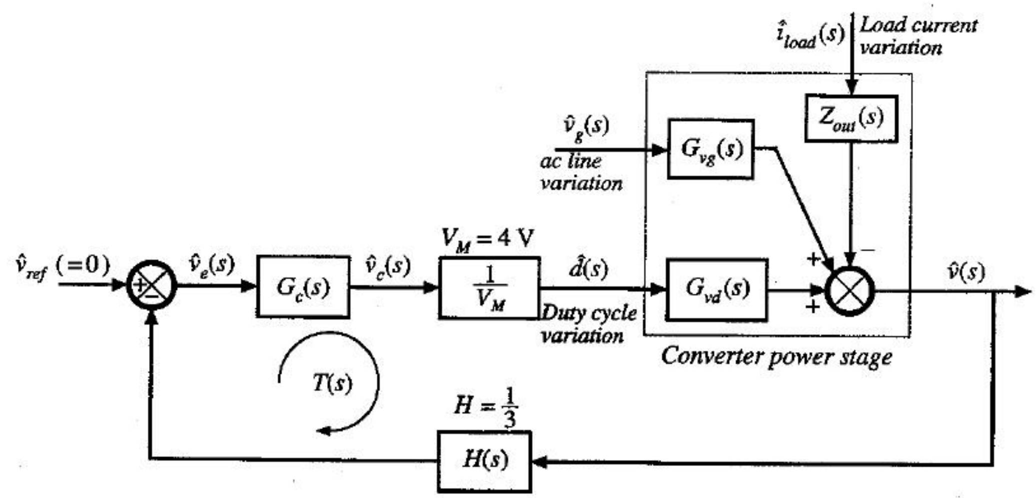

Figure 2: Buck converter control loop (Source: Erickson)

The basic topology for the converter control loop is shown above, where G_c is the compensation scheme used in the circuit, V_m is the transfer function of the pulse width modulator, and $H(s)$ is the conversion factor. The conversion factor is used to reduce the amplitude of the output to a level that will cancel the value of the system reference voltage. In practice, there will always be a small difference between $H(s)V(s)$ and the reference, which is defined as the error signal V_e. With a large enough compensation loop gain, the error signal will be able to provide enough voltage for the output to follow the reference [1, p. 332]. For the purpose of this report, assume that G_{vg} applies step disturbances to the system and Z_{out} has no contribution to the system response.

From [1], the transfer function of a Buck converter can be shown to be equal to the function below, where

$$G_p(s) = \frac{G_{p0}}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \; , \tag{1}$$

$$G_p(s) = \frac{G_{p0}}{1 + \frac{sL}{R} + s^2 LC} \; , \tag{2}$$

For the converter topology of this paper, the parameter values of the transfer function are shown below:

$$G_{p0} = V_g = 28, \quad f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{LC}} = 1KHz, \quad \text{and} \quad Q = R\sqrt{\frac{C}{L}} = 9.49 = 19.5dB$$

The loop gain of the system is defined as

$$T(s) = G_c(s)G_p(s)H(s)G_{pwm}(s) = \frac{T_0}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

Using the given values for the control loop, and setting $G_c(s) = 1$ for an uncompensated converter, the values of the control loop variables can be defined as shown below:

$$T_0 = G_c(s)H(s)G_{pwm}(s) = 2.33, \quad G_c = 1, \quad H(s) = \frac{1}{3}, \quad \text{and} \quad G_{pwm} = \frac{1}{4}$$

An asymptotic Bode plot has been created for the system and is shown in Figure 3. For this uncompensated converter design, the phase margin is read to be 0°. Realistically, the phase margin is a small positive value since the phase never reaches −180°, but is on the verge of instability. This could be a problem if the feedback loop was closed on this system, but for this portion the system is in an open loop configuration. Since the phase only approaches −180° but never reaches it, the gain margin is defined as infinite.

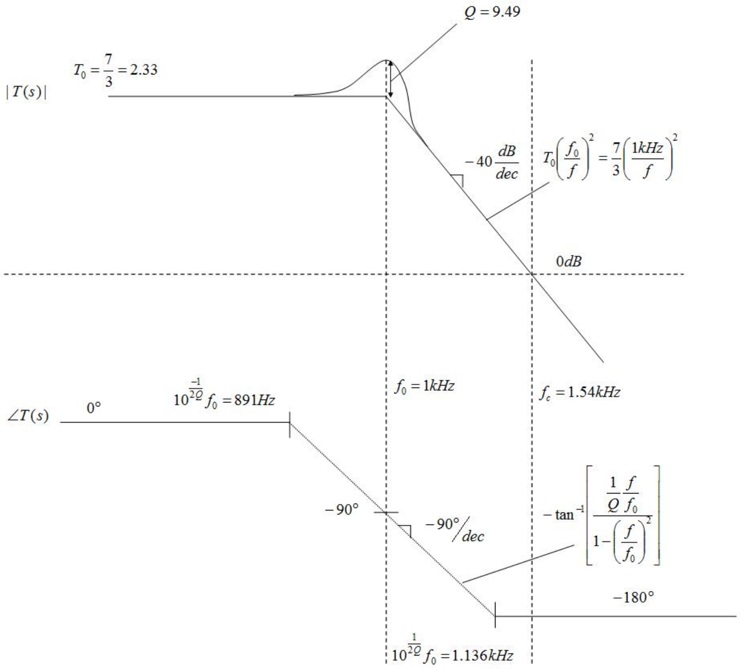

Figure 3: Uncompensated Buck converter

Figure 4 shows the response of the uncompensated Buck to a step disturbance at it's input. Because the system is uncompensated, the step response is translated to the the output of the system. In the following sections, compensation techniques will be explored to improve the system reponse to changes in the input voltage.

2) Dominant Pole Compensation (3 dB gain margin)

One way to improve the response of the buck converter is to introduce dominant pole compensation. Dominant pole compensation introduces an integrating circuit into a feedback loop. This particular integrating

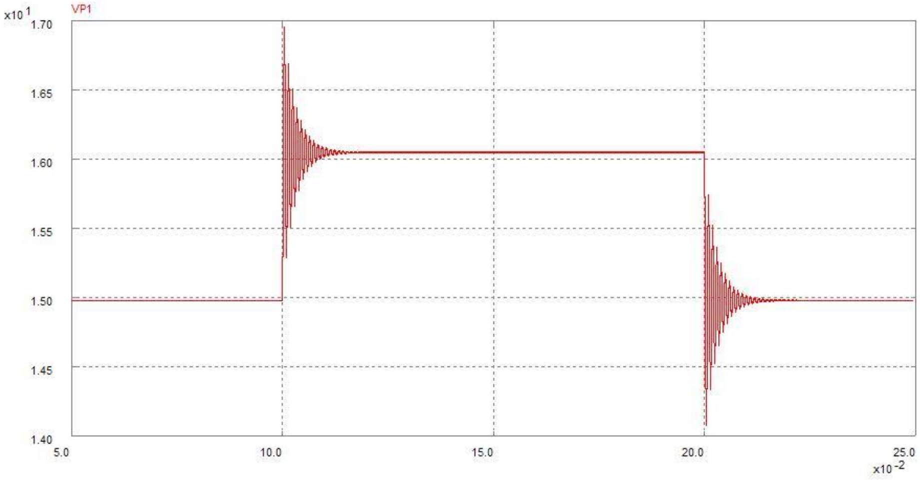

Figure 4: Uncompensated Buck converter system response to input voltage step

circuit will serve two purposes. The first will be to increase the phase margin so the system will be stable in a feedback configuration. The second is to design the converter with less gain to improve the system stability.

Figure 5 is an Op-Amp implementation of an integrator, or dominant pole compensation. The basic equation for a dominant pole is shown below, and is incorporated into the loop gain of the system.

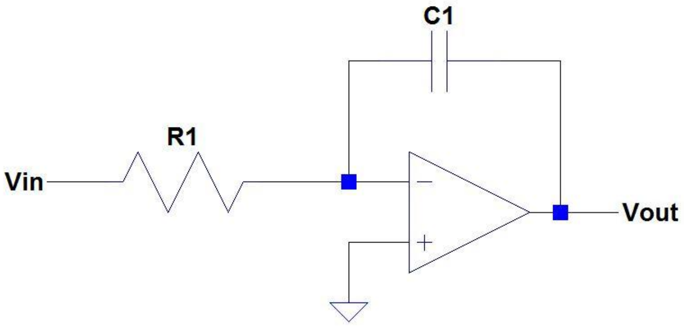

Figure 5: Dominant pole op-amp implementation

$$G_c(s) = \frac{G_{c0}}{s} \tag{3}$$

$$T(s) = \frac{T_0 G_{c0}}{s\left(1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right)} \tag{4}$$

To design this system for a 3 dB gain margin, it is required for the gain to be equal to .707 where the phase crosses $-180°$. Using Bode plot analysis (see Figure 7), the frequency where the phase is equal to

$-180°$ is found to be 1000 Hz. Using previously calculated parameters and the given values, the gain of the compensator can be calculated, as shown below.

$$\frac{T_0 G_{c0} Q}{2\pi f_0} = -3\text{ dB} = .707$$

$$G_{c0} = \frac{2\pi f_0 (.707)}{T_0 Q}$$

$$G_{c0} = \frac{2\pi\,(1000\text{ Hz})\,(.707)}{(2.33)(9.49)}$$

$$G_{c0} = 201$$

In the equation below, resistor and capacitor component values are calculated to realize the gain of the system.

$$G_c(s) = \frac{G_{c0}}{s} = \frac{1}{s}\frac{1}{R_1 C_1} \tag{5}$$

$$G_{c0} = \frac{1}{R_1 C_1} \tag{6}$$

Setting

$$R1 = 10k\Omega, \quad C1 = \frac{1}{G_{c0} R1} = \frac{1}{(201)(10k\Omega)} = 0.5\mu\text{F}$$

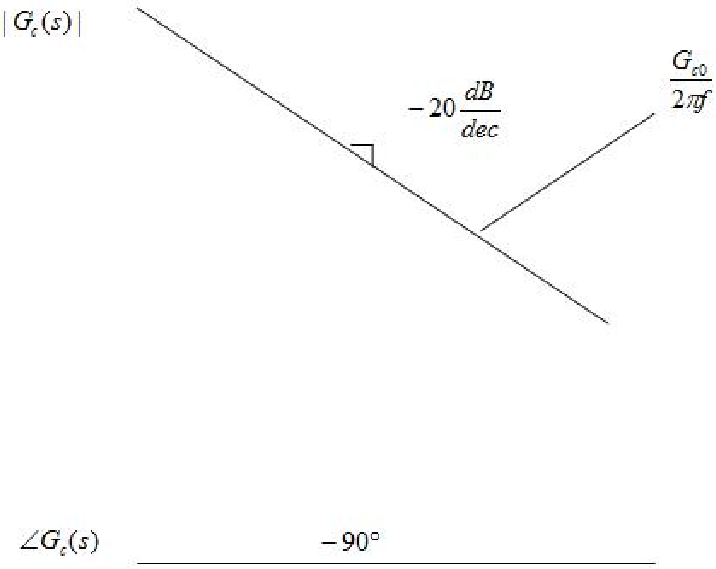

Figure 6: Compensation transfer function

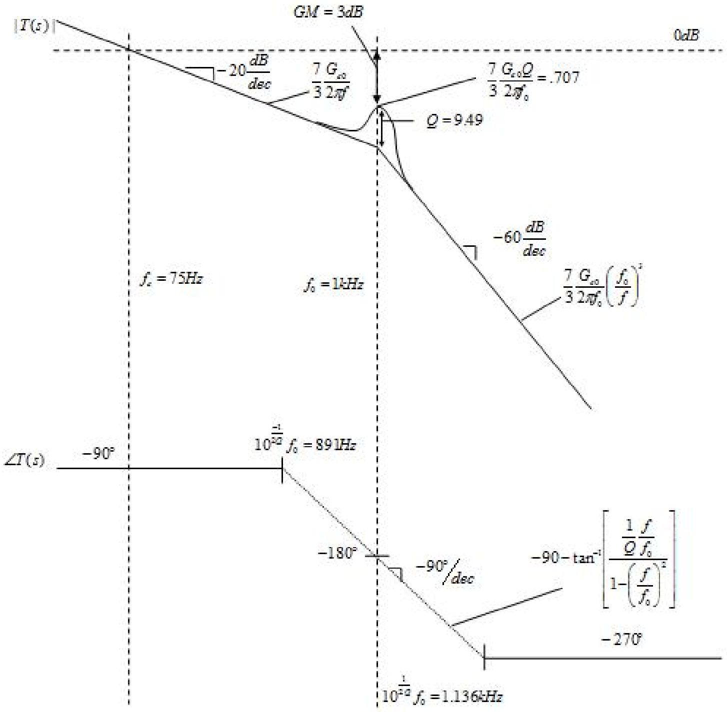

Figure 7: Dominant pole compensation loop gain

From the asymptotic bode plot (Figure 7), the gain and the phase margin of the system can be calculated directly. By design, the gain margin is equal to 3 dB.

$$fc = \frac{(2.33)(201)}{2\pi} = 74 \text{ Hz}$$

$$\phi_M = 180^\circ - 90^\circ = 90^\circ$$

$$\frac{T_0 G_{c0} Q}{2\pi f_0} = -3 \text{ dB} = .707$$

$$G_M = 3 \text{ dB}$$

Figure 8 shows the response of the dominant pole compensation to a step disturbance at its input. Because of the high Q factor in the system, there is definite overshoot and oscillation in the response as the output decays back down to the expected value of 15 Volts. Clearly, the dominant pole compensation is working to oppose the step disturbance on the input. Next we will explore the effect of adding a zero at the system corner frequency.

3) Dominant Pole with Zero Compensation (∼3 dB gain margin)

To obtain better performance and control of this system it can be advantageous to incorporate a zero, at some higher frequency, to the transfer function. Specifically, a zero will be placed at the corner frequency of the Buck converter. A zero will act to reduce the effect of the second order complex pole, which will decrease the roll off. The phase at 1000 Hz will be effected by the zero, and rise from -180° to -135°. As a

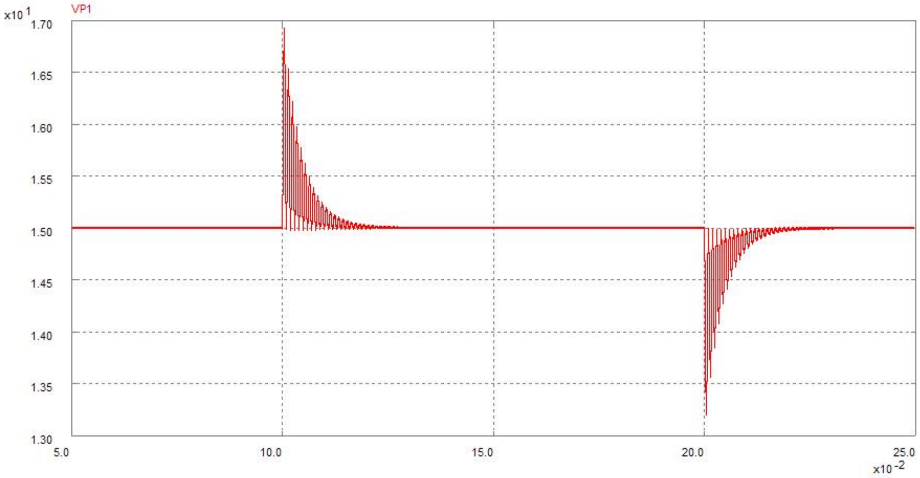

Figure 8: Step response of dominant pole compensated buck converter

starting point for the design, the feedback system uses this frequency for the gain margin, even though the gain margin will change. The transfer function of the compensator is shown below, as well as the changes to the complete transfer function.

$$G_c(s) = \frac{G_{c0}\left(1+\frac{s}{\omega_z}\right)}{s} \tag{7}$$

$$T(s) = T_0 G_{c0}\frac{1+\frac{s}{\omega_z}}{s\left(1+\frac{s}{Q\omega_0}+\left(\frac{s}{\omega_0}\right)^2\right)} \tag{8}$$

Analysis of this compensator topology is very similar to that of the dominant pole compensator. With the zero occuring at the corner frequency of the system, G_{c0} will be the same value.

To achieve the form of the transfer function shown in Equation 7, a PI Op-Amp topology will be used. Calculating the transfer function of the Op-Amp circuit shown in Figure 10, and substituting the parameters of the system, components values are calculated to realize the compensation scheme.

$$\frac{V_{out}}{V_{in}} = \frac{1}{R_1C}\frac{(sCR_2+1)}{s} = \frac{1}{R_1C}\frac{\frac{s}{\frac{1}{CR_2}}+1}{s}$$

It can be seen from the equation above that $\omega_z = \frac{1}{CR_2}$ and $G_{c0} = \frac{1}{CR_1}$. Using the calculated gain value ($G_{c0} = 201$), setting $R_2 = 10k\Omega$ and realizing that $f_0 = 1kHz$, the unknown component values can be calculated.

$$C = \frac{1}{R_2\omega_0} = \frac{1}{2\pi(1kHz)(10k\Omega)} = 15nF$$

$$R_1 = \frac{1}{CG_{c0}} = \frac{1}{201(15nF)} = 311k\Omega$$

Figure 12 shows the response of the dominant pole with zero compensation to a step disturbance at it's input. Similar to the dominant pole compensation, the system provides PI compensation and the step disturbances are corrected. Although this system's stability has been improved, the output is observed to be nearly the same.

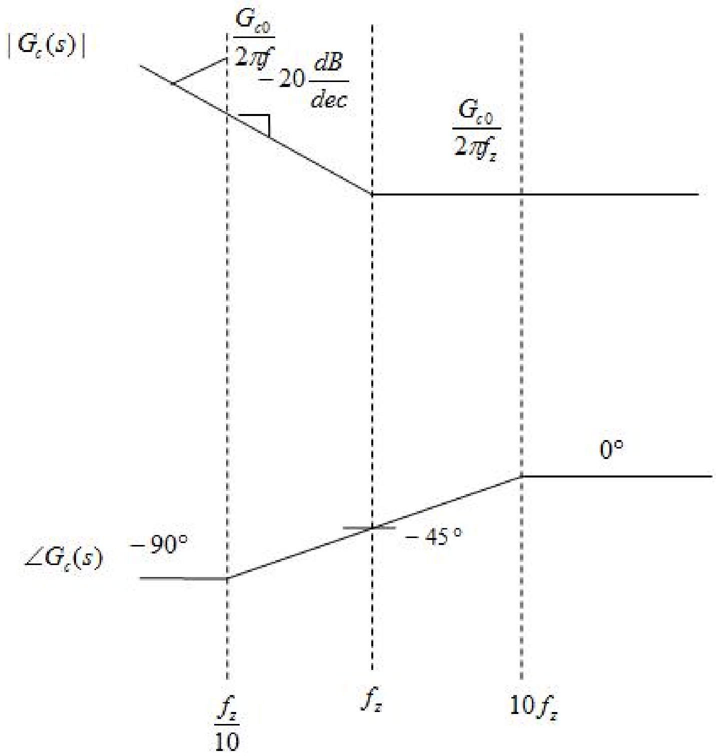

Figure 9: Dominant pole with zero compensation

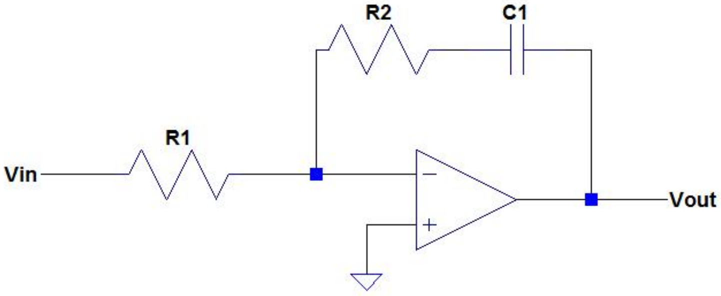

Figure 10: Dominant pole with zero Op-Amp implementation

The phase margin for this system is identical to that of the previous compensation design, because the added zero occurs after the unity-gain crossover point. To calculate the gain margin it's necessary to know where the phase crosses $-180°$. To determine this value, the phase at the lowest point presented on the asymptotic bode plot in Figure 11 needs to be calculated. The exact formula for the phase can be found on

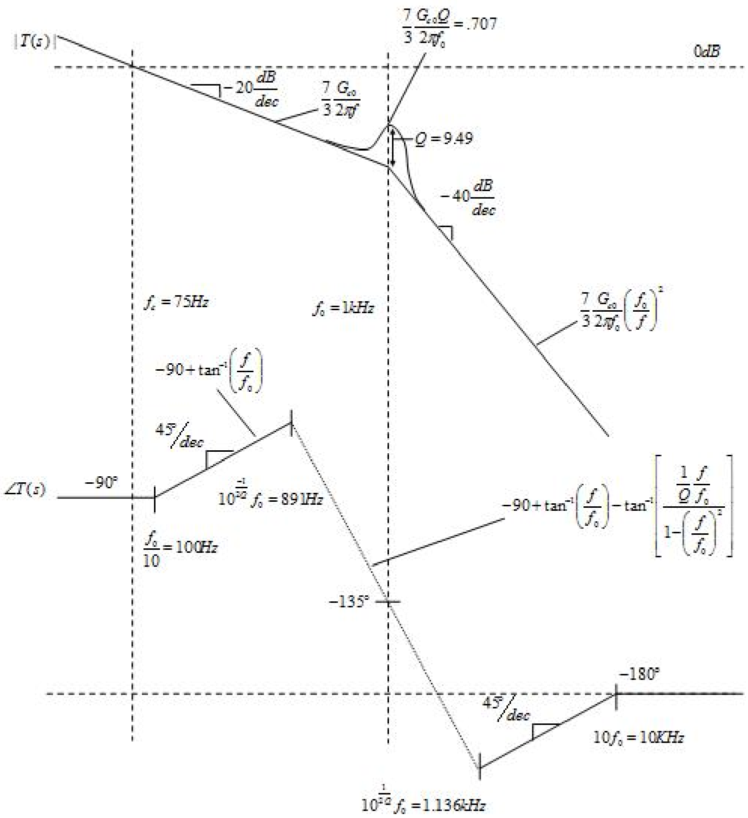

Figure 11: Dominant pole with zero compensation loop gain

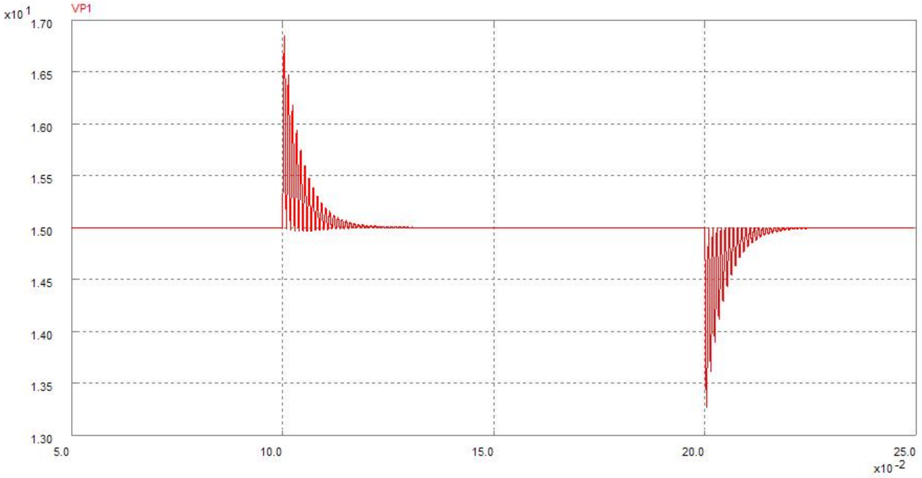

Figure 12: Step response of dominant pole with zero compensated buck converter (∼3 dB gain margin)

the bode plot and is also shown below:

$$-90^\circ + atan(\frac{f}{f_0}) - atan(\frac{\frac{1}{Q}\frac{f}{f_0}}{1-(\frac{f}{f_0})^2}) = \phi$$

Taking the frequencies shown on the bode plot and using the formula shown above, the exact phase at its lowest point is:

$$-90^\circ + atan(\frac{1.136kHz}{1kHz}) - atan(\frac{\frac{1.13}{9.49}}{1-(1.13)^2}) = -145.35^\circ$$

According to the above calculation, the approximations made using bode plot analysis shows that there is a significant deviation from the value of the actual phase. The phase of the converter never crosses -180° even at it's lowest point. Therefore, the gain margin is by definition infinite.

In the final section, this feedback topology will be adjusted so the peaking of the system at the corner frequency is lowered from -3dB to approximately -10 dB.

4) Dominant Pole with Zero Compensation (>10 dB gain margin)

For this design, the topology from section three will be modified to reduce the peaking to -10 dB (or .32) below unity. The PI compensator will functionally remain the same, only the value of G_{c0} will change to account for the lower peaking. Using the equation for G_{c0} shown in Figure 11

$$G_{c0} = \frac{2\pi f_0(.32)}{T_0 Q} = \frac{2\pi(1000Hz)(.32)}{2.33(9.49)}$$

$$G_{c0} = 45.4$$

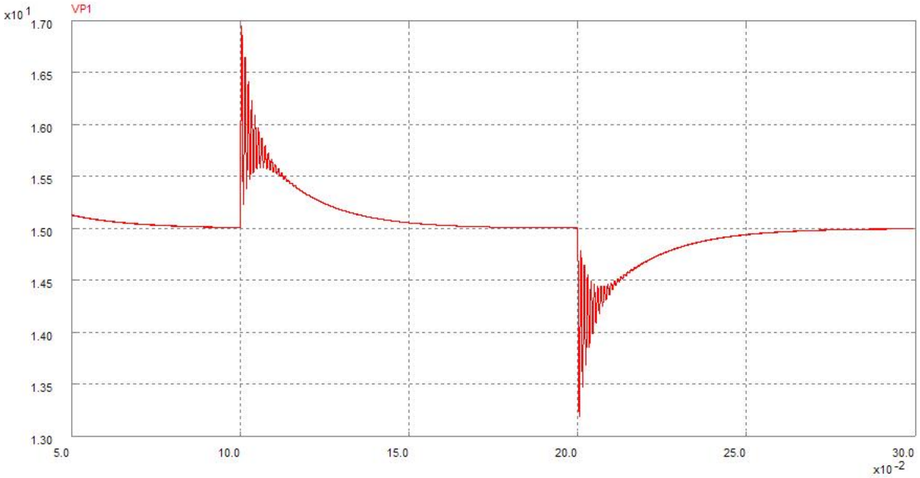

Figure 13: Step response of dominant pole with zero compensated Buck converter (>10 dB gain margin)

Using the PI compensator shown in section 3 and assuming that $R_2 = 10k\Omega$, solving for the new value of R_1:

$$R_1 = \frac{1}{R_2 G_{c0}} = \frac{1}{45.4(15nF)} = 1.3M\Omega$$

The value of the capacitor will not change. For gain and phase margins,

$$f_c = \frac{G_{c0}T_0}{2\pi} = \frac{45.4(2.33)}{2\pi} = 16.8Hz$$

Because only the gain of the system was reduced in this design, the bode plot is essentially the same, only with the gain of the system shifted down. The phase and gain margin are identical to that of section three. Figure 13 shows the response of the dominant pole with zero compensation to a step disturbance at it's input. With the inclusion of lower peaking, it is evident that the the system responds much slower to a step disturbance at the input. The system has less bandwidth and is slower to respond to disturbances.

Conclusion

The uncompensated Buck converter and three compensation methods were analyzed. The compensation methods have feedback which improve the stability of the output voltage in response to input disturbances. The uncompensated Buck converter simulations showed that input step disturbances directly affected the output of the system. The output never stabilized at the value it was designed for with the disturbance. Through interpretation of the output, it is realized that the uncompensated Buck converter implementation is unstable.

The first compensated design used a dominant pole. The simulation results showed the feedback of the system compensated for the input step disturbance and the output stabilized at the designed value. The next compensated design used a dominant pole with a zero added at the corner frequency. The simulation results were very similar to the first compensated design, even though the stability was increased. The last compensated design was the same as the previous, but with the system peaking lowered from -3dB to -10dB. The simulation results showed slower response to an input step disturbance; a result of the stability being increased. The increase in stability also decreased the bandwidth.

For this application the second compensated design had the best results. The stability was increased over that of the first design while the response time was comparable, and the fastest of all options considered. For applications where stability is a priority concern, it may be desirable to choose the last compensated design. The response time of the system will be compromised, but for greater stability.

References

[1] Robert W. Erickson and Dragan Maksimović. *Fundamentals of Power Electronics.* Springer Science+Business Media, LLC, second edition, 2001.

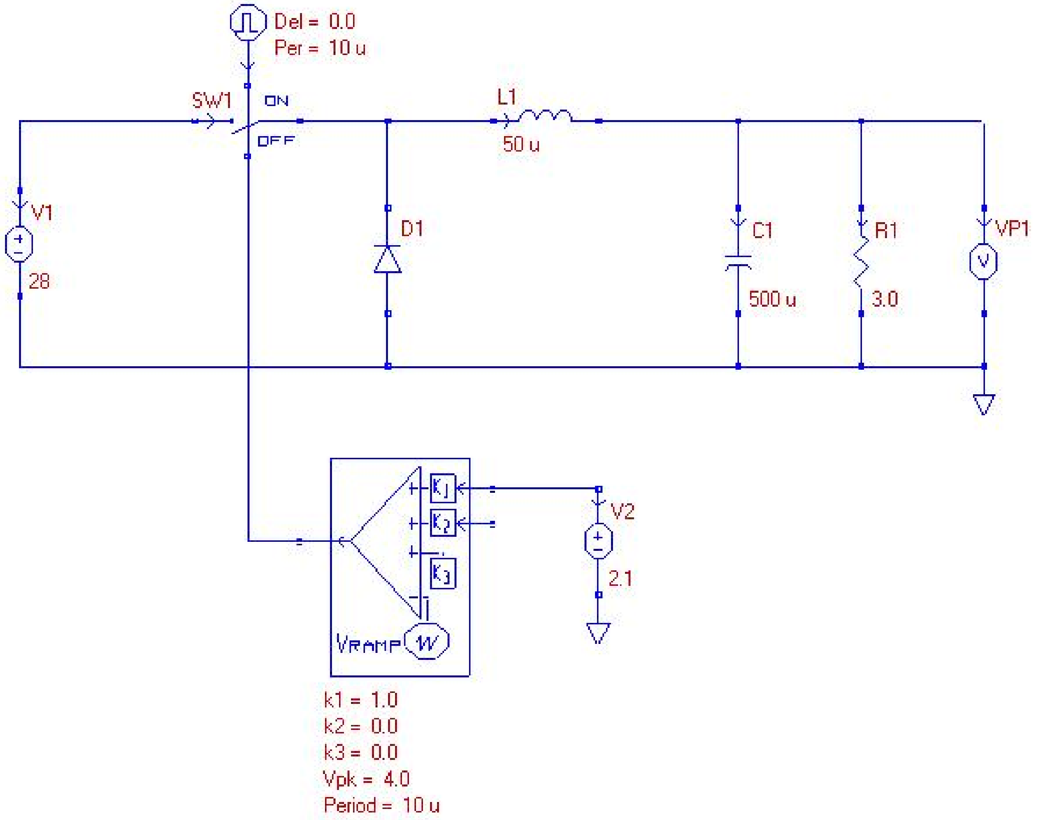

Figure 14: PECS schematic of uncompensated Buck converter

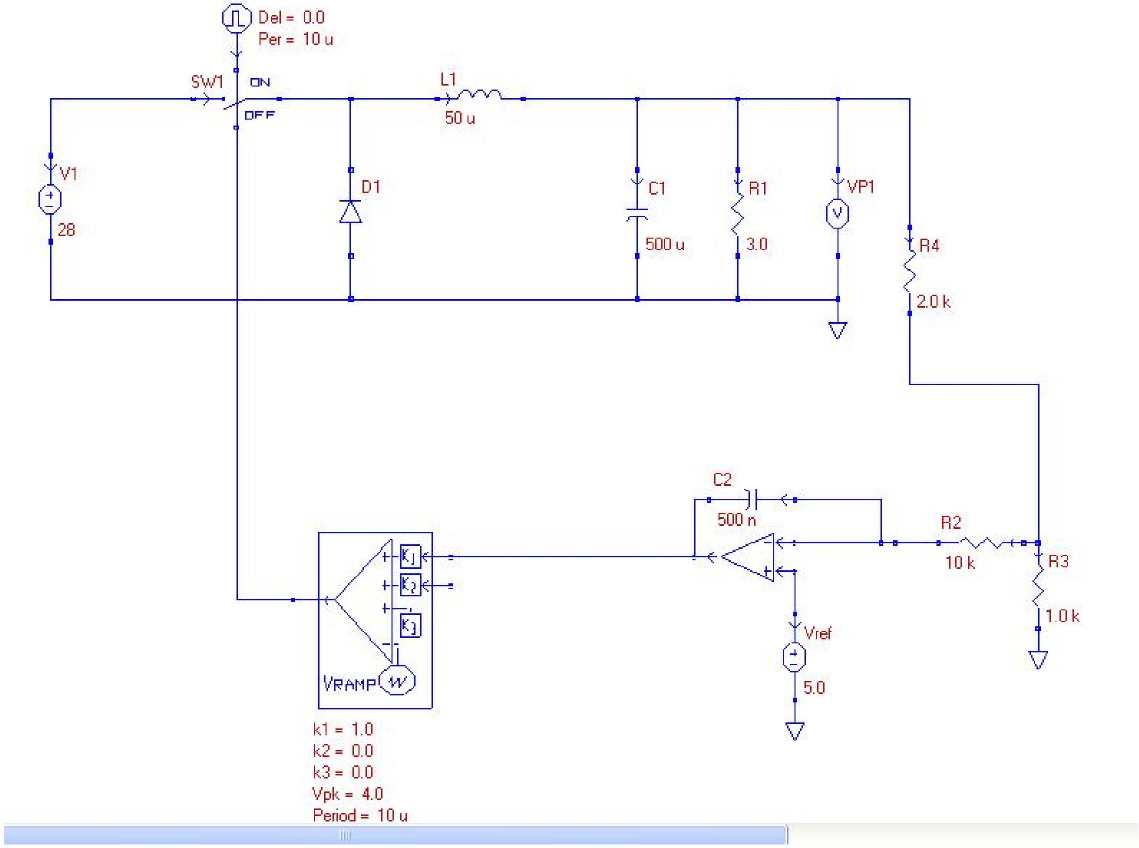

Figure 15: PECS schematic of dominant pole compensated Buck converter

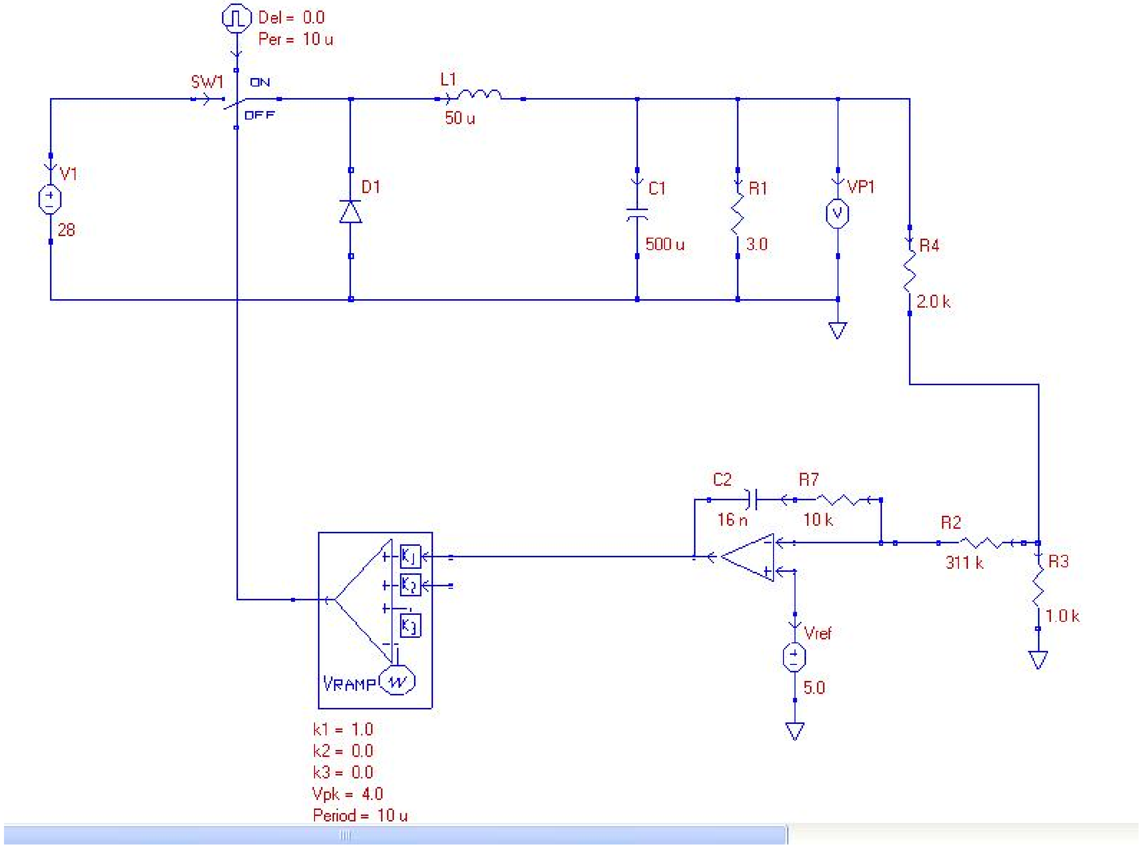

Figure 16: PECS schematic of dominant pole with zero compensated Buck converter (∼3dB)

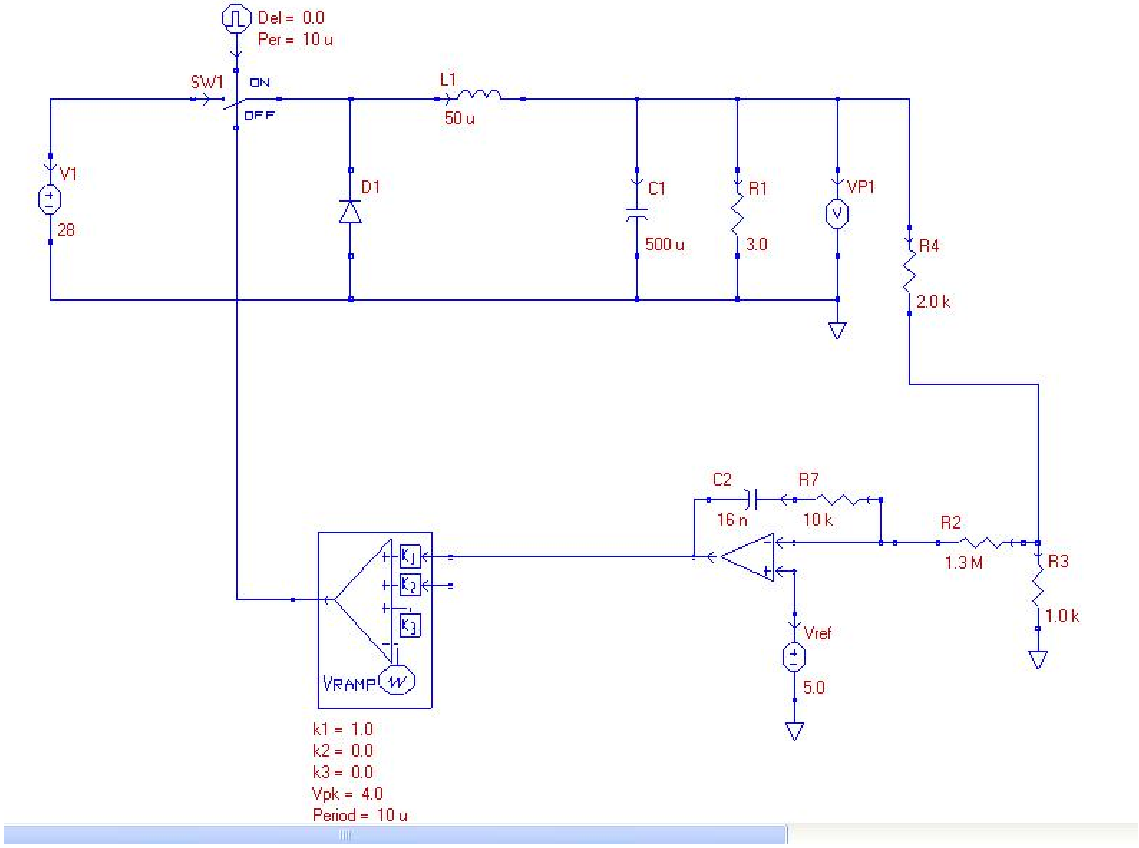

Figure 17: PECS schematic of dominant pole with zero compensated Buck converter (>10dB)