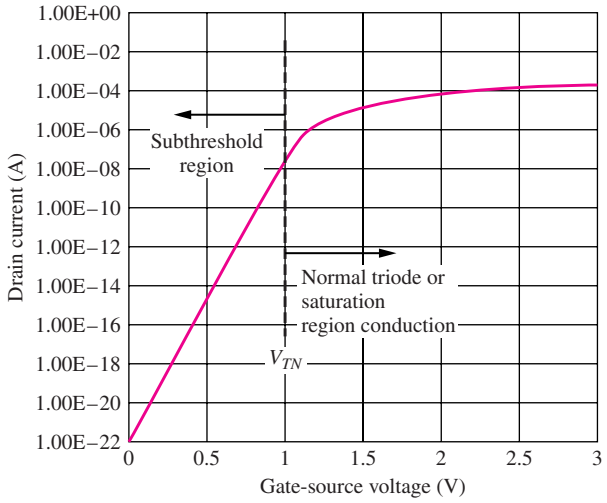

Figure 4.44 Subthreshold conduction in an NMOS transistor with $V_{TN} = 1$ V.

EXERCISE: (a) What is the leakage current in the device in Fig. 4.44 for $V_{GS} = 0.25$ V? (b) Suppose the transistor in Fig. 4.44 had $V_{TN} = 0.5$ V. What will be the leakage current for $V_{GS} = 0$ V? (c) A memory chip uses 10^9 of the transistors in part (b). What is the total leakage current if $V_{GS} = 0$ V for all the transistors?

ANSWERS: (a) $\cong 10^{-18}$ A; (b) $\cong 10^{-15}$ A; (c) $\cong 1$ μA

4.12 THE JUNCTION FIELD-EFFECT TRANSISTOR (JFET) (ADVANCED TOPIC)

Another type of field-effect transistor can be formed without the need for an insulating oxide by using *pn* junctions, as illustrated in Fig. 4.45. This device, the **junction field-effect transistor,** or **JFET,** consists of an *n*-type block of semiconductor material and two *pn* junctions that form the gate. Although less prevalent than MOSFETs, JFETs have many applications in both integrated and discrete circuit design, particularly in analog and RF and applications. In integrated circuits, JFETs are most often found in BiFET processes, which combine bipolar transistors with JFETs. The JFET provides a device with much lower input current and much higher input impedance than that typically achieved with the bipolar transistor.

In the ***n*-channel JFET,** current again enters the channel region at the drain and exits from the source. The resistance of the channel region is controlled by changing the physical width of the channel through modulation of the depletion layers that surround the *pn* junctions between the gate and the channel (see Sec. 3.1 and 3.6). In its triode region, the JFET can be thought of as simply a voltage-controlled resistor with its channel resistance determined by

$$R_{CH} = \frac{\rho}{t}\frac{L}{W} \tag{4.89}$$

where ρ = resistivity of the channel region

L = channel length

W = width of channel between the *pn* junction depletions regions

t = depth of channel into the page

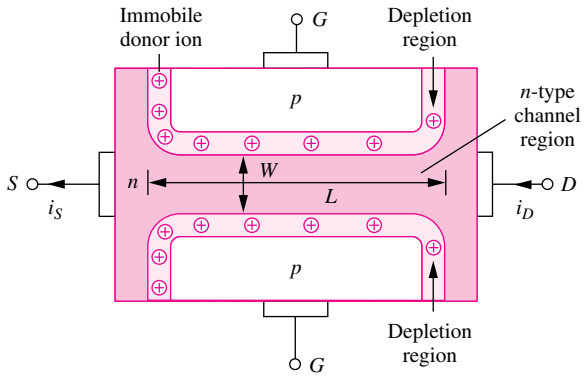

Figure 4.45 Basic n-channel JFET structure and important dimensions. (Note that for clarity the depletion layer in the p-type material is not indicated in the figure.)

When a voltage is applied between the drain and source, the channel resistance determines the current.

With no bias applied, as in Fig. 4.45, a resistive channel region exists connecting the drain and source. Application of a reverse bias to the gate-channel diodes will cause the depletion layers to widen, reducing the channel width and decreasing the current. Thus, the JFET is inherently a depletion-mode device — a voltage must be applied to the gate to turn the device off.

The JFET in Fig. 4.45 is drawn assuming one-sided step junctions ($N_A \gg N_D$) between the gate and channel in which the depletion layers extend only into the channel region of the device (see Sec. 3.1 and 3.6). Note how an understanding of the physics of the pn junction is used to create the JFET.

4.12.1 The JFET with Bias Applied

Figure 4.46(a) shows a JFET with 0 V on the drain and source and with the gate voltage $v_{GS} = 0$. The channel width is W. During normal operation, a reverse bias must be maintained across the pn junctions to provide isolation between the gate and channel. This reverse bias requires $v_{GS} \leq 0$ V.

In Fig. 4.46(b), v_{GS} has decreased to a negative value, and the depletion layers have increased in width. The width of the channel has now decreased, with $W' < W$, increasing the resistance of the channel region; see Eq. (4.89). Because the gate-source junction is reverse-biased, the gate current will equal the reverse saturation current of the pn junction, normally a very small value, and we will assume that $i_G \cong 0$.

For more negative values of v_{GS}, the channel width continues to decrease, increasing the resistance of the channel region. Finally, the condition in Fig. 4.46(c) is reached for $v_{GS} = V_P$, the pinch-off voltage; V_P is the (negative) value of gate-source voltage for which the conducting channel region completely disappears. The channel becomes pinched-off as the depletion regions from the two pn junctions merge at the center of the channel. At this point, the resistance of the channel region has become infinitely large. Further increases in v_{GS} do not substantially affect the internal appearance of the device in Fig. 4.47(c). However, v_{GS} must not exceed the reverse breakdown voltage of the gate-channel junction.

4.12.2 JFET Channel with Drain-Source Bias

Figures 4.47(a) to 4.47(c) show conditions in the JFET for increasing values of drain-source voltage v_{DS} and a fixed value of v_{GS}. For a small value of v_{DS}, as in Fig. 4.47(a), the resistive channel

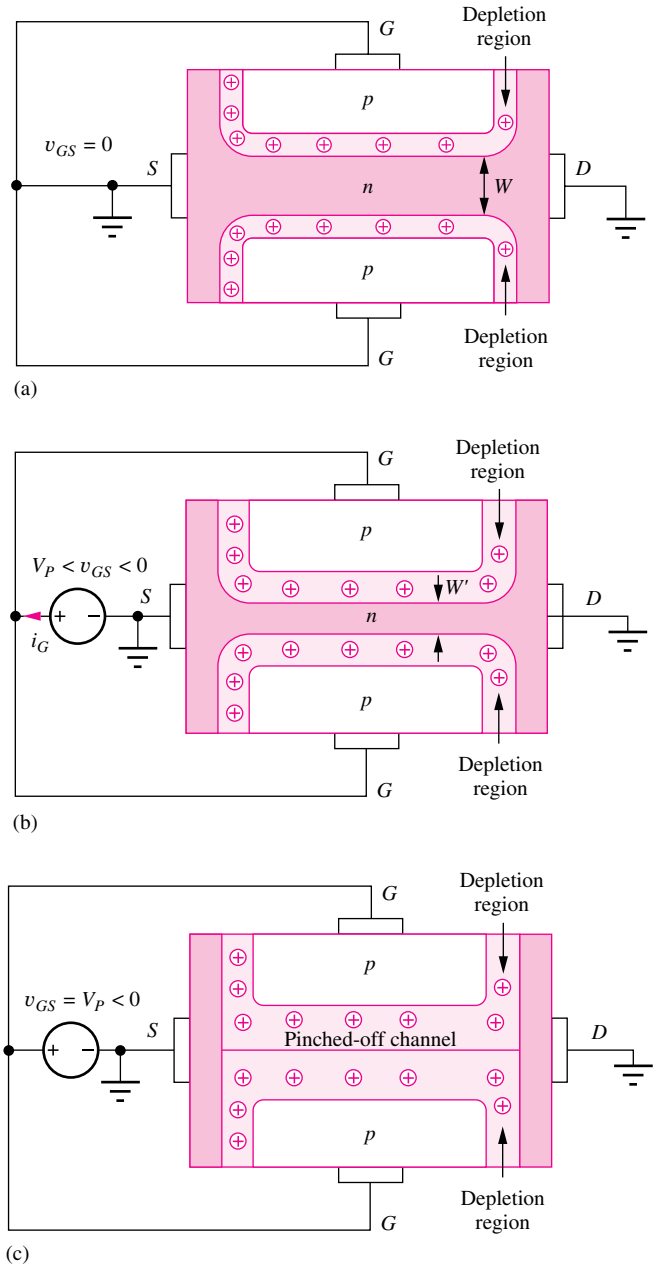

Figure 4.46 (a) JFET with zero gate-source bias. (b) JFET with negative gate-source voltage that is less negative than the pinch-off voltage V_P. Note $W' < W$. (c) JFET at pinch-off with $v_{GS} = V_P$.

connects the source and drain, the JFET is operating in its triode region, and the drain current will be dependent on the drain-source voltage v_{DS}. Assuming $i_G = 0$, the current entering the drain must exit from the source, as in the MOSFET. Note, however, that the reverse bias across the gate-channel junction is larger at the drain end of the channel than at the source end, and so the depletion layer is wider at the drain end of the device than at the source end. For increasing values of v_{DS}, the depletion layer at the drain becomes wider and wider until the channel pinches

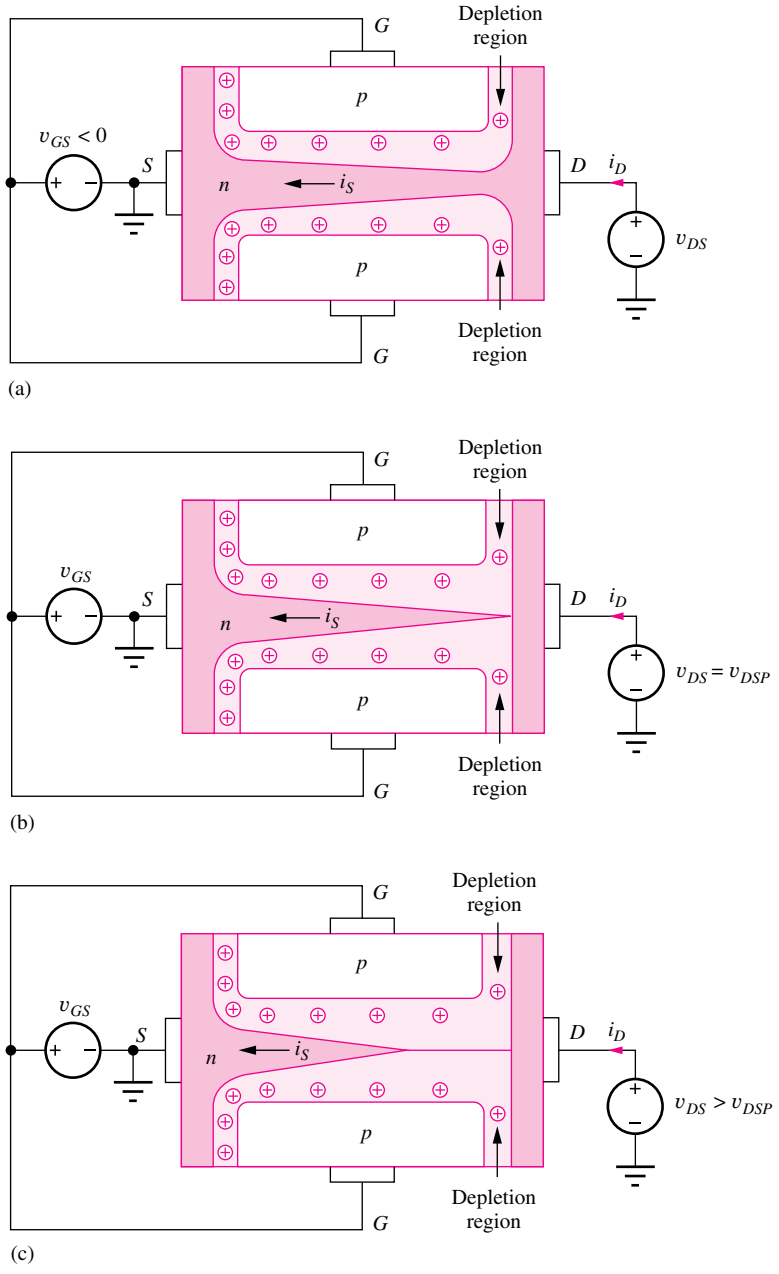

Figure 4.47 (a) JFET with small drain source. (b) JFET with channel just at pinch-off with $v_{DS} = v_{DSP}$. (c) JFET with v_{DS} greater than v_{DSP}.

off near the drain, as in Fig. 4.47(b). Pinch-off first occurs for

$$v_{GS} - v_{DSP} = V_P \qquad \text{or} \qquad v_{DSP} = v_{GS} - V_P \tag{4.90}$$

in which v_{DSP} is the value of drain voltage required to just pinch off the channel. Once the JFET channel pinches-off, the drain current saturates, just as for the MOSFET. Electrons are accelerated down the channel, injected into the depletion region, and swept on to the drain by the electric field.

Figure 4.47(c) shows the situation for an even larger value of v_{DS}. The pinch-off point moves toward the source, shortening the length of the resistive channel region. Thus, the JFET suffers from channel-length modulation in a manner similar to the MOSFET.

4.12.3 *n*-Channel JFET *i*-*v* Characteristics

Since the structure of the JFET is considerably different from the MOSFET, it is quite surprising that the i-v characteristics are virtually identical. We will rely on this similarity and not try to derive the JFET equations here. However, although mathematically equivalent, the equations for the JFET are usually written in a form slightly different from those of the MOSFET. We can develop this form starting with the saturation region expression for a MOSFET, in which the threshold voltage V_{TN} is replaced with the pinch-off voltage V_P:

$$i_D = \frac{K_n}{2}(v_{GS} - V_P)^2 \tag{4.91}$$

Factoring out $(-V_P)^2$ yields

$$i_D = \frac{K_n}{2}(-V_P)^2\left(1 - \frac{v_{GS}}{V_P}\right)^2 \qquad \text{or} \qquad i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 \tag{4.92}$$

in which the parameter I_{DSS} is defined by

$$I_{DSS} = \frac{K_n}{2}V_P^2 \qquad \text{or} \qquad K_n = \frac{2I_{DSS}}{V_P^2} \tag{4.93}$$

The pinch-off voltage V_P typically ranges from 0 to -25 V, and the value of I_{DSS} can range from 10 μA to more than 10 A.

If we include channel-length modulation, the expression for the drain current in pinch-off (saturation) becomes

$$I_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2(1 + \lambda v_{DS}) \qquad \text{for} \qquad v_{DS} \geq v_{GS} - V_P \geq 0 \tag{4.94}$$

The transfer characteristic for a JFET operating in pinch-off, based on Eq. (4.94), is shown in Fig. 4.48. I_{DSS} is the current in the JFET for $v_{GS} = 0$ and represents the maximum current in the device under normal operating conditions because the gate diode should be kept reverse-biased, with $v_{GS} \leq 0$.

The overall output characteristics for an n-channel JFET are reproduced in Fig. 4.49 with $\lambda = 0$. We see that the drain current decreases from a maximum of I_{DSS} toward zero as v_{GS} ranges from zero to the negative pinch-off voltage V_P.

The triode region of the device is also apparent in Fig. 4.49 for $v_{DS} \leq v_{GS} - V_P$. We can obtain an expression for the triode region of the JFET using the equation for the MOSFET triode region. Substituting for K_n and V_{TN} in Eq. (4.27) yields

$$i_D = \frac{2I_{DSS}}{V_P^2}\left(v_{GS} - V_P - \frac{v_{DS}}{2}\right)v_{DS} \quad \text{for } v_{GS} \geq V_P \qquad \text{and} \qquad v_{GS} - V_P \geq v_{DS} \geq 0 \tag{4.95}$$

Equations (4.94) and (4.95) represent our mathematical model for the n-channel JFET.

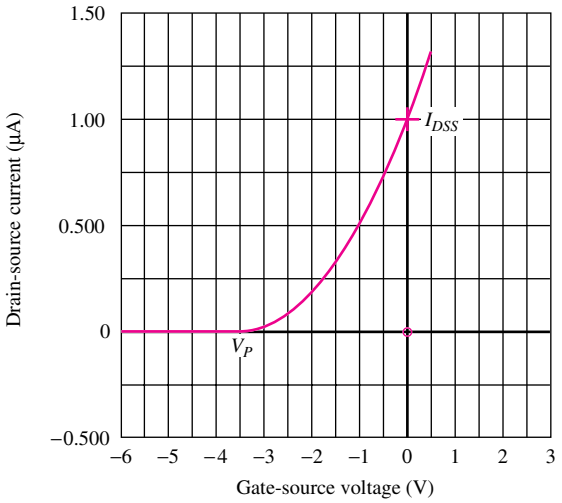

Figure 4.48 Transfer characteristic for a JFET operating in pinch-off with $I_{DSS} = 1$ mA and $V_P = -3.5$ V.

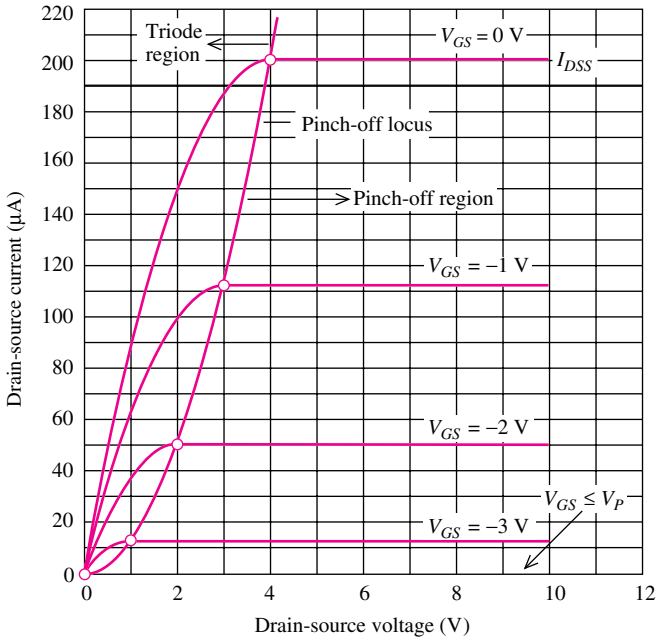

Figure 4.49 Output characteristics for a JFET with $I_{DSS} = 200$ μA and $V_P = -4$ V.

EXERCISE: (a) Calculate the current for the JFET in Fig. 4.48 for $V_{GS} = -2$ V and $V_{DS} = 3$ V. What is the minimum drain voltage required to pinch off the JFET? (b) Repeat for $V_{GS} = -1$ V and $V_{DS} = 6$ V. (c) Repeat for $V_{GS} = -2$ V and $V_{DS} = 0.5$ V.

ANSWERS: (a) 184 μA, 1.5 V; (b) 510 μA, 2.5 V; (c) 51.0 μA, 1.5 V

EXERCISE: (a) Calculate the current for the JFET in Fig. 4.49 for $V_{GS} = -2$ V and $V_{DS} = 0.5$ V. (b) Repeat for $V_{GS} = -1$ V and $V_{DS} = 6$ V.

ANSWERS: (a) 21.9 μA; (b) 113 μA

4.12.4 THE *p*-CHANNEL JFET

A ***p*-channel** version of the JFET can be fabricated by reversing the polarities of the n- and p-type regions in Fig. 4.45, as depicted in Fig. 4.50. As for the PMOSFET, the direction of current in the channel is opposite to that of the n-channel device, and the signs of the operating bias voltages will be reversed.

4.12.5 CIRCUIT SYMBOLS AND JFET MODEL SUMMARY

The circuit symbols and terminal voltages and currents for n-channel and p-channel JFETs are presented in Fig. 4.51. The arrow identifies the polarity of the gate-channel diode. The JFET structures in Figs. 4.45 and 4.50 are inherently symmetric, as were those of the MOSFET, and

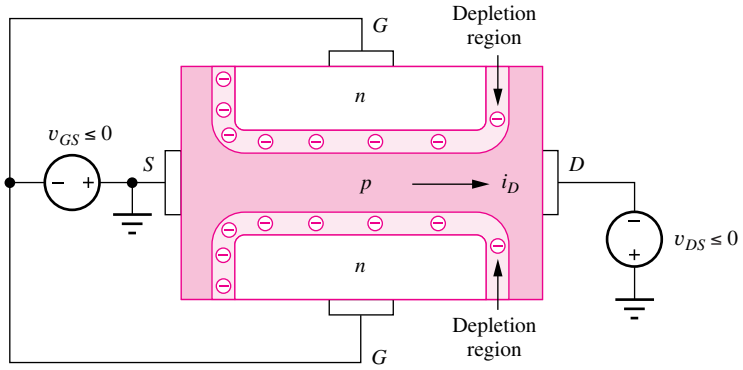

Figure 4.50 *p*-channel JFET with bias voltages.

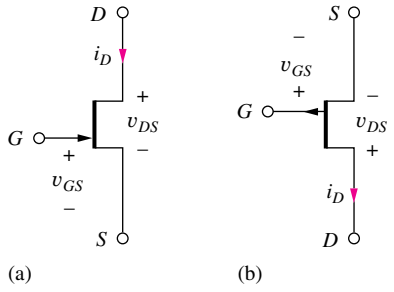

Figure 4.51 (a) *n*-channel and (b) *p*-channel JFET circuit symbols.

the source and drain are actually determined by the voltages in the circuit in which the JFET is used. However, the arrow that indicates the gate-channel junction is often offset to indicate the preferred source terminal of the device.

A summary of the mathematical models for the *n*-channel and *p*-channel JFETs follows. Because the JFET is a three-terminal device, the pinch-off voltage is independent of the terminal voltages.

n-CHANNEL JFET

For all regions:

$$i_G = 0 \quad \text{for} \quad v_{GS} \le 0 \tag{4.96}$$

Cutoff region:

$$i_D = 0 \quad \text{for} \quad v_{GS} \le V_P \quad (V_P < 0) \tag{4.97}$$

Triode region:

$$i_D = \frac{2I_{DSS}}{V_P^2}\left(v_{GS} - V_P - \frac{v_{DS}}{2}\right)v_{DS} \quad \text{for} \quad v_{GS} \ge V_P \quad \text{and} \quad v_{GS} - V_P \ge v_{DS} \ge 0 \tag{4.98}$$

Pinch-off region:

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 (1 + \lambda v_{DS}) \quad \text{for} \quad v_{DS} \ge v_{GS} - V_P \ge 0 \tag{4.99}$$

p-CHANNEL JFET

For all regions:

$$i_G = 0 \quad \text{for} \quad v_{GS} \ge 0 \tag{4.100}$$

Cutoff region:

$$i_D = 0 \quad \text{for} \quad v_{GS} \ge V_P \quad (V_P > 0) \tag{4.101}$$

Triode region:

$$i_D = \frac{2I_{DSS}}{V_P^2}\left(v_{GS} - V_P - \frac{v_{DS}}{2}\right)v_{DS} \quad \text{for} \quad v_{GS} \le V_P \quad \text{and} \quad |v_{GS} - V_P| \ge |v_{DS}| \ge 0 \tag{4.102}$$

Pinch-off region:

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 (1 + \lambda|v_{DS}|) \quad \text{for} \quad |v_{DS}| \ge |v_{GS} - V_P| \ge 0 \tag{4.103}$$

Overall, JFETs behave in a manner very similar to that of depletion-mode MOSFETs, and the JFET is biased in the same way as a depletion-mode MOSFET. In addition, most circuit designs must ensure that the gate-channel diode remains reverse-biased. This is not a concern for the MOSFET. In certain circumstances, however, forward bias of the JFET diode can actually be used to advantage. For instance, we know that a silicon diode can be forward-biased by up to 0.4 to 0.5 V without significant conduction. In other applications, the gate diode can be used as a built-in diode clamp, and in some oscillator circuits, forward conduction of the gate diode is used to help stabilize the amplitude of the oscillation. This effect is explored in more detail during the discussion of oscillator circuits in Chapter 18.

4.12.6 JFET Capacitances

The gate-source and gate-drain capacitances of the JFET are determined by the depletion-layer capacitances of the reverse-biased *pn* junctions forming the gate of the transistor and will exhibit a bias dependence similar to that described by Eq. (3.21) in Chapter 3.

Exercise: (a) Calculate the drain current for a *p*-channel JFET described by $I_{DSS} = 2.5$ mA and $V_P = 4$ V and operating with $V_{GS} = 3$ V and $V_{DS} = -3$ V. What is the minimum drain-source voltage required to pinch off the JFET? (b) Repeat for $V_{GS} = 1$ V and $V_{DS} = -6$ V. (c) Repeat for $V_{GS} = 2$ V and $V_{DS} = -0.5$ V.

Answers: (a) 156 μA, −1.00 V; (b) 1.41 mA, −3.00 V; (c) 273 μA, −2.00 V

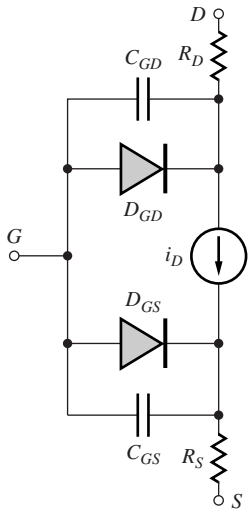

Figure 4.52 SPICE model for the *n*-channel JFET.

4.13 JFET Modeling in SPICE

The circuit representation for the basic JFET model that is implemented in SPICE is given in Fig. 4.52. As for the MOSFET, the JFET model contains a number of additional parameters in an attempt to accurately represent the real device characteristics. Small resistances R_S and R_D appear in series with the JFET source and drain terminals, diodes are included between the gate and internal source and drain terminals, and device capacitances are included in the model.

The model for i_D is an adaptation of the MOSFET model and uses some of the parameter names and formulas from the MOSFET as can be observed in Eq. (4.104).

$$\text{Triode region:} \quad i_D = 2 \cdot \text{BETA}\left(v_{GS} - \text{VTO} - \frac{v_{DS}}{2}\right) v_{DS}(1 + \text{LAMBDA} \cdot v_{DS}) \quad \text{for} \quad v_{GS} - \text{VTO} \ge v_{DS} \ge 0 \tag{4.104}$$

$$\text{Pinch-off region:} \quad i_D = \text{BETA}(v_{GS} - \text{VTO})^2(1 + \text{LAMBDA} \cdot v_{DS}) \quad \text{for} \quad v_{DS} \ge v_{GS} - \text{VTO} \ge 0$$

TABLE 4.5
SPICE JFET Parameter Equivalences

PARAMETER	OUR TEXT	SPICE	DEFAULT
Transconductance	—	BETA	100 μA/V^2
Zero-bias drain current	I_{DSS}	—	—
Pinch-off voltage	V_P	VTO	−2 V
Cannel length modulation	λ	LAMBDA	0
Zero-bias gate-drain capacitance	C_{GD}	CGD	0
Zero-bias gate-source capacitance	C_{GS}	CGS	0
Gate-bulk capacitance per unit width	C_{GBO}	CGBO	0
Ohmic drain resistance	—	RD	0
Ohmic source resistance	—	RS	0
Gate diode saturation current	I_S	IS	10 fA

The transconductance parameter BETA is related to the JFET parameters by

$$\text{BETA} = \frac{I_{DSS}}{V_P^2} \tag{4.105}$$

The SPICE description adds a channel-length modulation term to the triode region expression. An additional quirk is that the value of VTO is always specified as a positive number for both *n*- and *p*-channel JFETS. Table 4.5 contains the equivalences of the SPICE model parameters and our equations summarized at the end of the previous section. Typical and default values of the SPICE model parameters can also be found in Table 4.5. For more detail see [5].

EXERCISE: An *n*-channel JFET is described by $I_{DSS} = 2.5$ mA, $V_P = -2$ V, and $\lambda = 0.025$ V^{-1}. What are the values of BETA and VTO for this transistor?

ANSWERS: 625 μA; 2 V; 0.025 V^{-1}

EXERCISE: A *p*-channel JFET is described by $I_{DSS} = 5$ mA, $V_P = 2$ V, and $\lambda = 0.02$ V^{-1}. What are the values of BETA and VTO for this transistor?

ANSWERS: 1.25 mA; 2 V; 0.02 V^{-1}

4.14 BIASING THE JFET AND DEPLETION-MODE MOSFET

The basic bias circuit for an *n*-channel JFET or depletion-mode MOSFET appears in Fig. 4.53. Because depletion-mode transistors conduct for $v_{GS} = 0$, a separate gate bias voltage is not required, and the bias circuit requires one less resistor than the four-resistor bias circuit discussed earlier in this chapter. In the circuits in Fig. 4.53, the value of R_S will set the source and drain currents, and the sum of R_S and R_D will determine the drain-source voltage. R_G is used to provide a dc connection between the gate and ground while maintaining a high resistance path for ac signal voltages that may be applied to the gate (in amplifier applications, for example). In some cases, even R_G may be omitted.

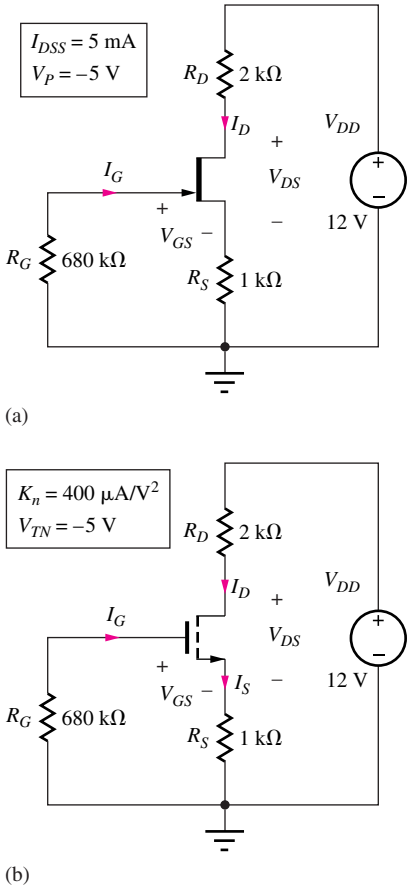

Figure 4.53 Bias circuits for (a) *n*-channel JFET and (b) depletion-mode MOSFET.

EXAMPLE 4.12 BIASING THE JFET AND DEPLETION-MODE MOSFET

Biasing of JFETs and depletion-mode MOSFETS is very similar, and this example presents a set of bias calculations for the two devices.

PROBLEM Find the quiescent operating point for the circuit in Fig. 4.53(a).

SOLUTION **Known Information and Given Data:** Circuit topology in Fig. 4.53(a) with $V_{DD} = 12$ V, $R_D = 2$ kΩ, $R_G = 680$ kΩ, $I_{DSS} = 5$ mA, and $V_P = -5$ V

Unknowns: V_{GS}, I_D, V_{DS}

Approach: Analyze the input loop to find V_{GS}. Use V_{GS} to find I_D, and I_D to determine V_{DS}.

Assumptions: The JFET is pinched-off, the gate-channel junction is reverse biased, and the reverse leakage current of the gate is negligible.

Analysis: Write the input loop equation including V_{GS}:

$$I_G R_G + V_{GS} + I_S R_S = 0 \qquad \text{or} \qquad V_{GS} = -I_D R_S \tag{4.106}$$

Equation (4.106) was simplified since $I_G = 0$ and $I_S = I_D$. By assuming the JFET is in the pinch-off region and using Eq. (4.92), Eq. (4.106) becomes

$$V_{GS} = -I_{DSS}R_S\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{4.107}$$

Substituting in the circuit and transistor values into Eq. (4.107) yields

$$V_{GS} = -(5 \times 10^{-3}\,\text{A})(1000\,\Omega)\left(1 - \frac{V_{GS}}{-5\,\text{V}}\right)^2 \quad \text{or} \quad V_{GS}^2 + 15V_{GS} + 25 = 0 \tag{4.108}$$

which has the roots -1.91 and -13.1 V. The second value is more negative than the pinch-off voltage of -5 V, so the transistor would be cutoff for this value of V_{GS}. Therefore $V_{GS} = -1.91$ V, and the drain and source currents are

$$I_D = I_S = \frac{1.91\,\text{V}}{1\,\text{k}\Omega} = 1.91\,\text{mA}$$

The drain-source voltage is found by writing the output loop equation:

$$V_{DD} = I_D R_D + V_{DS} + I_S R_S \tag{4.109}$$

which can be rearranged to yield

$$V_{DS} = V_{DD} - I_D(R_D + R_S) = 12 - (1.91\,\text{mA})(3\,\text{k}\Omega) = 6.27\,\text{V}$$

Check of Results: Our analysis yields

$$V_{GS} - V_P = -1.91\,\text{V} - (-5\,\text{V}) = +3.09\,\text{V} \quad \text{and} \quad V_{DS} = 6.27\,\text{V}$$

Because V_{DS} exceeds $(V_{GS} - V_P)$, the device is pinched off. In addition, the gate-source junction is reverse biased by 1.91 V. So, the JFET Q-point is (1.91 mA, 6.27 V).

Discussion: Because depletion-mode transistors conduct for $v_{GS} = 0$, a separate gate bias voltage is not required, and the bias circuit requires one less resistor than the four-resistor bias circuit discussed earlier in this chapter. The circuitry for biasing depletion-mode MOSFETs is identical as indicated in Fig. 4.53(b) — see the exercises after this example.

Computer-Aided Analysis: SPICE analysis yields the same Q-point as our hand calculations. If we add $\lambda = 0.02\ \text{V}^{-1}$, the Q-point shifts to (2.10 mA, 5.98 V). It is helpful to add a voltmeter to the circuit to directly measure V_{DS}.

EXERCISE: What are the values of VTO, BETA, and LAMBDA used in the simulation in the last example?

ANSWERS: -5 V; 0.2 mA; 0.02 V^{-1}

EXERCISE: Show that the expression for the gate-source voltage of the MOSFET in Fig. 4.53(b) is identical to Eq. (4.108). Find the Q-point for the MOSFET and show that it is the same as that for the JFET.

EXERCISE: What is the Q-point for the JFET in Fig. 4.53(a) if $V_{DD} = 9$ V?

ANSWER: (1.91 mA, 3.27 V)

EXERCISE: Find the Q-point in the circuit in Fig. 4.53(a) if R_S is changed to 2 kΩ.

ANSWER: (1.25 mA, 4.00 V)

EXERCISE: (a) Suppose the gate diode of the JFET in Fig. 4.53(a) has a reverse saturation current of 10 nA. Since the diode is reverse biased, $I_G = -10$ nA. What is the voltage at the gate terminal of the transistor? [See Eq. (4.106)]. What is the new value of V_{GS}? What will be the new Q-point of the JFET? (b) Repeat if the saturation current is 1 μA.

ANSWERS: (a) +6.80 mV, −1.91 V, (1.91 mA, 6.27 V); (b) 0.680 V, −1.64 V, (2.26 mA, 5.22 V)

SUMMARY

- This chapter discussed the structures and i-v characteristics of two types of field-effect transistors (FETs): the metal-oxide-semiconductor FET, or MOSFET, and the junction FET, or JFET.
- At the heart of the MOSFET is the MOS capacitor, formed by a metallic gate electrode insulated from the semiconductor by an insulating oxide layer. The potential on the gate controls the carrier concentration in the semiconductor region directly beneath the gate; three regions of operation of the MOS capacitor were identified: accumulation, depletion, and inversion.
- A MOSFET is formed when two pn junctions are added to the semiconductor region of the MOS capacitor. The junctions act as the source and drain terminals of the MOS transistor and provide a ready supply of carriers for the channel region of the MOSFET. The source and drain junctions must be kept reverse-biased at all times in order to isolate the channel from the substrate.
- MOS transistors can be fabricated with either n- or p-type channel regions and are referred to as NMOS or PMOS transistors, respectively. In addition, MOSFETs can be fabricated as either enhancement-mode or depletion-mode devices.
- For an enhancement-mode device, a gate-source voltage exceeding the threshold voltage must be applied to the transistor to establish a conducting channel between source and drain.
- In the depletion-mode device, a channel is built into the device during its fabrication, and a voltage must be applied to the transistor's gate to quench conduction.
- The JFET uses pn junctions to control the resistance of the conducting channel region. The gate-source voltage modulates the width of the depletion layers surrounding the gate-channel junctions and thereby changes the width of the channel region. A JFET can be fabricated with either n- or p-type channel regions, but because of its structure, the JFET is inherently a depletion-mode device.
- Both the MOSFET and JFET are symmetrical devices. The source and drain terminals of the device are actually determined by the voltages applied to the terminals. For a given geometry and set of voltages, the n-channel transistor will conduct two to three times the current of the p-channel device because of the difference between the electron and hole mobilities in the channel.
- Although structurally different, the i-v characteristics of MOSFETs and JFETs are very similar, and each type of FET has three regions of operation.
  - In cutoff, a channel does not exist, and the terminal currents are zero.