Microelectronic Systems Reliability

An IEEE/HKN/SWE sponsored seminar

2–5 pm Friday, January 18, Room NH 227
(also part of the ECE 507 seminar course)

(1) Reliability issues in complex microelectronic assemblies: methodological approaches - Dr Helene Fremont, University of Bordeaux, France

The reliability of embedded electronic systems is a major concern among manufacturers of aircraft and automotive systems and of systems for military or medical applications.

The predictive study of reliability of microelectronic assemblies is based on the joint use of accelerated aging tests, of experimental surveys, of computational tools which implement the analytical models and of numerical simulations by finite elements. Assessing the reliability of these assemblies passes in recent years by a comprehensive approach of reliability. The approach includes descriptions of and links to environmental constraints. It also includes knowledge of physical laws governing the failure mechanisms and interpretation of results obtained from these data (process called "PoF" Physics of Failure).

New materials, like high-k gate dielectrics, Cu and low-k materials, new device architectures such as multiple gate FETs, new technologies such as micro-electromechanical systems (MEMS), and new packaging technologies are introduced. For these new materials, devices and technologies the failure mechanisms are still not well understood and their speed of introduction exceeds the capability to explore their reliability.

The purpose of the lecture is to give key definitions, and an introduction to key methods and to key tools to assess the reliability of microelectronic devices of today and tomorrow.

(2) Thermal-Electrical-Mechanical Simulations Concerning Reliability in 3-D Integration – Dr Kirsten Wiede-Zaage, Leibniz University of Hanover, Germany

Thermal-Electrical-Mechanical Simulations Concerning Reliability in 3-D Integration
Next package generations have to offer a rising amount of solder contacts or they are exposed to extreme operation conditions. Cracking as a consequence of coefficient of thermal expansion (CTE) mismatch is one well known risk concerning the reliability of solder joints. Modern 3D-Packaging leads to an increased number of ICs on the same amount of space, due to this the contact density increases and the diameter of the solder joints decrease. CoC as one possibility for 3D integration can be used for the vertical assemble of ICs. CoC structures base on a direct connection of ICs on chip level with through silicon vias (TSVs) and micro bump arrays (µBGAs) with new reliability aspects. The placement of the TSV in the circuit design is one of the aspects to be looked on. The shrinking dimensions of solder joints and the rising operation temperatures cause new risks to the reliability of solder joints. Two new phenomena are void formation and accelerated inter metallic compound (IMC) growth due to electromigration (EM). During the development of a reliable micro electronic system, migration induced reliability issues have to be considered on chip and package level. The simulations enable a more detailed interpretation of the stress test results. Simulation results of PoP and Flip-Chip also µ-BGA and TSV structures at different operation condition were investigated. The EM performance of future solder joints and copper traces in PoP, µBGA and TSV is determined.

(3) Virtual Prototyping for Power Electronics Module Design – Current Status and Future Challenges – Prof Chris Bailey, University of Greenwich, UK

Power Electronics is the application of solid-state electronics for the efficient control and conversion of electrical power. Whereas microelectronics is used to carry communications of data, with Power Electronics it is power that is handled and controlled. Power Electronics covers various disciplines, especially semiconductor, circuit design, thermal design, electromagnetics, digital electronics, control theory, and materials science in the context of packaging and reliability engineering. It also covers a wide range of power (mW to MW), temperature (-55C to 275C), frequencies (DC to GHz) and dimensions (um to km). When designing a new power electronics module the design engineer must ensure that cost, efficiency, size/weight and reliability meet customer expectations. In addition EMC/EMI, cooling, mechanics and manufacturability must be considered. These objectives will be particularly important to meet future power electronics module designs in terms of maximising the performance of the semiconductor technology and designing Integrated Power Electronics Modules (IPEM) where power semiconductors are integrated with digital control, passives and sensors in the same module. This presentation will detail the current status of virtual prototyping for power electronics modules which includes design for electromagnetic compatability, themal management, and reliability. Focus will be on IGBT modules ; future challenges will also be dicussed in terms of integrated design and prognostics and health management.

Speaker Biographies

Hélène Frémont is Associate Professor at University of Bordeaux 1 in France. Her research expertise is microelectronics reliability and failure analysis. She is currently leading the PACE (Packaging, Assembly and Electromagnetic Compatibility) team of the IMS laboratory (Integration from the Material to the System) of the University of Bordeaux. She is member of the technical committee of different CPMT-IEEE conferences and of the organizing committee of the European Symposium on Reliability of Electron Devices, Failure Physics and Analysis ESREF. She co-authored more than 120 scientific articles, including journal and conference publications, book chapters and invited papers.

Kirsten Weide-Zaage studied Physics with main topic Biophysics and received her Diploma in 1988. In 1994 she received her PhD in Electrical Engineering, and 2011 the venia legendi in micro electronics at the Leibniz Universität in Hannover Germany. She is working since 1991 at the Information Technology Laboratory as researcher and leader of the simulation group 'robust electronics' in the field interconnect and package reliability.

Chris Bailey is Professor of Computational Mechanics and Reliability, and Director of the Computational Mechanics and Reliability Group at the University of Greenwich. He is a member of the NAFEMS Multi-Physics Modelling working group, represents Europe on the Board of Governors of IEEE-CPMT, is a member of the INEMI Roadmap team, Chair of the UK&RI IEEE CPMT/Reliability chapter, and an associate editor of the IEEE CPMT Transactions. Chris is a member of a number of IEEE conference committees which includes EuroSime, ESTC and EPTC. Key industrial links include Mentor Graphics, Selex-Galileo, GE-Aviation - Newmarket, Dynex Semiconductors, Semelab, Rolls Royce, Henkel, EADS, SSE, and MBDA. He has published over 200 papers in the field of modeling and simulation of micro-technology based processes and products.

Reliability simulations and experimental determinations are key elements of any electronic system's development process. The three 40-min talks to be presented here by three distinguished European researchers in the field will explore different facets of reliability studies at an appropriate level for undergraduate and graduate ECE students alike, and will introduce the core concepts and terminologies.