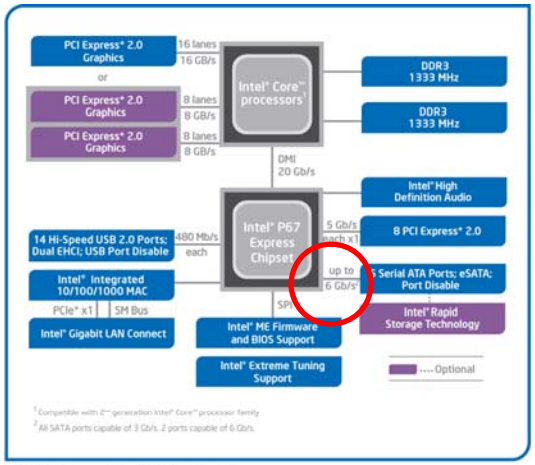
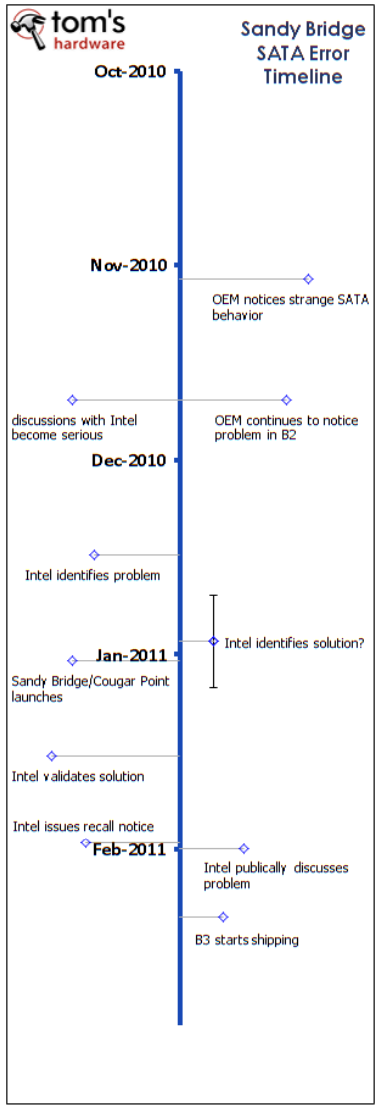
Sandy Bridge Recall



Intel® P67 Express Chipset Platform Block Diagram



- OEMs notice degradation in 3 Gb/s SATA port of Cougar Point (Sandy Bridge chipset)
  - Failure rate 5-15%/3y
- Causes:
  - Physical: Low-voltage xistor connected to high-voltage supply
  - Management: Risk Assessment Hole
- Cost to Intel: $1B

Risk Assessment Post Mortem

- Risk Assessment
  - Design Rule Check (SS required = 0)
    - Many exceptions manually invalidated.
    - How are they reviewed?
  - Si Validation (SS required = 1)
    - High-traffic I/O at accelerated stress not in validation suite.
    - How are Use Models determined, and reviewed?
- Learnings
  - This was caused by a failure in pre-Si Risk Assessment.
  - Use Model was incomplete.
  - Sample size had little to do with it.

Glenn's opinions.