SINGLE-LOOP CONTROL FOR PWM CONVERTERS

Single-Loop Controlled Switching Regulator

Feedback Control to Achieve:

- Accuracy
- Speed
- Stability
DC Analysis of Switching Regulators

Small-Signal Analysis of Switching Regulators

- DC PWM Gain: \( \frac{D}{V_c} = \frac{1}{V_p} \)
Small-Signal Analysis of Switching Regulators

Small-signal Block diagram

where

\[ G_v = \left. \frac{\hat{V}_o}{\hat{V}_i} \right|_{d=0} \]  \quad \text{open-loop voltage susceptibility}

\[ Z_p = \left. \frac{\hat{V}_o}{\hat{I}_o} \right|_{d=0} \]  \quad \text{open-loop output impedance}

\[ G_d = \left. \frac{\hat{I}_d}{\delta d} \right|_{\hat{V}_i = \hat{I}_o = 0} \]  \quad \text{control to output transfer fn.}

\[ A(s) = \frac{\hat{V}_o}{\hat{I}_o} \]  \quad \text{Compensator gain}

\[ FM = \frac{\hat{V}_o}{\hat{I}_o} \]  \quad \text{PWM gain}

Small-signal PWM gain, FM

\[ V_o \quad \delta t \]

\[ \hat{V}_o = V_o - \hat{V}_c \]

\[ \hat{I}_o = \frac{\hat{V}_o}{V_p} \quad \text{\( s \)-domain} \]

\[ \hat{V}_c = \hat{V}_o \]

\[ \hat{I}_c = \hat{I}_o \]

\[ \hat{V}_o = \frac{\hat{V}_c}{\hat{I}_c} \]  \quad \text{PWM to output transfer fn.}
Closed-Loop Transfer Functions

• Closed-loop audio-susceptibility, $\frac{\hat{V}_s}{V_s}$
  $$\hat{V}_s = G_v \cdot \hat{V}_o + G_d \cdot \hat{d} \quad — (1)$$
  $$\hat{d} = -A \cdot F.M. \cdot \hat{V}_o \quad — (2)$$

  Eliminate $\hat{d}$ from (1) + (2)

  $$\Rightarrow \frac{\hat{V}_s}{V_s} = \frac{G_v}{1 + G_d \cdot F.M. \cdot A} = \frac{G_v}{1 + T}$$

  Where $T = G_d \cdot F.M. \cdot A$ is Loop gain

• Closed-loop output impedance, $\frac{\hat{V}_o}{I_o}$
  $$\hat{V}_o = Z_p \cdot I_o + G_d \cdot \hat{d} \quad — (3)$$

  From (3) + (2)

  $$\frac{\hat{V}_s}{V_s} = \frac{Z_p}{1 + T}$$

Loop Gain Analysis

Provides:

• System performance analysis
• Stability analysis
  • absolute stability
  • degree of stability
• Design insight
• Measurement verification
Desired Loop Gain Characteristics

The graph shows the desired loop gain characteristics with high gain at low frequency and a -20dB/dec slope. The wide bandwidth is indicated, and the phase margin \( \phi_M \) is labeled.

Stability Margins

The Nyquist stability criterion is illustrated, showing the relationship between \( G_M \) and the phase margin \( \phi_M \). The graph indicates the frequency response with the phase margin and gain margins clearly marked.
Compensation:

- Pole at Origin.
- Double Zero at $f_0$.
- Pole at ESR Zero.

- Zero at Origin ($R_f = 0$).
- Double Pole at $f_0$.
- Zero due to Capacitor ESR.
AUDIO SUSCEPTIBILITY ASYMPTOTES

- DC Gain Determined by Steady-State Duty Cycle.
- Double Pole at $f_0$.
- Zero due to Capacitor ESR.

Function of the Loop Gain, $T$

Example: Closed-loop audio-susceptibility

$$\frac{\hat{V}_o}{\hat{V}_g} |_{CL} = \frac{G_{TV}}{1 + T} \triangleq G_{CL}$$
Function of the Loop Gain, $T$

**Closed-Loop Output Impedance**

$G_d = \frac{G_m}{1 + \frac{s}{\omega_n} + \frac{s^2}{\omega_n^2}}$

$G_m = \frac{V_o}{D}$, $\omega_n = \frac{1}{\sqrt{LC}}$

$Q = R\sqrt{\frac{L}{C}}$

- Suppose $A(s) = K$; constant gain
- Not enough low freq. gain

$\phi_H = 0 \Rightarrow$ oscillation

$\Rightarrow$ Need an integrator for high gain at low freq.
Compensator, $A(s)$ Design Considerations

- to Shape the Loop Gain, $T = G_d \cdot FM \cdot A(s)$

- Suppose $A(s) = \frac{u_m}{S}$; integrator

\[ T = \frac{u_m}{S} \cdot \frac{1}{1 + \frac{s}{\omega_m} + \frac{s^2}{\omega_m^2}} \]

\[ \omega_m = \omega_c \cdot G_m \cdot FM \]

\[ |T| \]

\[ -20 \text{ dB/dec} \]

\[ -60 \text{ dB/dec} \]

\[ -90^\circ \]

\[ -270^\circ \]

\[ \Rightarrow \text{Excessive phase lag at the loop gain crossover, } \omega_c \]

\[ \text{due to the integrator } \left(-90^\circ\right) \text{ and complex pole pair } \left(-180^\circ\right) \text{ need to be compensated by introducing two zeroes before } \omega_c \]

Compensator Characteristics

- An integrator for high dc gain
- Two zeroes below the loop gain crossover frequency, $f_c$ to compensate the excessive phase lag due to the integrator and the power stage complex pole pair.
- Two high frequency poles
  - to attenuate high frequency noise
  - to ensure the magnitude of the loop gain keeps decreasing after the 0 dB crossover
- *Phase lag due to the two poles at the loop gain crossover should be minimum
Compensator Circuit

\[
\frac{\dot{v}_e}{v_0} = -\frac{z_f}{z_i} \quad z_i = R_i \parallel (\frac{1}{sC_1} + R_3)
\]

\[
z_f = \frac{1}{sC_3} \parallel (\frac{1}{sC_2} + R_3)
\]

\[
= -\frac{w_z (1 + \frac{w_z}{w_{z1}})(1 + \frac{w_z}{w_{z2}})}{s (1 + \frac{w_p}{w_{p1}})(1 + \frac{w_p}{w_{p2}})}
\]

where

\[
w_z = \frac{1}{R_1(C_1 + R_2)}
\]

\[
w_{z1} = \frac{1}{R_3C_1} \quad w_{z2} = \frac{1}{C_2(R_1 + R_3)}
\]

\[
w_{p1} = \frac{1}{R_3C_2} \quad w_{p2} = \frac{1}{R_2S + G}
\]

For \( C_1 \gg C_3 \), \( R_1 \gg R_3 \)

\[
u_i = \frac{1}{R_1C_1}
\]

\[
u_{z1} = \frac{1}{R_3C_1} \quad u_{z2} = \frac{1}{R_1C_2}
\]

\[
u_{p1} = \frac{1}{R_3C_2} \quad u_{p2} = \frac{1}{R_2S + G}
\]
Buck Regulator Design

\[ T = G_d \cdot FM \cdot A(s) \]

\[ G_d \equiv \frac{\dot{V}_d}{V_d} = V_d \cdot \frac{1 + \frac{\omega_d}{\omega_0}}{1 + \frac{s}{\omega_0} + \frac{s^2}{\omega_0^2}} \]

\[ \omega_d = \frac{i}{R_c C} \]

\[ \omega_s = \frac{i}{\sqrt{LC}}, \quad Q = R\sqrt{\frac{L}{C}} \]

\[ G_{sv} \equiv \frac{\dot{V}_s}{V_s} = 0 \cdot \frac{1 + \frac{\omega_s}{\omega_0}}{1 + \frac{s}{\omega_0} + \frac{s^2}{\omega_0^2}} \]

\[ Z_p \equiv \frac{\dot{I}_d}{i_d} = R_d \parallel R \cdot \frac{(1 + \frac{\omega_d}{\omega_0})(1 + \frac{\omega_s}{\omega_0})}{1 + \frac{s}{\omega_0} + \frac{s^2}{\omega_0^2}} \]

\[ \omega_{d1} = \frac{R_d}{L} \]

Loop Gain Design Procedure

\[ T = \frac{w_m}{s} \frac{(1 + \frac{s}{\omega_{d1}})(1 + \frac{s}{\omega_{d2}})}{\left((1 + \frac{s}{\omega_0})(1 + \frac{s}{\omega_m})\right)^2(1 + \frac{s}{\omega_{d2}} + \frac{s^2}{\omega_0^2})} \]

where \[ w_m = \frac{V_m}{FM \cdot w_2} \]

The objective is to design a compensator, \( \omega_0, \omega_{d1}, \omega_{d2}, \omega_m \), and \( \omega_m \), to shape the loop gain, \( T \) for stability and optimum performance for given power stage parameters, \( \omega_0, \omega_m, Q \) and \( V_m \) and the PWM gain, \( FM \).
Design Steps

1. Set the loop gain crossover frequency, $f_c$, for given switching frequency, $f_s$.
   i.e., $f_c = f_s/6$

2. Cancel the ESR zero, $f_{z0}$, by a compensator pole, $f_{p1}$, (i.e., $f_{z0} = f_{p1}$)

3. Place a high frequency compensator pole, $f_{p2}$, to get the maximum attenuation of the switching ripple and high frequency noise with the minimum phase lag at $f_c$.

4. Place the two compensator zeroes, $f_{z1}$ and $f_{z2}$, below $f_c$.
   Place $f_{z1}$ below the power stage resonant frequency, $f_r$, to avoid a conditional instability.
   Design $f_{z1}$ and $f_{z2}$ considering the trade-off between the regulator performance and the stability margin.

5. The integrator gain, $f_i$, is determined after the step 4.

6. Select the compensator parameters (R's and C's)
Design of \( f_{c1} \) and \( f_{c2} \) - Case 2

\[ T \]
\[ o < d \beta \]
\[ \theta \]

Design of \( f_{c1} \) and \( f_{c2} \) - Case 3

\[ T \]
\[ o < d \beta \]

SINGLE LOOP CONTROL FOR PWM CONVERTERS

\[ 25: \]

\[ 26: \]
Settling Time for the Step Input / Load Transient

Closed-loop transfer function

\[ G_{CL} = \frac{G_0}{1 + T} \]

\[ \approx \frac{G_0}{T} \quad \text{at low frequency} \quad (1T \gg 1) \]

\[ G_o = \frac{F_i(s)}{G(s)} \]

\[ T = \frac{(1 + \%w_n) \cdot \omega_m}{G(s) s} \]

\[ \frac{(1 + \%w_{n1})(1 + \%w_{n2})}{(1 + \%w_{m1})(1 + \%w_{m2})} \]

\[ G_{CL} = \frac{\%w_m \cdot F_i(s) \cdot (1 + \%w_{m1})(1 + \%w_{m2})}{(1 + \%w_{n1})(1 + \%w_{n2})(1 + \%w_{n3})} \]

\[ \text{ESR zero} \]

The lower frequency compensator zero, \( f_1 \), determines the settling time.

Design Trade-Off for \( f_1 \) and \( f_2 \)

<table>
<thead>
<tr>
<th>freq.</th>
<th>closed-loop peak</th>
<th>settling time</th>
<th>stability margin</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_1 )</td>
<td>↑</td>
<td>↓</td>
<td>faster</td>
</tr>
<tr>
<td>↓</td>
<td>↑</td>
<td>slower</td>
<td>↑</td>
</tr>
<tr>
<td>( f_2 )</td>
<td>↓</td>
<td>↑</td>
<td>↓</td>
</tr>
</tbody>
</table>
Flyback Regulator Design

\[ G_d \triangleq \frac{\hat{v}_d}{\hat{i}_d} = \frac{N_s}{N_p} \cdot \frac{v_s}{v_i} \cdot \frac{(1 - \frac{1}{\omega_c}) (1 + \frac{1}{\omega_c})}{1 + \frac{\omega_s}{\omega_c} + \frac{s}{\omega_c}} \]

\[ \omega_o \triangleq \frac{D'}{\sqrt{L C}} \quad Q = D' R \sqrt{\frac{C}{L}} \]

\[ \omega_a = \frac{D'^2 R}{D L} \quad \omega_b = \frac{1}{R_c C} \]

\[ G_v \triangleq \frac{\hat{v}_v}{\hat{v}_2} = \frac{D \cdot \omega_a}{D' \cdot \omega_b} \cdot \frac{1 + \frac{1}{\omega_b}}{1} \]

\[ \tilde{z}_p \triangleq \frac{\hat{v}_z}{\sqrt{L}} = (\frac{v_z}{V}) R \cdot \frac{(1 + \frac{1}{\omega_c}) (1 + \frac{1}{\omega_c})}{1} \]

\[ \omega_c = \frac{v_z}{L} \]

Loop Gain Design

- Due to the RHP zero, \( f_c \), the loop gain crossover frequency, \( f_c \), must be designed well below the RHP zero. I.e., \( f_c = f_c / 10 \)

- The two poles in the compensator should cancel both ESR zero, \( f_c \), and RHP zero, \( f_c \).

- Design of the two zeroes are the same as in the buck regulator case.