Introduction to theory, strategy, and methods of simulation-based functional pre-silicon validation of digital integrated circuits. Topics include complete validation flow, validation environment, stimulus, checking, and coverage. Familiarity with computer architecture and hardware description languages required. A design project is an integral part of this course.

Students will gain experience using simulation techniques used to validate modern digital designs using System Verilog to construct test benches. The course material complements other ECE pre-silicon and post-silicon functional validation courses.

Prerequisites: An upper-division undergraduate computer architecture (e.g. ECE 371) and Verilog HDL class (e.g. ECE 351) or permission of instructor. ECE 571 System Verilog recommended.

Course Coordinator/Instructor: Tom Schubert
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D2L website active: Lecture notes, papers, homework assignments and dropbox, announcements, etc

Required Texts and/or Required Reading List
- Comprehensive Functional Verification - The Complete Industry Cycle, Wile & Goss & Roesner
- Mentor Graphics simulation tool documentation

Outline of Course Content
- Introduction to Functional Verification
  - Verification in the Chip Design Process
  - Goals, challenge, costs, verification cycle
- Verification Flow
  - Design hierarchy, levels of verification, strategy
- Simulation Based Verification
  - Constraints, checking, and coverage
  - Basic Verification Environment, test bench design, observability, assertion based verification, testing strategies
- Verification Plan
  - Functional specification, plan contents, plan evolution
- HDLs and Simulation Engines
  - Event-driven and cycle based simulation, improving throughput
- Creating Environments
  - Test Bench writing
- Verification Coverage
  - functional vs manufacturing test coverage
  - structural and functional coverage
  - coverage data collection and analysis
- Stimulus generation strategies
- Results checking strategies
  - debug methodology
- Pervasive Function Verification
  - System Reset and Bring-Up, Error and Degraded Mode Handling. Verifying Hardware Debug Assists, Low Power Mode Verification
- Re-use Strategies
  - Beyond General-Purpose Logic Simulation
- Completing the Verification Cycle
  - Regression, Problem Tracking, Tape-Out Readiness, Escape Analysis
- Advanced Verification Techniques
  - Save Verification Cycles, High-Level Modeling, Coverage-Directed Generation
  - FPGA based emulation vs. commercial emulator based emulation

**Student Learning Outcomes**

1. Knowledge of validation theory, simulation tools, and application to modern digital design.
2. Knowledge of verification methodologies used in industry.
3. Able to describe simulation-based verification methodology tradeoffs.
4. Able to develop a strategy to verify a complex VLSI design.
5. Able to develop verification components used in a pre-silicon environment.
6. Recognize
   - The central role of validation in modern digital design
   - The need for a structured, measured process to achieve objectives
   - The importance of continuous improvement and team collaboration

**Course requirements**

- Midterm (20%), Final (25%), Project (30%), Homework (25%)

There will be approximately 4 homework assignments. To pass the course, each assignment must be turned in on or before its due date. Some assignments may be done in groups. If you choose to work in a group, please turn in only one solution, indicating the names of all group members. Of course, individually, you will be expected to understand the material and demonstrate so on exams.

Some of the solutions might be obtained from previous classes. Using such solutions is **very** counterproductive! To pass exams, you'll need to develop analysis skills by working through problems. More importantly, working through the problems yourself, discussing in groups, or with the TA or me is the best way to learn the material. I strongly encourage you to come to my office hours after struggling and we'll work out the correct answer together.

**Project:** The project is an important educational complement to the material presented in lectures. A good project will encounter problems that will require some research to find a solution. We'll discuss the project in more detail in a few weeks, but you should soon start thinking about possible projects. To complete the project, the first step is to identify a design. The design needs to be sufficiently complicated to require significant testing such that you can insert a subtle error in the design that might be difficult to catch. You are welcome to create a new design from scratch, though I recommend students start with a pre-existing Verilog design. I also encourage students to work in groups of 2 people. Students are expected to orally present their projects as well as turn in a written report.

**ECE 510 paper requirement:** For graduate students, there is an additional requirement to write a paper critiquing 3-4 technical papers (roughly 1 page per paper). I will provide some suggestions, but students are also welcome to propose other papers as well.
**Professionalism:**
In our worldwide discipline, we must work with many men and women from different cultures, races, sexual preferences, religions, political affiliations, etc. To pass this course, each student must demonstrate they are a good team player. Students are expected to work/learn in a harassment free environment with the highest professional standards.

**Academic Honesty:** I enjoy teaching very much and consider students to be future colleagues. Thus plagiarism is an extremely depressing thing for me to encounter and will be taken very seriously. Plagiarism is definitely not just a harmless prank. It can have very serious effects, harmful to your standing at the university, and also possibly very harmful to your job prospects when you seek employment after graduation. The penalty for plagiarism is an F in the course and a letter describing the incident sent to the Vice Provost for Student Affairs. Please avoid any actions during an exam (e.g. talking, looking around, etc.) which might make the exam proctors doubt your honesty.

Please also view PSU’s Student Code of Conduct at [http://www.pdx.edu/dos/codeofconduct](http://www.pdx.edu/dos/codeofconduct)

**Doing Well:** Lectures cannot cover all aspects of the material. Much of the detail will be learned through exercises or supplied by consulting the book and other online material. Ask me about anything that you don’t understand, no matter how minor it seems. I recommend actively attending lectures. This is not a video/distance learning class. Though the class is recorded, it is automated and isn’t a perfect system---sometimes there are audio problems or a lecture cannot be posted at all. You are responsible for learning the lecture material regardless. Most lectures will be interactive or include interactive small group discussions that are not well captured by recordings. Finally, note that grading is non-competitive, so it is possible for everyone to do well.