Lab Project #2

3 State FSM using One-Hot Encoding
Objective

Design the following 3 state FSM (Moore machine) using One-Hot encoding.
References

- Digital Design Principles And Practices, 3e, John F. Wakerly (Text book used in the class)
- Digital Design, 4e, Morris Mano & M. D. Ciletti
Background

- Moore state machine:
  \[ \text{Outputs} = f(\text{Present State}) \]

- Mealy machine:
  \[ \text{Outputs} = f(\text{Present State, Inputs}) \]
Moore State Machine

Inputs → Next State Combi. Logic

Next State

Present State Register

Preset state

Output Combi. Logic

Moore Outputs
Clock Generator

Build the clock generator using a D Flip flop and DIP switches

(1) To get a high at Q: Connect C and A
(2) To get a low at Q: Connect C and B
Materials

- D flip flops
- Logic function IC’s (inverter, NAND or OR)
- LED’s
- DIP switch
- Resistors
Requirements

- Build the circuit on the breadboard
- Test the state machine for the following sequence of inputs (Assume C is the initial state)
  
  1 1 0 0 1 0

- Set the inputs before every clock pulse.
- Demonstrate the correct state transitions.
Guidelines to build the circuit

- Implement reset using a DIP switch and voltage divider circuit
- LED’s should be connected in series with a resistor
- Place the IC’s and design the circuit with least number of wires crisscrossing
- Read all the datasheets carefully. Do not connect inputs to outputs
Contents of the Lab Report

- State diagram for the FSM
- State Table for One-Hot encoding
- Karnaugh maps for the Next State combinational logic
- Schematic of the complete circuit
- Timing diagrams for input and output.

Documented by Avinash Amarnath