ECE 271L – Digital Systems Lab
Spring 2010

Lab Project #1
Counter Design Using D–Flip Flop
Objective

- Design and demonstrate a synchronous counter using D flip-flops with the following count sequence:
  
  $0 \rightarrow 2 \rightarrow 1 \rightarrow 3 \rightarrow 1 \rightarrow 3 \rightarrow 1$

- Use a 1 Hz clock for the circuits and connect the counter outputs to LEDs so you can monitor the count sequence.
References

- Digital Design Principles And Practices, 3e, John F. Wakerly (Text book used in the class)
- Digital Design, 4e, Morris Mano & M. D. Ciletti
Background

- Counter – set of registers which go through predefined sequence of states
- Input pulses are usually a clock
- Two types – ripple and synchronous
- Ripple – Clock of flip-flops driven by output of other flip flops
- Synchronous – All the flip-flops have a common clock input. It is Moore State Machine but no output logic is needed
Moore State Machine

Diagram:

- Inputs
- Next State Combi. Logic
- Present State Register
- Output Combi. Logic
- Moore Outputs
- Clock
- Reset
- Preset state
- Moore Outputs
Materials

- D flip flops
- Logic function IC’s (inverter, NAND or OR)
- Function Generator
- LED’s
- DIP switch
- Resistors
Requirements

- Build the circuit on the breadboard and demonstrate the correct counter outputs to the TA
- Submit the lab report to the TA by the due date
Guidelines to build the circuit

- Implement reset using a DIP switch and voltage divider circuit
- LED’s should be connected in series with a resistor
- Place the IC’s and design the circuit with least number of wires crisscrossing
- DIP switch can also be used to turn or off the clock input
- Read all the datasheets carefully. Do not connect inputs to outputs
Contents of the Lab Report

- State diagram for the counter state machine
- State Table for the counter with binary encoding
- Karnaugh maps for the Next State combinational logic
- Schematic of the complete circuit