Agenda

Objective
3 problems this paper try to solve
Solutions to the three problems
Small signal models analysis and simulation
Test circuit and results
Conclusion

Introduction

The PSRR is defined as the ratio of signal path gain to the gain of power supply to Vout transfer function.
It simplifies to the ratio of the change in supply voltage to the equivalent (differential) input voltage it produces in the op-amp, often expressed in decibels.

\[ \text{PSRR} = \frac{\Delta V_{\text{supply}}}{\Delta V_{\text{IOS}}} \]

Objective:

This paper presents two circuits that overcome the PSRR problems of the earlier amplifier. One for virtual ground applications such as switched-capacitor integrators, and the other for buffer applications requiring wide common-mode input range.

Small signal analysis is developed for the open loop and PSRR responses of the two amplifiers. In addition, design guidelines are suggested and test results are presented.

A test circuit including these amplifiers has been fabricated and demonstrates the improved performance.

Problem 1: poor ac PSRR

Internally compensated two-stage CMOS op amp suffers from poor ac power supply rejection to one of the power rails.

Cause: The output drive transistor at moderate frequencies becomes "diode connected" with its drain ac shorted to its gate by the compensating capacitor, which couples the supply signal to the output.

![Diagram](image.png)

Fig. 1. A conventional internally compensated CMOS op amp.
Fig. 4. An ac small-signal model for the op amp of Fig. 1.

Fig. 5. An ac small-signal PSRR model for the op amp of Fig. 1.
The article ignores the $g_{m1}/g_{m2}$ dependent-sources saying
"$g_{02}$ connects to the source of the input pair which is an open-circuit for common-mode signals
such as power supply noise and must be excluded."
The model in the article basically removed the circuit on the left of D2.

$$\text{PSRR}(s) \approx \frac{(s + \omega_{pd})}{(s + \omega_{p})}$$

The zero at the low frequency of the dominant pole prematurely degrades the PSRR.
The explanation is that as frequency rises, the impedance of the compensation capacitor $C_C$ becomes low and the gate
and drain of M6 begin to track one another.
The transistor is current-source biased by M7 and must maintain a relatively constant gate-source drive consistent with
the bias current.
This requirement forces the gate of M6 to track VDD fluctuations which are in turn transmitted by $C_C$ to
the drain, which is the output of the amplifier.

**Solution to problem 1**
Cascoding technique greatly improves high-frequency rejection, as shown in Fig. 2.

M3/M4 decouples the gate of the driver transistor from the compensation capacitor.

A detailed small-signal model for the cascoded op amp presented in this paper simplifies the design of these op amps.
A small-signal PSRR model demonstrates the improvement in PSRR of the new op amps over the earlier one in Fig. 1.
Fig. 6. An ac small-signal model for the cascode op amps of Figs. 2 and 3.

DC gain

\[
\left| \frac{V_o}{V_i} \right|_{DC} = \frac{g_{m1}g_{m3}}{G_{01} + \frac{g_{01}(g_{02} + G_{01}/2)}{G_{m2}}} G_{02} \approx \frac{g_{m1}g_{m3}}{G_{01}G_{02}}.
\]

Fig. 8. A small-signal PSRR model for the cascode op amps of Figs. 2 and 3.

\[
\text{PSRR}(s) \approx \frac{C_2}{C_C(1+\delta_3)} \left[ \frac{s + \frac{G_{01}G_{02}}{g_{m3}C_2}}{s + \omega_T \frac{1}{(1+\delta_3)}} \right]
\]

compared to the original PSRR
**Problem 2: reduction in common-mode input range**

One disadvantage of this circuit is a reduction in common-mode input range due to the voltage drop across the cascodes.

The common-mode input cannot be too high to force the input device out of saturation.

\[ V_{\text{in,max}} < V_{\text{bias1}} \] vs \[ V_{\text{in,max}} < V_{\text{DD}} \] on the figure 1

**Solution to problem 2**

The folded cascode technique presented in Fig. 3 has wide common mode range and retains the benefits of the compensakicmapproach.

It has wide range if the source, and hence, the gate bias of the cascode devices are low.

The gate voltage of M3 and M4 can be quite low, restricted only by the need to maintain the n-channel current sources M10 and M11 in saturation.

\[ V_{\text{in,max}} < V_{\text{DD}} - V_{\text{th1}} - V_{\text{sat,M7}} \]

**Problem 3: that circuit on Fig 3 solved: Spiky output on large common mode input**
A recent paper [7] presented an n-channel input circuit similar to the circuit of Fig. 3, and emphasized its widecommon-mode input range. That circuit, however, suffers from a peculiar adversity due to its biasing, which can be discussed in the context of the p-channel input circuit of the present paper.

If the gates of transistors M10 and M11 are driven by a fixed voltage, as in [7], then for large positive common-mode inputs, as exists with a voltage follower for example, the output will abruptly spike up to the positive supply voltage. The sources of the input transistors reduce the drain-source voltage MT, for large positive common-mode inputs, and the bias current is reduced substantially.

For large positive common-mode inputs, the input pair current is thus too small to be significant with respect to the fixed bias current of M10 and M11, and the gate voltage of the output driver M8 is therefore abruptly pulled down, causing the output to pull high.

**Solution to problem 3**
This problem can easily be avoided by using the novel biasing technique for the n-channel current sources (M12 – M13) shown in Fig. 3. A current mirroring approach is used here whereby the bias current through M10 and M11 tracks the current through the input source-coupled pair. For excessive positive common-mode inputs, the use of M13 with its gate driven by the plus input, will force the current of M13 to follow that of MT. This imposes the same reduced drain-source voltage on M13 as on MT, and this current is mirrored to the n-channel transistors. Difference-mode input components are normally held very small by feedback, and thus do not modify this behavior significantly. Through the use of this method there is no penalty when the common-mode input limit is exceeded other than soft clipping.

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**Simulation Results**
Also included in the figure is a PSRR frequency response curve for a noncascoded version of the same op amp. A major improvement in high frequency PSRR (>30 dB) is evident for the cascoded, op amps.

Test Results
In all other respects similar test results were obtained for both amplifiers as expected and are outlined for the circuit of Fig. 2, in Table I. A photograph of the experimental VDD PSRR for the circuit of Fig. 3 showing the excellent high-frequency rejection ( >49 dB at 100 kHz) appears in Fig. 11.

**CONCLUSIONS**

1. PSRR improvement for both circuits.
2. The circuit solves an output spike phenomena which arose in a previously reported op amp.
3. The small signal model is validated by simulation and test results.
4. Design techniques for frequency compensation are presented.