Task for this week: Finish up PLL, a lecture on CMOS interfacing.

The final assignment for ECE 323 2015 is a 4 page final lab report on your Phase Locked Loop, due in class on Thursday June 11 during the scheduled Final Exam period. You are encouraged to bring your Phase-Locked-Loop to class on that day for discussion and comparison with other students.

The four pages of your final lab report are as follows:

Page 1. Your name, and the name(s) of a lab partner if any. Title: Final 2015 ECE 323 Phase Locked Loop Report. The block diagram of a phase locked loop, with $k_f$ and $k_{vco}$ labeled on the block diagram.

Page 2. A detailed schematic of your VCO, including the component values you used, number of turns on the inductors and type of ferrite core, and the diode you used as a varactor. Schematic of phase detector with capacitor and any resistor values. This may be an ADE-1 or one you built using diodes and toroids.

Page 3. Measured performance. Measured $k_f$ and $k_{vco}$. You measured $k_f$ early in the quarter. Include a measurement of the complete tuning range of your vco with a variable dc supply connected to the tuning diode input. Measured lock range and capture range. Observations of instability or strange behavior.

Page 4. Follow-on experiments of your choice. Examples might include: experiments with FM demodulation, including a 74HC74 divide by 2 or divide by 4 in the loop, adding an LED lock detector... It is not necessary to have completed the experiments, just describe them well enough that your understanding is clear.

Thank you for all your hard work this quarter, as we experimented with a new VCO design. This has been a most interesting class, and has immersed us in the core of electronics, building on essential understanding and skills.