Before Lab: To begin Lab 3, you must have a working PLL with floating SBL-1 IF ports, a screen shot showing the loop voltage to the VCO and a spectrum analyzer screen shot showing the VCO output when unlocked and locked. You will also need measured lock and capture range, and a detailed schematic from Lab 2 showing the component values you used.

After you have documented a working first order PLL in Lab 2, you will use Lab 3 to make changes to the working circuit. Here are some suggested lab 3 modifications/improvements/changes to the Lab 2 circuit. Select at least 2 from the following list. Make the changes and document the performance in the lab.

1. Shorten leads and make a neater layout, perhaps with a different construction technique.
2. Analyze, design, implement a second order loop with a lead-lag filter
3. Clean up the output frequency spectrum.
4. Demodulate an FM signal
5. Modulate, radiate, and receive an FM signal
6. Lock to a harmonic of a crystal oscillator
7. Build a JFET Hartley VCO and replace the POS-100
8. Replace the SBL-1 with an XOR phase detector.
9. Explore the optimum use of the prototyping board at Very High Frequency

Your Lab 3 work and report are the major project components of the ECE323 course. Be sure that you include all 3 essential parts of a project: Description/Analysis, Simulations, and Measurements of hardware. This report is due Wednesday June 12, and the final week of class, from June 3 to June 7 will be devoted entirely to getting the Lab 3 projects finished up and measured for the report. Get started early--many students have already completed more than one of the suggestions from the above list.

Work hard and have fun.