Lecture 5: DRAM Basics
DRAM Evolution
SDRAM-based Memory Systems

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Sources: Lecture based on materials provided by Mark F. Jacob’s DRAM Systems article
Memory component datasheets
Outline

- Taxonomy of Memories
- Memory Hierarchy
- SRAM
  - Basic Cell, Devices, Timing
- DRAM
  - Basic Cell, Timing
- Memory Organization
  - Multiple banks, interleaving
- DRAM Evolution
- DDR3 SDRAM
- DRAM modules
- Error Correction
- Memory Controllers
Dynamic RAM (DRAM)
DRAM Technology

- **Write**
  - Drive bit line
  - Select desired word ("row")

- **Read**
  - Pre-charge bit line
  - Select desired word ("row")
  - Sense charge
  - Write value back (restore)

- **Refresh!**
  - Periodically read each cell
    - (forcing write-back)

Read is destructive → must restore value
Charge leaks out over time → refresh

1 transistor

Bit state (1 or 0) stored as charge on a tiny capacitor
Volatile Memory Comparison

- **Larger cell**
  - lower density, higher cost/bit
- **Non-destructive Read**
- **No refresh required**
- **Simple read** $\Rightarrow$ faster access
- **Standard IC process** $\Rightarrow$ natural for integration with logic
- **Non-multiplexed address lines**
  - Density “low enough” to keep the number of address lines reasonable

- **Smaller cell**
  - higher density, lower cost/bit
- **Destructive Read**
- **Needs periodic refresh**
- **Complex read** $\Rightarrow$ longer access time
- **Special IC process** $\Rightarrow$ difficult to integrate with logic circuits
- **Multiplexed address lines**
  - Density $>>$ SRAM density so would require lots of address lines
DRAM Device Pin Outs

- Cost Rules!
  - Fewer pins, smaller package, less $

- So Multiplex
  - Data (In/Out)
    - /WE asserted (low) for write
    - /OE asserted (low) to enable output buffers
  - Address (Row/Column)
    - /RAS (Row Address Strobe) asserted after row placed on address pins
    - /CAS (Column Address Strobe) asserted after column placed on address pins

256K = 18 address bits
9 row address bits
9 column address bits

2Mb (256K x 8) DRAM

Data (DQ)

Address

/RAS
/CAS
/WE
/OE

Address

Row Address
Col Address

RAS

CAS
DRAM Organization

We want to keep row/column organization (square is good) but get devices of more than x1 bit wide

(from Bruce Jacob)
Square keeps the wires short:
Power and speed advantages
Less RC, faster pre-charge and discharge \( \rightarrow \) faster access time!

Internal DRAM Organization 2Mb as 256K x 8

- Select the addressed bit
- Do this 8 times
- Read 512 bits at a time
DRAM Timing
DRAM Timing

- **Read cycle - RAS + CAS**
  - (RAS asserted)  Entire row is latched in a data register
  - (CAS asserted)  Data in register is multiplexed to output
  - (RAS de-asserted) Data in data register is rewritten to row in array
  - (CAS de-asserted) Output is released

- **Write cycle - RAS + WE + CAS**
  - (RAS asserted)  Entire row is latched in data register
  - (WE asserted)  Data to be written is stable
  - (CAS asserted)  Write Data to register
  - (WE de-asserted) Data to be written is no longer stable
  - (RAS de-asserted) Data in data register is rewritten to row in array
  - (CAS de-asserted) Operation complete

- **Refresh cycle - RAS Only**
  - (RAS asserted)  Entire row is latched in data register
  - (RAS de-asserted) The data in the register is rewritten to row in array
DRAM Read Timing

- Every DRAM access begins at:
  - The assertion of the /RAS
- After the row access is complete, /CAS is asserted

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256K x 8 DRAM
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/RAS ————

/CAS

Row Address

Col Address

Junk

Row Address

Col Address

Junk

/WE

/OE

D High Z X Junk X Data Out X High Z X Data Out

Read Access Time

Output Enable Delay
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DRAM Write Timing

- DRAM WR Cycle Time
- /RAS
- /CAS
- /OE
- /WE
- A: Row Address
- Col Address
- Junk
- Row Address
- Junk
- D: Junk
- Data In
- Junk
- Data In
- Junk
- WR Access Time
- WR Access Time
Key DRAM Timing Parameters

- $t_{RCD}$: RAS to CAS Delay
  - Minimum time between RAS asserted and CAS asserted

- $t_{CAC}$: Column Access Time
  - Delay from falling /CAS to valid data out

- $t_{RAC}$: Random Access Delay
  - Minimum time from /RAS falling to valid data output
  - Quoted as the speed of a DRAM
  - $t_{RAC} = t_{RCD} + t_{CAC}$

- $t_{RAS}$: Row Address Strobe
  - Minimum time /RAS must be maintained

- $t_{RP}$: Row Pre-Charge Delay
  - Minimum time to pre-charge before /RAS can be asserted again

- $t_{RC}$: Row Cycle Time
  - Minimum time between successive row accesses
  - $t_{RC} = t_{RAS} + t_{RP}$
DRAM Evolution
DRAM Evolution...A Technology Timeline

- BEDO – Burst Extended Data Out
  - SDRAM
  - DDR SDRAM (double data rate)
  - DDR2
  - DDR3
  - DDR4

- Other DRAM technologies
  - Rambus DRAM (RDRAM)
  - Concurrent Rambus DRAM
  - Direct Rambus DRAM (DRDRAM)

- Numerous Specialty DRAMs not shown
  - Virtual Channel Memory (VCDRAM)
  - Enhanced SDRAM (ESDRAM)
  - MoSys 1T-SRAM
  - Reduced Latency DRAM (RLDRAM)
  - Fast Cycle DRAM (FCRAM)

By 2002 most PCs were shipping with SDRAM and DDR SDRAM
By 2015 PCs were shipping with DDR4 in volume...and still are

(from Bruce Jacob & David Wang)
Conventional DRAM Read Timing

(from Bruce Jacob & David Wang)
Fast Page Mode DRAM Read Timing

- Innovation – Hold entire row (page) in sense amplifiers
- Benefit – CPU can access each column in row without providing row address (and pre-charging) each time

(from Bruce Jacob & David Wang)
Extended Data Out DRAM Read Timing

- Innovation – Add latch between sense amplifiers and output pins
- Benefit – Can begin pre-charging sooner (data from prior access remains valid)

(from Bruce Jacob & David Wang)
Burst EDO DRAM Read Timing

- **Innovation** – DRAM provides column data sequentially
- **Benefit** – No need to transfer column address on each read

(from Bruce Jacob & David Wang)
Synchronous DRAM Read Timing

- Innovation – Pipeline access, command interface (vs. individual signals)
- Benefit – Simplified timing, command interface,...
SDRAM (Synchronous DRAM)

- Adopted for Pentium use
- Synchronous (clocked) interface
- RAS, CAS, WE, CS signals combined to make "command"
- Burst read/write
  - Initial latency, then data every clock cycle
- Internal interleaved banks allow multiple rows (pages) to be "open" for read/write
- Ideal for cache line fill when bus width < cache line size
SDRAM Details

- Multiple “banks” of cell arrays are used to reduce access time:
  - Ex: Each bank is 4K rows by 512 “columns” by 16 bits
  - Read and Write operations are split into row access followed by column access

- These operations are controlled by sending commands
  - Commands are sent using the RAS, CAS, CS, & WE pins.

- Address pins are “time multiplexed”
  - During RAS operation, address lines select the bank and row
  - During CAS operation, address lines select the column.

- “ACTIVATE” command “opens” a bank/row for operation
  - Transfers contents of the entire row to a buffer

- Subsequent “READ” or “WRITE” commands access the contents of the row buffer

- For burst reads and writes during “READ” or “WRITE” the starting address of the block is supplied.
  - Burst length is programmable as 1, 2, 4, 8 or a “full page” (entire row) with a burst terminate option

- Special commands are used for initialization (burst options etc.)

- A burst operation takes \( \approx 4 \) (address/read row) + n cycles (for n words)