Problem No. 1 (12 points)

For each of the following statements, indicate whether the statement is **TRUE** or **FALSE**:

(a) In single handshake protocol, the sender does not need to seek permission from the receiver before transmitting the data.  **TRUE**

(b) DRAM refresh overhead usually decreases with an increase in DRAM device density.  **FALSE**

(c) Parallel tag and data access is commonly used in L2 and L3 caches.  **FALSE**

(d) Serial buses usually operate at faster speeds as compared to parallel buses.  **TRUE**

(e) In a USB-based I/O system, any USB device can become the bus master.  **FALSE**

(f) The relationship between a TLB and page table is the same as the relationship between a cache and main memory.  **TRUE**

Problem No. 2 (9 points)

For each of the following questions, encircle **ALL** the correct answers:

(a) Which of the following are advantages of using an 8b/10b transmission code?
   
   i. Reduces the total amount of data transferred  
   ii. Guarantees that the edge density is sufficient to recover clock from the embedded clock/data signal  
   iii. Ensures that the signal is DC balanced  
   iv. None of the above

(b) Which of the following techniques can be used to reduce the cache hit time?
   
   i. Way prediction  
   ii. Increase the associativity of the cache  
   iii. Increase the size of cache  
   iv. Use multiple cache banks

(c) Which of the following is a disadvantage of using a virtually indexed, virtually tagged cache?
   
   i. TLB access needs to complete before the cache is accessed  
   ii. Aliasing  
   iii. Lower associativity  
   iv. None of the above
Problem No. 3 (17 points)

Consider a computer system with a two-level cache hierarchy. The system parameters and statistics for a program are as follows:

(i) L1 cache access rate is 300 accesses per 1000 instructions,
(ii) L1 cache hit ratio is 90%,
(iii) L1 cache hit time is 3ns,
(iv) L2 cache miss rate is 12 misses per 1000 instruction,
(v) L2 cache hit time is 10ns,
(vi) The main memory (DRAM) in the system consists of an 8GB PC3-12800 DIMM with (10-10-10-25) timing and a burst length of 8
(vii) The memory controller uses the open page policy. Row buffer hit rate is 60%,
(viii) TLB latency is 2ns and TLB hit ratio is 100%,
(ix) Each cache in the system is a blocking cache that only processes one miss at a time, and blocks all other accesses until the miss returns from the next cache level or the memory.
(x) For both L1 and L2 caches, determining if an access is a miss takes the same out of time as returning the data in case of a hit.

Answer the following questions:

(a) (7 points) Calculate the average DRAM access latency.

The DIMM clock on PC3-12800 is 12800/8/2 or 800 MHz.
Therefore, 1 DRAM clock cycle = 1/800MHz = 1.25 nsec
A single burst requires 8 data transfers. There are 2 data transfers in one DRAM clock cycle. Therefore, tBURST = 8/2 = 4 cycles
Row hit latency = tCL + tBURST = 10 cycles + 4 cycles = 14 cycles
Row miss latency = tRP + tRCD + tCL + tBURST = 10 + 10 + 10 + 4 = 34 cycles
Row buffer hit rate = 60%
Therefore, average DRAM latency = (60% * 14) + (40% * 34) = 22 cycles = (22 * 1.25) nsec = 27.5nsec

(b) (5 points) Calculate the L1 and L2 cache miss ratios.

L1 cache miss ratio = 1 – L1 cache hit ratio = 1 – 90% = \textbf{10%}
L1 cache miss rate = L1 cache access rate * L1 cache miss ratio = 300 * 10% = 30 MPKI
L2 cache access rate = L1 cache miss rate = 30 accesses PKI
L2 cache miss rate = 12 MPKI
Therefore, L2 cache miss ratio = 12 / 30 = \textbf{40%}
(c) (5 points) Calculate the average memory access time (AMAT) for this system.

L2 hit time = 10ns, L2 hit ratio = 60%
L2 miss ratio = 40%, L2 miss time = 10ns + average DRAM latency = 10ns + 27.5ns = 37.5ns
AMAT of L2 cache = (L2 hit time * L2 hit ratio) + (L2 miss time * L2 miss ratio)
= (10ns * 60%) + (37.5 * 40%) = 21ns
L1 hit time = 3ns, L1 hit ratio = 90%
L1 miss ratio = 10%, L1 miss time = 3 + AMAT of L2 cache = 3ns + 21ns = 24ns
Therefore:
AMAT of L1 cache = (L1 hit time * L1 hit ratio) + (L1 miss time * L1 miss ratio) = (3ns * 90%) + (24ns * 10%) = 5.1ns

Problem No. 4 (21 points)
Consider a memory system with the following parameters:
- L1 Data Cache is 16KB, 2-way set associative, 32 bytes/line and uses writeback policy
- Translation Lookaside Buffer (TLB) has a total of 512 entries and is 2-way set associative.
- 42-bit Virtual address, 32-bit physical address, 8KB page size

(a) (11 pts) Below is a block diagram of the cache and TLB.
Refer to the different fields A, B, C, D, E, F, G, H and I shown in the above diagram. Then, complete the following table by filling in the width of each of the fields in terms of number of bits.

<table>
<thead>
<tr>
<th></th>
<th>L1 Cache</th>
<th>TLB</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>19 bits</td>
<td>F</td>
</tr>
<tr>
<td>B</td>
<td>8 bits</td>
<td>G</td>
</tr>
<tr>
<td>C</td>
<td>5 bits</td>
<td>H</td>
</tr>
<tr>
<td>D</td>
<td>256 bits</td>
<td>I</td>
</tr>
<tr>
<td>E</td>
<td>21 bits</td>
<td></td>
</tr>
</tbody>
</table>

(b) (5 pts) Assume that the same virtual address, physical address and page sizes (from part a) are being used in a hierarchical paging system like the one described in class (Page Table Directory + Page Table(s) + Page Frame(s)). Assume that the PTDE (Page Table Directory Entry) and PTE (Page Table Entry) are each 4-bytes wide. Also assume that the Page Table Directory takes up a total of 64KB of physical memory. How are the virtual address bits distributed between the indices of the Page Table Directory and the Page Tables? In other words, how many address bits are needed to access each of the levels in the paging hierarchy?

Given a 42-bit virtual address and 8KB (2\(^{13}\)) page size, we have 42 – 13 = 29 bits to split between the page table directory and the page tables.
Page Directory takes up 64KB of memory and each PDE is 4-bytes wide.
Therefore, number of PDEs = 64KB / 4B = 16K = 2\(^{14}\)
Hence, 14 address bits are needed to access the page table directory.
The remaining 29-14 = \(29 - 14 = 15\) address bits are needed to access the page table.

(c) (5 pts) Assume that only 1/8th of all the page tables are populated and resident in memory. How much physical memory is taken up by the page tables?

Since the page directory has 2\(^{14}\) entries and only 1/8\(^{th}\) of all the page tables are populated,. Therefore, there are 2\(^{14}\) * (1/8) = 2\(^{11}\) page tables taking up space in the physical memory.
Each of these page tables has 2\(^{15}\) PTEs.
Therefore, the physical memory consumed by all the page tables = 2\(^{11}\) page tables * 2\(^{15}\) PTEs per page table * 4 bytes/PTE = 256MB
Problem No. 5 (16 points)

(a) (6 points) A 4-processor system implements the MESI cache coherence protocol to keep all the processor caches coherent. For the following sequence of accesses, show the state of the cache line containing the variable a in each processor’s cache after each access is completed. Each processor starts out with the line containing a invalid in its cache.

<table>
<thead>
<tr>
<th>Access</th>
<th>State of P0’s cache</th>
<th>State of P1’s cache</th>
<th>State of P2’s cache</th>
<th>State of P3’s cache</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start</td>
<td>I</td>
<td>I</td>
<td>I</td>
<td>I</td>
</tr>
<tr>
<td>P1 reads a</td>
<td>I</td>
<td>E</td>
<td>I</td>
<td>I</td>
</tr>
<tr>
<td>P2 reads a</td>
<td>I</td>
<td>S</td>
<td>S</td>
<td>I</td>
</tr>
<tr>
<td>P3 writes a</td>
<td>I</td>
<td>S</td>
<td>I</td>
<td>M</td>
</tr>
<tr>
<td>P0 writes a</td>
<td>M</td>
<td>I</td>
<td>I</td>
<td>M</td>
</tr>
<tr>
<td>P1 reads a</td>
<td>S</td>
<td>S</td>
<td>I</td>
<td>I</td>
</tr>
</tbody>
</table>

(b) (3 points) State two factors which can cause the “actual bus bandwidth” to be less than “theoretical bus bandwidth”.

Protocol overhead (for example, cycles to send address)
Arbitration and error phases

(c) (4 points) How does a disk drive handle bad blocks? What techniques are used to present a contiguous LBA address space to the user in the presence of bad blocks?

The disk controller prevents the bad block/sector to be accessed by remapping the LBA to a different block/sector in the disk. One of the following techniques can be used:
Sector Slipping - If a sector is bad, find next non-defective sequential sector to be that LBA Sector Sparing - Reserve some spare sectors at one or more locations on the disk.

(d) (3 points) During PCI enumeration, each PCI device reports two parameters: Max_Lat and Min_Gnt to the PCI arbiter. What is meant by these two parameters?

Max_Lat = maximum permissible bus access grant delay
Min_Gnt = minimum time during which the device must have control over the bus after it has been granted the bus