1. [15 points] If a computer has a virtual address size of 32 bits and a page size of 2048 bytes, then how many page table entries are needed?

How many levels of paging does such a memory system require?

If each page table entry is 4 bytes, how much space do the page table entries take?

2. [15 points] Suppose we have a CPU with an L1 cache of size 512 kbytes (i.e. 512*1024 bytes). Further, suppose it takes 4 nanoseconds to access the L1 cache on a cache hit and 60 nanoseconds to access main memory on a cache miss. What is the necessary cache hit ratio necessary to achieve an average memory access time 20 nanoseconds across all memory references? What is the necessary cache hit ratio necessary to achieve an average memory access time of 10 nanoseconds across all memory references?

3. [15 points] Suppose we have a 1 MB cache that is 4-way set associative and has 32-byte lines. What size are the offset, set id, and tag for this caching scheme?

How does this change for a 64-byte line cache?