

Droop Compensation Versus Ideal Regulation

By **Conor Quinn**, Product Marketing Manager, and **Paul Nikkel**, Principal Design Engineer, Artesyn Technologies, Eden Prairie, Minn.

Advances in silicon technology have led to significantly faster processors, memory and switching logic. These high-performance semiconductor devices can demand very fast changes in load current, posing considerable challenges for the voltage regulator supplying their core voltage. When switching out of “sleep” mode, for example, processors often activate a large number of hitherto dormant circuits, resulting in a large step-change in load current within a few hundred nanoseconds. Minimizing peak-to-peak voltage deviation in the face of such large dynamic changes in load current involves innovative power conversion techniques, especially if large amounts of output capacitance are to be avoided.

Several techniques have been proposed to address these challenging regulation requirements. One method that has gained wide industry acceptance is called “droop” compensation. Designers interested in applying this technique must understand how it works, when it should be used, and more importantly, when it should not be used.

Reduced Transient Response

Droop compensation intentionally increases the dc output impedance of a converter, lowering its output voltage, as load current increases. The technique was first employed with dc-dc converters designed for parallel operation to help balance current sharing. It is now used by a number of the leading multi-phase pulse width modulated (PWM) controller ICs and voltage regulator modules (VRMs) designed to power latest-generation processors. The effect of droop compensation is to reduce overshoot of the core

voltage during large step changes in load current.

Artesyn’s new VRM10 series of processor power VRMs, for example, include two models with different power ratings and different levels of droop compensation. Both models comply with Intel’s VRM10.x specifications. The top-of-the-range VRM10-85-12-U model, which is intended for powering high-end server-type processors, such as Intel’s Xeon, has an output load line impedance, or droop compensation value of 1.25 m Ω . Fig. 1 shows that with this level of droop compensation, if the VRM is programmed to generate a 1.4-V output, this will decrease to 1.275 V at 100 A of load current.

As highlighted in Fig. 1, if the processor is demanding very little current, it makes sense to stay at the top of the regulation window, because any step change in current demand can only result in a lowering of the VRM’s output voltage. Conversely, if the processor is operating at full load the next step-change in current can only be to a lower value, causing a rise in VRM output voltage. Thus, it is best to stay at the bottom of the regulation window. It follows that at half load, when the next (worst-case) step change can by definition only be a half-load step, it is best to be positioned in the middle of the regulation window.

Droop compensation has the potential for improving the load step response by a factor of two, as shown by the waveforms in Fig. 2a. In this figure, the black waveform represents the output voltage of the converter without droop compensation during a transition from no load to full load and back to no load. The red waveform shows the output voltage with droop compensation. In both scenarios, the magnitudes of the voltage excursions are identical during the load transients. However, the total excursion under droop compensation is reduced by a factor of two by modifying the regulation point with load current. In effect, the output impedance of the converter is programmed to match the ESR (equivalent series resistance) of the output capacitors.

However, this fact is only true for a full-load step. The magnitude of the voltage excursion can be estimated by multiplying the step current by the ESR of the output capacitors. No PWM controller can change that fact of life for power system designers, whose job is to decide how much, if any, output resistance to design into a VRM. Figs. 2a (full-load step), 2b (half-load step) and 2c (quarter-load step) may help them choose the most appropriate load line *Continued on page 67.*

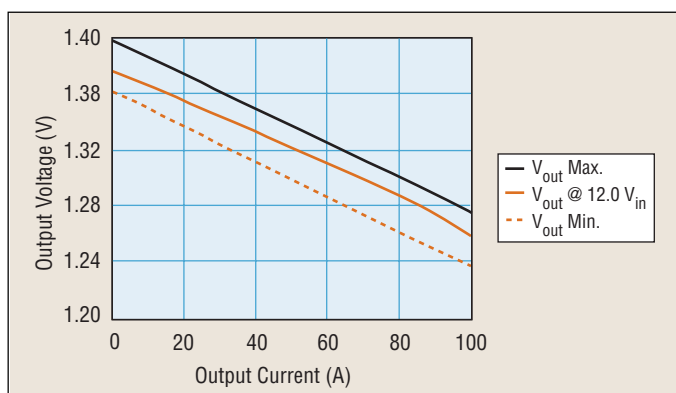


Fig. 1. Droop compensation characteristic of Artesyn’s VRM10-85-12-U.

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impedance. These diagrams illustrate how the magnitude of the required step response is a key factor in making this decision.

The amount of droop shown matches the output voltage change for a full-load step, which corresponds to a dc output impedance that matches the effective ESR of the distribution impedance, including all the output capacitance.

Choosing the amount of droop compensation to apply remains a slightly empirical process, because the designer needs to know the worst-case transient load change that the system is likely to experience. This may prove hard to predict, in which case it is probably best to err on the side of caution and be prepared for full-load transients; if this results in an unacceptable degree of droop, more capacitors can be used to lower the ESR, so that less droop is needed.

If the load-step magnitude is between 100% and 50% of full load, droop impedances less than the ESR magnitude also can result in some improvements. However, for load steps of less than 50% of full load, droop compensation is unlikely to offer any performance advantages, as highlighted by Fig. 2b, which shows both a 0% to 50% step response and a 50% to 100% step response. Fig. 2c, for example, shows how droop can actually degrade performance if the step requirement is only quarter load.

A question often asked is whether the ESR of ceramic capacitors can be included in the ESR for calculating the ΔV for a ΔI step. Given that the impedance of the ceramic capacitors will be in parallel with the impedance of the electrolytic capacitors, the answer is yes, but only for a given frequency. The ESRs of ceramic and electrolytic capacitors may well be 15 m Ω apiece, but that doesn't mean that when connected in parallel they will have an ESR of 7.5 m Ω , because each type of capacitor will have its minimum ESR at a different frequency. An impedance analyzer can be used to produce a parallel impedance plot to verify

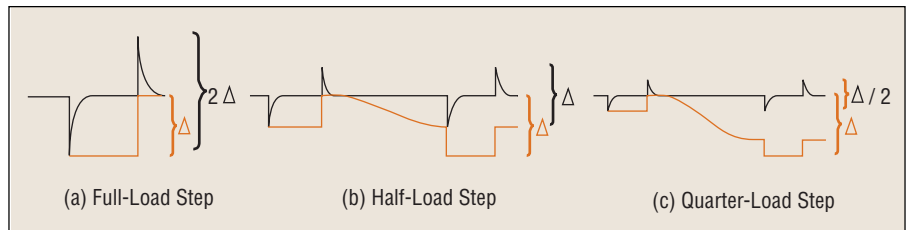


Fig. 2. Graphs comparing transient response characteristics with (red traces) and without (black traces) droop compensation for different load steps.

this; it will show two minimums of 15 m Ω at different frequencies, rather than a single minimum of 7.5 m Ω .

By monitoring the voltage on a processor running with a VRM that has a known droop characteristic, the output resistance or droop can be used as a current shunt. The dc voltage variation can be correlated to current variation. This may provide a way to measure processor current without the need for a current probe and a large inductive loop between the VRM output capacitors and the processor.

Droop compensation certainly has a role to play in processor power de-

livery. Eliminating voltage overshoot significantly improves transient response performance in the face of large step-changes in load current. As a result, Artesyn implements droop compensation on all its latest-generation VRM10 series converters. Droop compensation also can reduce the number of capacitors needed to maintain the required peak-to-peak dynamic response; this improves overall system reliability, lowers implementation costs and saves valuable board space.

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