Buck Converter Design Example and Loop Compensation Analysis

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Abstract

This paper develops a buck converter design example using different compensation methods to ensure closed loop stability and to optimize system performance. The effects of various compensator designs are shown using asymptotic Bode Plots which graphically describe the system stability criteria and provide insight to other factors which improve closed loop performance. Computer simulation results are included to show time domain step response behavior and to verify performance improvements.

1 Introduction

The Buck converter is a switch mode, DC-DC, power supply. It accepts a source voltage, V_g and produces a lower output voltage, V with high efficiency. An important component of a practical Buck converter is control feedback which assures a consistent output voltage and attenuates unwanted characteristics of the circuit. The feedback loop of a Buck converter presents several challenges which are explored in the compensation examples.

In this paper we present a series of example Buck converter feedback compensation approaches. The design of the Buck converter circuit is kept constant to allow comparison of the effects of different compensation schemes. The primary tool that will be applied to evaluate the different compensation approaches are asymptotic Bode plots which are drawn based on corner frequencies of each block in the converter. This methodology provides a quick and efficient assessment of circuit performance and an intuitive sense for the trade offs for each compensation approach. Bode plots also directly illuminate the two critical loop stability characteristics, gain and phase margin (GM and PM respectively).

Additional analysis of each compensation approach are done through computer simulation. The PECS [1] circuit simulator is used to evaluate the effects of V_g transients, a common problem in real power supply designs. A MATLAB [2] simulation is also performed to validate the manual Bode analysis and to determine the exact gain and phase margin. Finally a closed loop MATLAB simulation is used to show the ability of the feedback system to attenuate undesired effects as a function of frequency.

We explore the following topics in the remainder of the paper:

Section 2 Definition and analysis of the test circuit

Section 3 Behavior of an uncompensated Buck converter

Section 4 Dominant pole compensation with 3dB GM

Section 5 Pole-zero compensation with 3dB and 10dB GM

Section 6 Pole-zero compensation with two zeros

Section 7 Conclusions

Appendix Additional supporting materials

2 Buck Converter System Models

2.1 General Model [3]

Figure 1 is a block diagram of the system components of a Buck converter with feedback. The *Converter power stage* accepts V_g as its power source and the control input $d(s)$ to produce the output voltage V. The feedback sensor $H(s)$, monitors the converter output voltage which is then compared with a reference voltage V_{ref}. The difference output of these two voltages are provided to the feedback compensation circuit $G_c(s)$ and then to the pulse width modulator (PWM) which produces the control waveform for the switching converter $d(s)$.

$$T(s) = G_c(s) \left(\frac{1}{V_M} \right) G_{vd}(s) H(s) \tag{1}$$

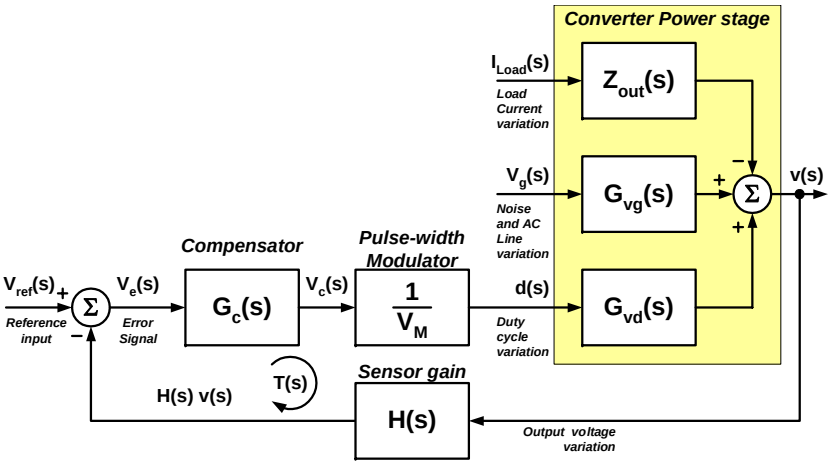

Figure 1: Generalized Power System Model [1]

2.2 Simplified System Model

The general Buck converter block diagram provides a complete model for analysis of converter. However, for our analysis we will use a simplified model show in figure 2 which includes only the elements required for the analysis we will provide. We do not evaluate any source of disturbance except V_g transients.

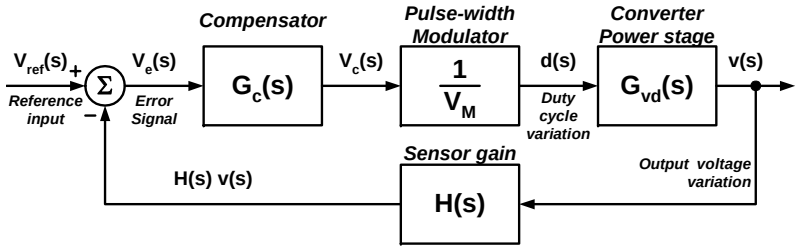

Figure 2: Simplified System Diagram

2.3 Design Targets

To facilitate easy comparison between the selected compensation schemes, the design of the Buck converter is fixed with specified values. These values are specified in table 1. Figure 3 shows the simplified block diagram including these specified values.

Table 1: Specified values

Name	Value	Description
V_g	28V	Input Voltage
V	15V	Output Voltage
I_{load}	5A	Test load
L	50uH	Buck inductor value
C	500uF	Buck capacitor value
V_m	4V	PWM compliance range
$H(s)$	1/3	Sensor gain
f_s	100kHz	PWM frequency

2.4 Buck Converter Model Analysis

Figure 4 shows a schematic model for the power converter block. The LCR is a second order circuit with a transfer function described by equation 2. It has a resonant frequency value, $f_0 = 6.28Krad/s$ or 1.0 kHz from equation 3 and a

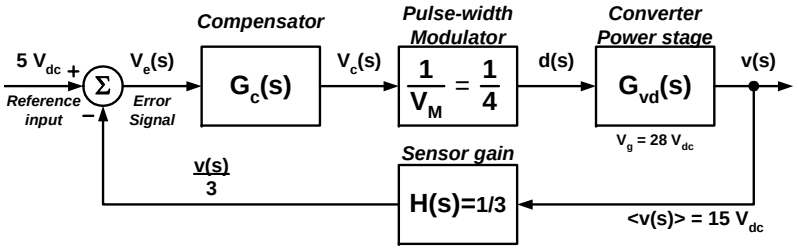

Figure 3: System Diagram With Values

Q of 9.5 from equation 4. The low frequency gain of the converter is equal to V_g which is specified to be 28V.

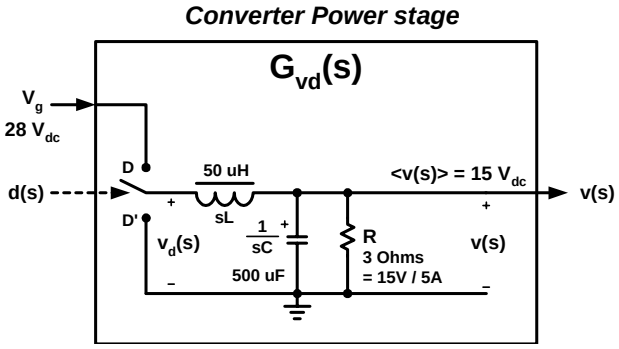

Figure 4: Converter Power Stage

$$G_{vd}(s) = V_g \frac{1}{1 + \frac{s}{Q_0 \cdot f_0} + \left(\frac{s}{f_0}\right)^2} \tag{2}$$

$$f_0 = \frac{1}{\sqrt{LC}} \tag{3}$$

$$Q = R\sqrt{\frac{C}{L}} \tag{4}$$

Consider the transfer function v(s)/vd(s) of the Low Pass Filter formed by the LCR network. The switching frequency $f_s = 100kHz$ is much higher than the resonant frequency $f_0 = 1kHz$ of the LCR. During circuit operation, the switch toggles the LCR input between V_g and ground with a duty cycle D determined by the feedback loop. A Fourier analysis of the LCR input waveform includes

an average DC component $V = DV_g$ and a f_s component with the harmonics produced by the square wave shape of f_s. The LCR acts as a low pass filter with a cut off frequency f_c equal to f_0. It passes the DC component to the output but attenuates f_s and its harmonics. The transfer function of the converter power stage $\frac{v(s)}{d(s)} = G_{vd}(f)$ is shown in figure 5.

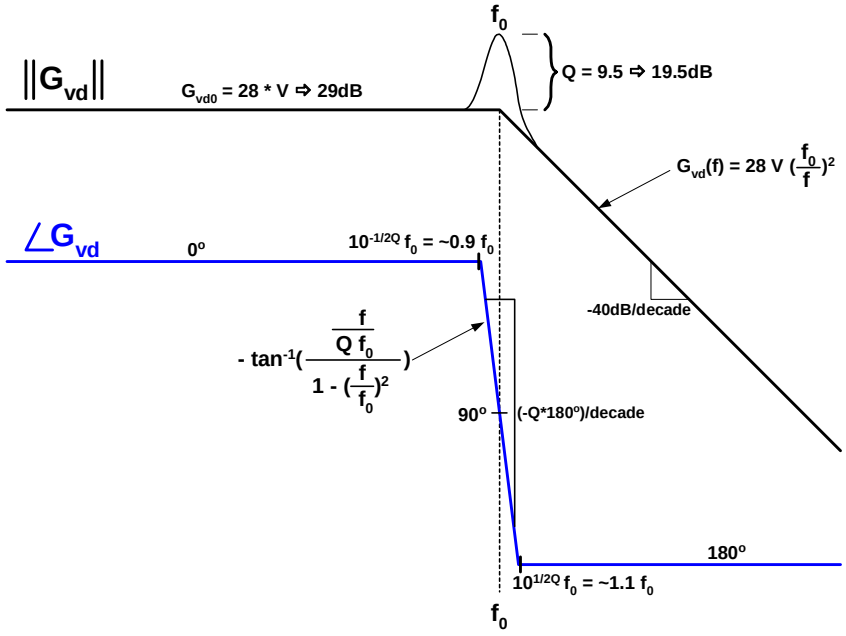

Figure 5: Converter Power Stage Transfer function $G_{vd}(f)$

3 Uncompensated Design

It is instructive to start our evaluation with an uncompensated converter, one with a $G_c(s) = 1$. To construct a Bode plot we use the values from equations 2-4 to establish the shape of the Bode magnitude plot. The low frequency gain is described by equation 5 has a value of 2.33 or 7.4dB. The magnitude around f_0 peaks to +19.5dB due to the resonant Q. At frequencies above f_0 the gain declines at -40dB/decade.

The Bode phase plot is determined only by $G_{vd}(s)$. It has a low frequency phase shift of 0°. At $f_0 10^{-\frac{1}{2Q}}$ or 886Hz, the phase turns negative and at f_0 the phase has reached $-90°$. The phase continues to become more negative until it reaches $-180°$ at $10^{\frac{1}{2Q}}$ or 1129Hz. At frequencies higher than 1129Hz the phase remains at $-180°$.

$$G_{LF} = \frac{V_g H(s)}{V_m} \tag{5}$$

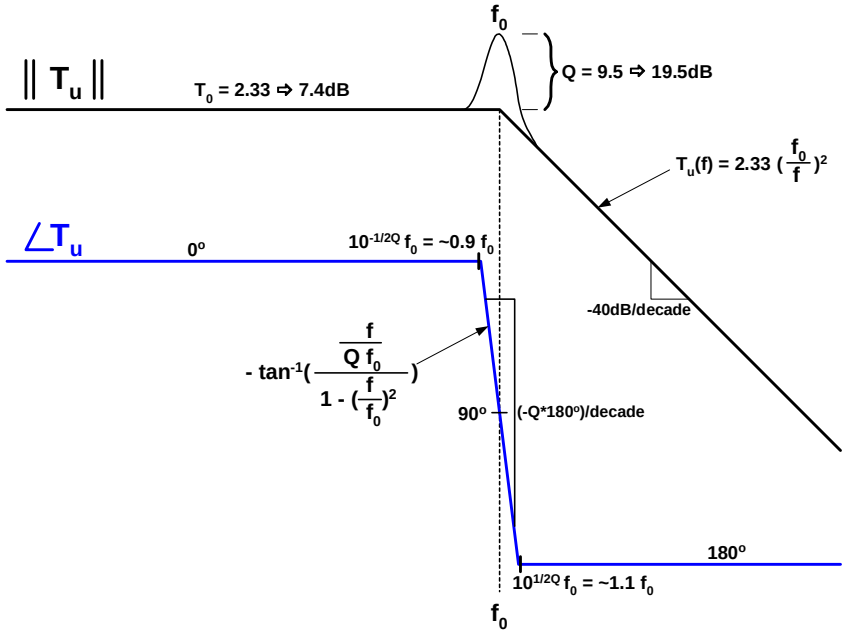

Figure 6: Uncompensated Gain and Phase Plot Tu(f)

From the Bode plot it can be determined that unity gain occurs at $7.4dB = (\frac{f_0}{f})^2$ which is 1.5 kHz. At this frequency the phase is $-180°$ providing zero phase margin. The exact gain margin is difficult to extract from the Bode plot due to the approximate shape near resonance but can be reasonably estimated to be -7dB, the feedback loop still has positive gain when the loop phase has shifted 180°. Figure 7 is a MATLAB margin plot indicating the actual unity gain frequency to be 1.8 kHz with a phase margin near zero. Because the phase shift at high frequencies is asmptotic to $-180°$ the MATLAB analysis indicate an infinite gain margin.

4 Dominant Pole Compensation

With frequency compensation an engineer strives to achieve two goals: 1) avoid oscillation from the unintentional creation of positive feedback and 2) control overshoot and ringing due to the step response. Probably the most commonly used form of compensation is dominant-pole compensation, which in

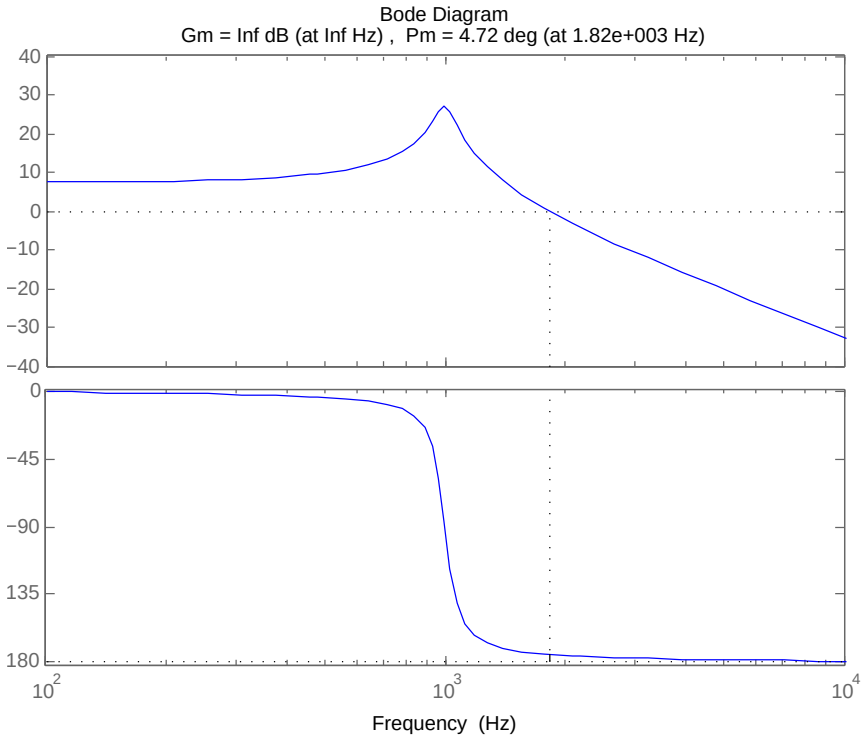

Figure 7: MATLAB Uncompensated Bode plot

reality is a form of lag compensation. A pole introduced at an appropriate low frequency in the open-loop response reduces the gain to 0 dB for a frequency close to or nearest the location of the next highest frequency pole. This lowest frequency pole is called the dominant pole because of its dominating effect over the all higher frequency poles. The overall result being that the difference between the open loop output phase and the phase response of a feedback network having no reactive elements never falls below $-180°$ while the system gain has a gain of one or more, thus ensuring stability.

4.1 Dominant Pole with 3dB Gain Margin

Including dominant pole compensation in the test converter will add an additional $-90°$ of phase shift to the loop transfer function. When combined with the LCR phase shift of $-90°$ at f_0 the frequency of zero phase margin is equal to f_0. To assure loop stability, we set the gain margin at f_0 to 3dB. From the Bode plots of the uncompensated circuit it can be seen that the magnitude at

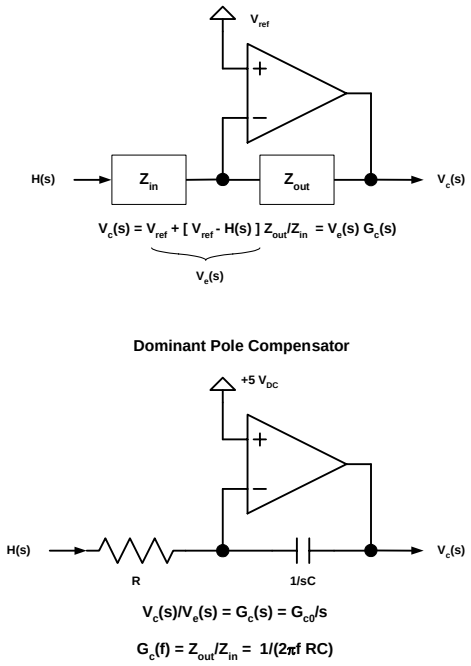

Figure 8: Dominant Pole Compensator Circuits

f_0 is $7.4dB + 19.5dB = 26.9dB$. Adding an additional 3dB for gain margin requires the dominant pole to provide an attenuation of 29.9dB at f_0.

Setting a pole at zero $G_C(s) = \frac{1}{s}$ produces an attenuation at f_0 of $20log(\frac{1}{f_0})$ or -76dB at f_0. To set the gain margin at f_0 to 3dB we must add an additional gain of $76dB - 29.9dB = 46.1dB$ or 202. The dominant pole now has the transfer function $G_c(s) = \frac{202}{s}$. The system loop Bode plot is shown in figure 9. Figure 10 shows the MATLAB that verify the gain and phase margins.

The dominant pole design was simulated using PECS simulation to determine sensitivity to V_g transients. Figure 11 is the PECS schematic diagram used in the simulation. Figure 12 shows the output V when a 2V step is imposed on V_g. The test toggles between a V_g of 28V and 30V.

The simulation shows significant ringing resulting from the V_g step. The frequency of the ringing is that of the LCR resonance f_0. From figure 9 it can be seen that the feedback loop has no gain at f_0 so the ringing is just the natural response of the LCR circuit when excited by the step input.

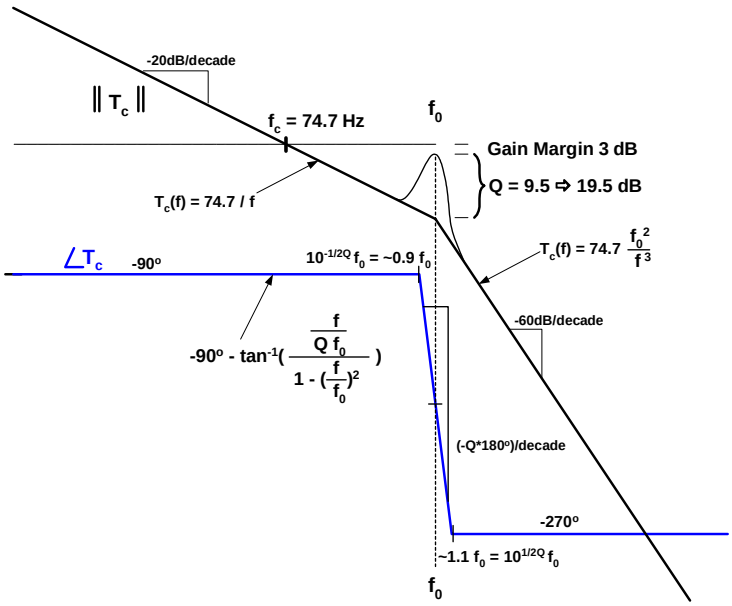

Figure 9: Open Loop System Gain and Phase with Dominant Pole Compensation

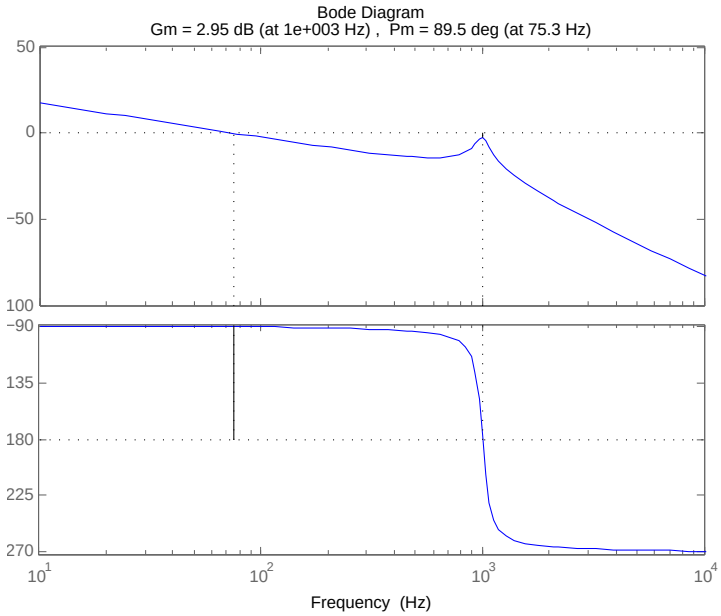

Figure 10: MATLAB single pole Bode plot

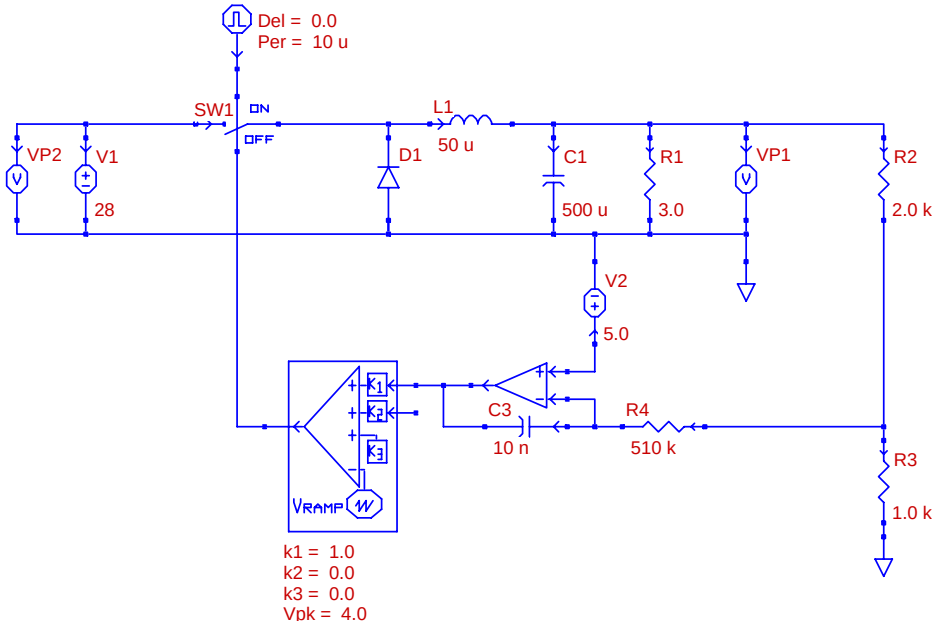

Figure 11: System Schematic with Dominant Pole Compensation

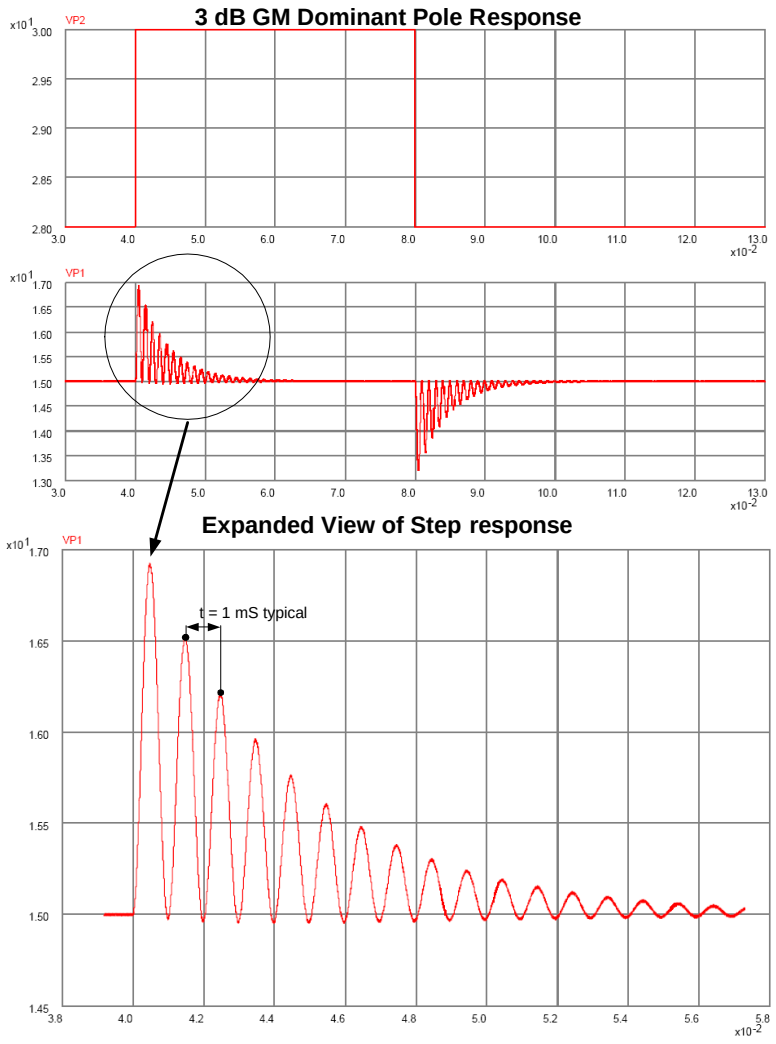

Figure 12: System step response with Vg Disturbance

5 Pole Zero Compensation

5.1 3dB Gain Margin Compensator

To improve the phase margin at the resonant frequency f_0 we can add a zero to the dominant pole compensator at f_0. This provides positive phase shift of $+45°$ to counter the dominant pole and LCR phase lag contributions. The zero begins contributing positive phase shift at $\frac{f_0}{10}$ and contributes $+90°$ by $10f_0$.

Next we determine the appropriate loop gain to provide 3dB of gain margin. Because the LCR dominates the shift of phase and the Bode plot shape of the $G_{vd}(s)$ is approximate near f_0, we will assume the zero phase margin point remains at f_0. Further, the addition of a zero at f_0 does not affect the Bode magnitude at the zero corner frequency. Thus, the gain of the feedback loop does not need to change from our prior calculation for a dominant pole compensator. The open loop magnitude and phase Bode plot is drawn in figure 13. The MATLAB evaluation is shown in figure 14.

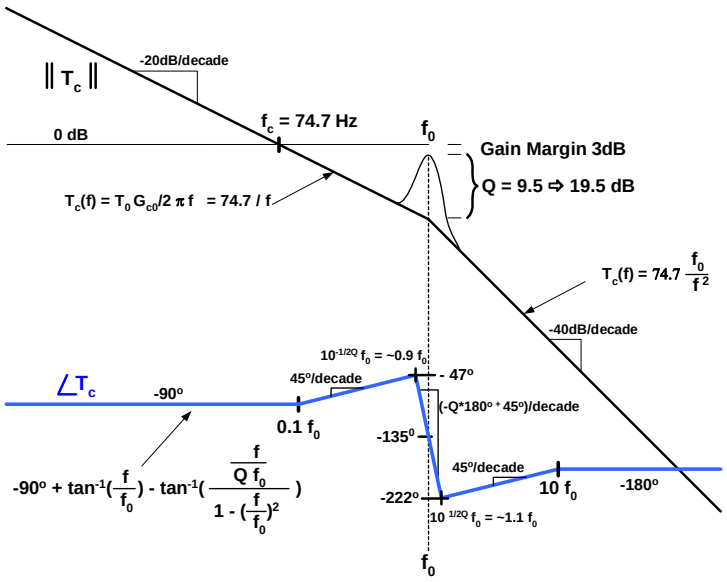

Figure 13: System Gain and Phase Plot with Dominant Pole and Zero Compensation (3 dB GM)

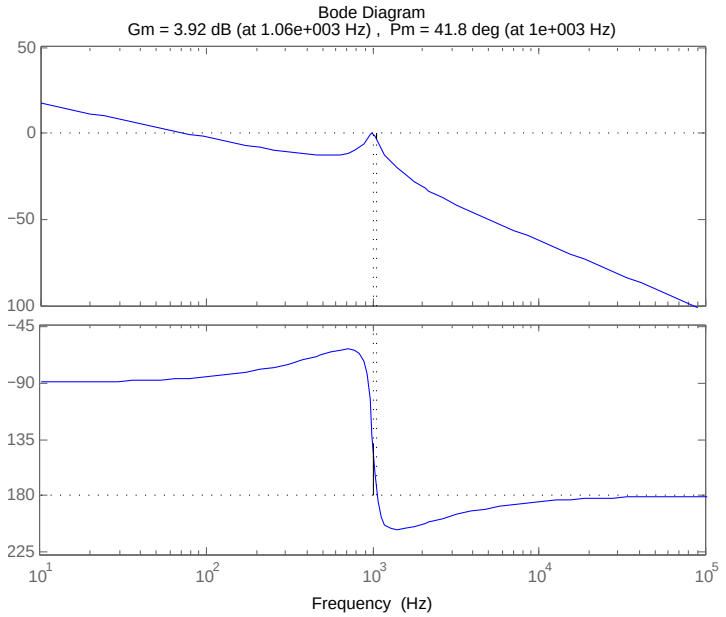

Figure 14: MATLAB pole-zero Bode plot 3dB gain margin

The pole-zero design was simulated using PECS to determine sensitivity to V_g. Figure 15 is the schematic diagram used in the simulation. Figure 16 shows the simulation results from a V_g step between 28V and 30V.

5.2 10dB Margin Compensator

To explore the effect of the size of gain margin, we increased the gain margin to 10 dB. This requires that the loop gain be reduced by 7dB from our prior analysis of the pole zero compensator. For the 3dB gain margin case, an additional 46.1dB of gain was added to the loop. To get a 10dB gain margin this additional gain is reduced to 39.1dB or a gain of 90. The resulting open loop Bode plot is shown in figure 17. The MATLAB evaluation is shown in figure 20.

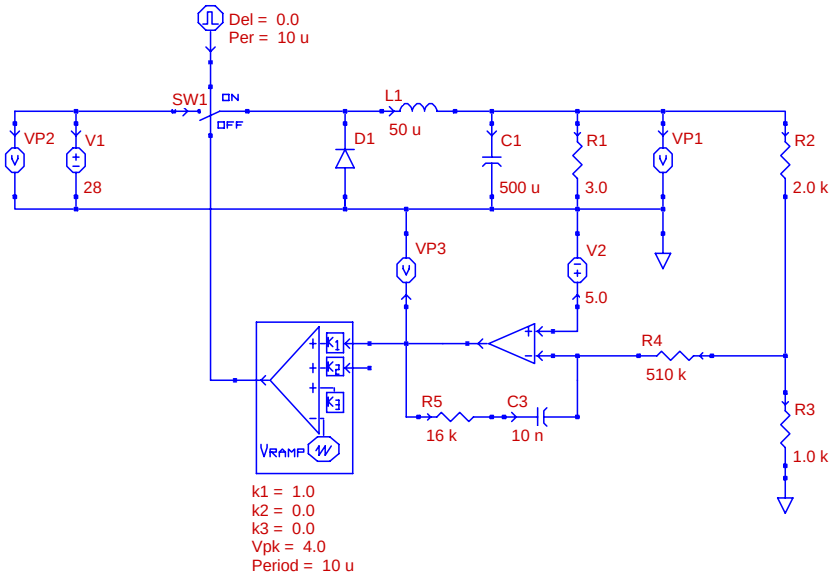

Figure 15: Schematic with Dominant Pole and Zero Compensation (3 dB GM)

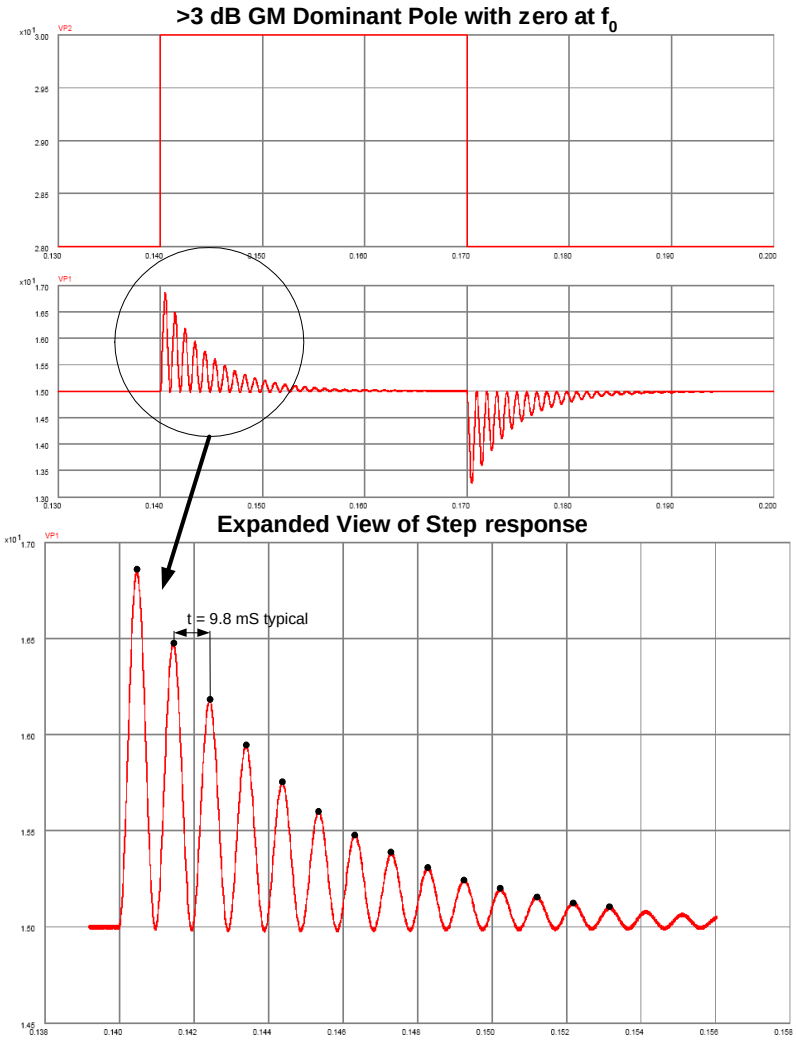

Figure 16: System response with Vg Disturbance (3 dB GM)

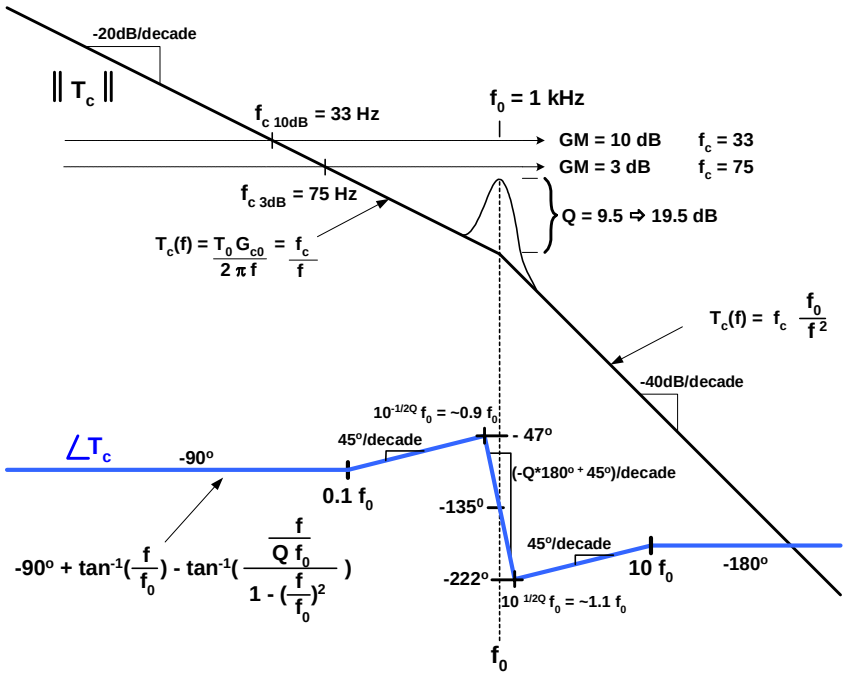

Figure 17: Open Loop System Gain and Phase with pole-zero Compensation (10dB GM)

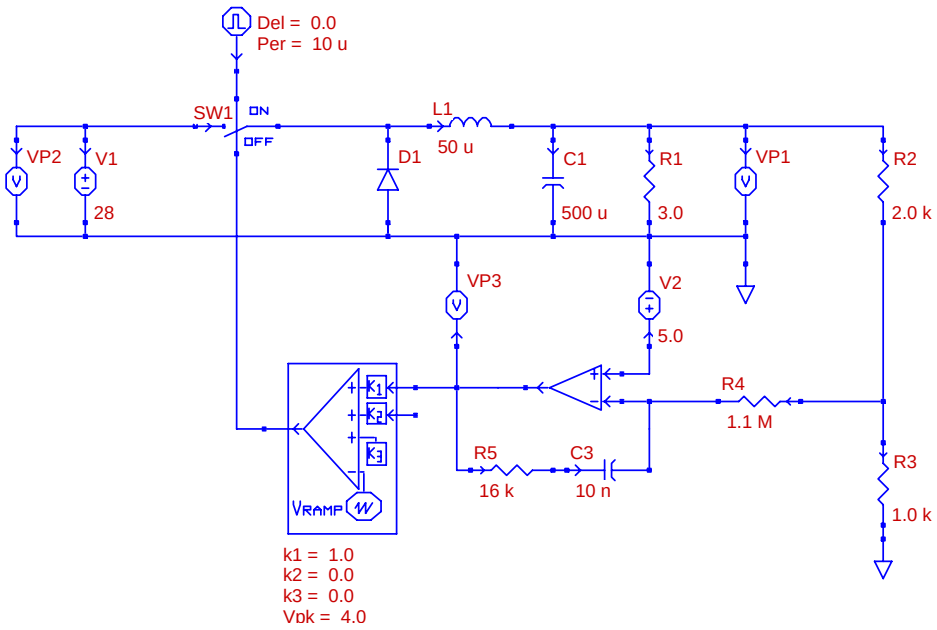

Figure 18: Schematic with Dominant Pole and Zero Compensation (10 dB GM)

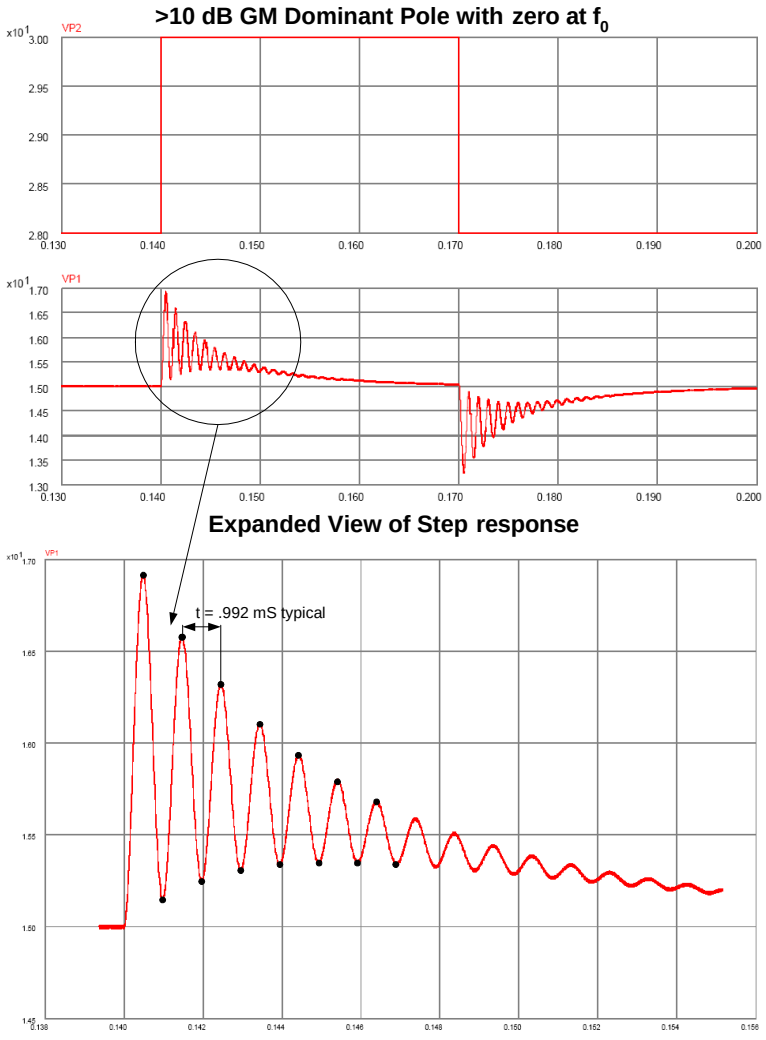

Figure 19: System response with Vg Disturbance (10 dB GM)

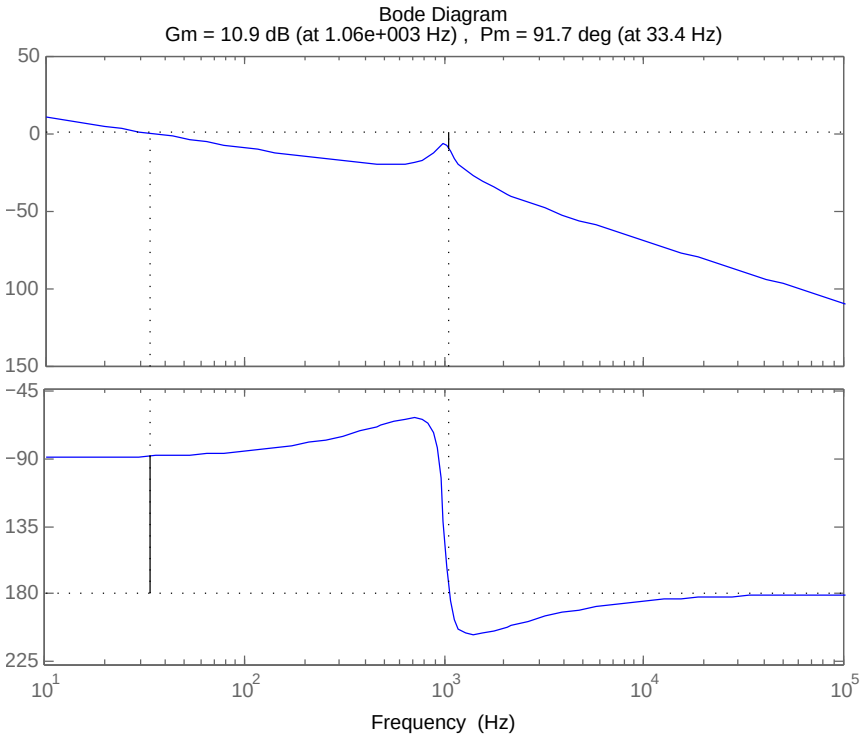

Figure 20: MATLAB pole-zero Bode plot 10dB gain margin

6 Other methods and approaches

While the previous methods are stable and provide good DC results, they yield poor rejection of the output stage resonance and generally a prolonged overshoot response to transient disturbances. So to approach these issues a modified strategy was selected by introducing a second zero at the resonant frequency f_{z1}. The goal of this approach was to further improve phase margin and significantly increase the open loop unity gain crossover frequency to greater than f_0 to optimize the compensator's ability to eliminate these performance limitations.

In the diagram in figure 21, the initial design choice is to place one zero at f_0 and one at $f_0/10$. This reasoning is derived from inspection of the asymptotic plot that shows the 90° phase improvement of the first zero is fully realized when $f = f_0$, and the majority of the phase correction will be completed before the rapid $-180°$ drop due to the LC resonance. The zero also needs to be placed as close to f_0 as possible so that the open loop magnitude response is maintained as high as possible. This result was also checked with MATLAB these phase and gain margin plots in figure 22.

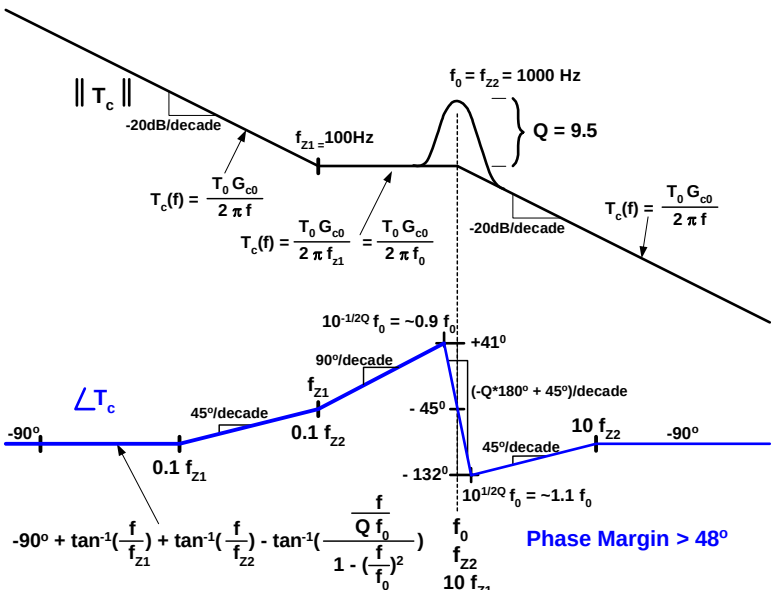

Figure 21: Open Loop System Gain and Phase with Dominant Pole and Zero Pair Compensation

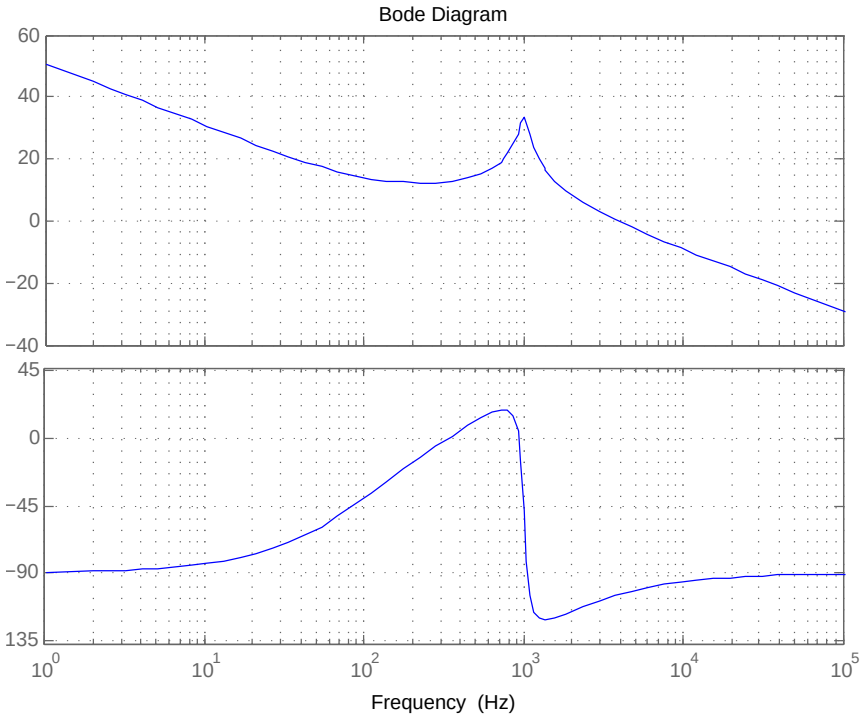

Figure 22: MATLAB Gain and Phase Margin plots Dominant Pole and Zeros at 100 and 1 kHz

In the MATLAB gain plot in figure 23, the magnitude response T is included with a graph of $\frac{1}{1+T}$ to show the effectiveness of the modified compensator. The plot shows the increase in excess gain that extends to $f_c = 3.86$ kHz. This plot also shows that the high Q resonance of the power conversion section also contributes extra gain to help minimize the resonant effects.

To realize this compensator design, we first need to examine the compensator circuit model and further consider second order effects that occur when interfacing with other parts of the circuit. Fortunately a single Inverting Operational Amplifier gain stage will also provide the basis for this design. First consider the general model in figure 24.

In the design that follows the impedance of the $H(s)$ divider network is included to provide a more complete assessment of the effect of the circuit realization. In the comparative PECS designs that were evaluated this finite source

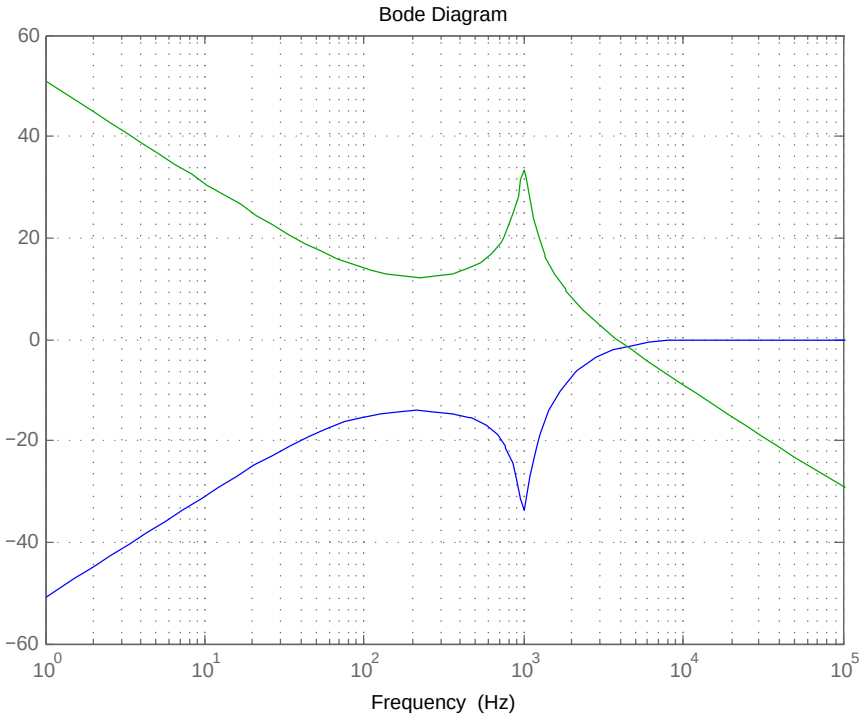

Figure 23: MATLAB Gain plots for T and $\frac{1}{1+T}$ Dominant Pole and Zeros at 100 and 1 kHz

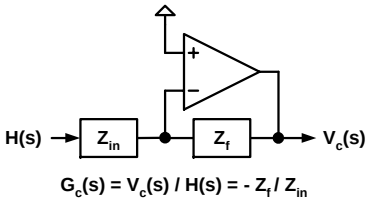

Figure 24: Single stage Compensator General Gain Model

impedance was found to add some significant degradation of the transfer characteristics. So the low source impedance approximation was eliminated. To address this and optimize results the $H(s)$ divider is transformed to a complex

impedance form and used as part of the compensator network. This allows that the idealized transfer characteristic can be achieved with no increase in components and no wasted power in low impedance dividers.

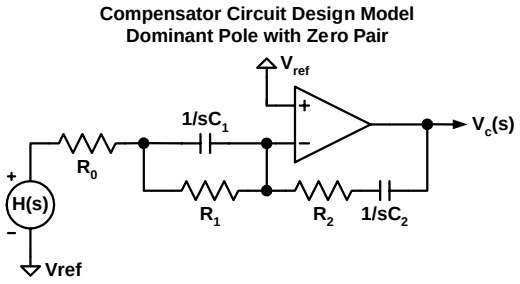

Figure 25: Compensator Circuit Design Model Dominant Pole with Zero Pair

$$Z_f = R_2 + \frac{1}{sC_2} \tag{6}$$

$$Z_{in} = R_0 + (\frac{1}{sC_1}||R_1) = R_0 + (sC_1 + \frac{1}{R_1})^{-1} \tag{7}$$

$$\frac{Z_f}{Z_{in}} = \frac{(sR_1C_1 + 1)(sR_2C_2 + 1)}{s(R_0 + R_1)C_2 + s^2R_0R_1C_1C_2} \tag{8}$$

If $R_0 \ll R_1$ and R_2, then

$$\frac{Z_f}{Z_{in}} \cong= (\frac{1}{R_1C_2s})(sR_1C_1 + 1)(sR_2C_2 + 1) \tag{9}$$

This reduces to the form of two zeroes, one at $\frac{1}{R_1C_1}$ and the other at $\frac{1}{R_2C_2}$ which is multiplied by a Pole with gain $\frac{1}{sR_1C_2}$.

For the initial design let

$$\frac{1}{R_1C_1} = 2\pi f_{z2} = 2\pi 1000Hz \tag{10}$$

$$\frac{1}{R_2C_2} = 2\pi f_{z1} = 2\pi 100Hz \tag{11}$$

In the step response plots shown in figures 27 and 28, the output of the compensator is labeled as VP3 and is included to show that the 0 to 4V input range of the Modulator is not exceeded. The two plots show a 2 V step from 28-30-28 V similar to the previous design examples and also a 12V step 28-40-28 to better demonstrate the large signal behavior of this design.

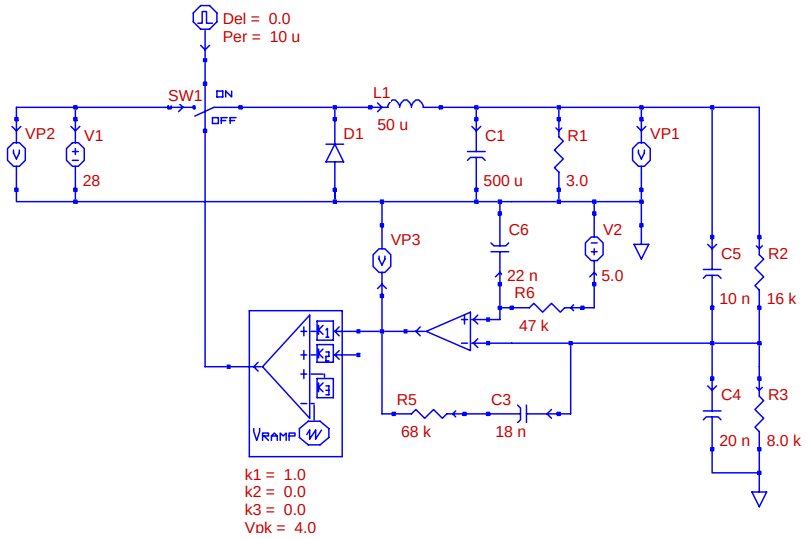

Figure 26: Schematic with Dominant Pole and Zero Pair Compensation $> 48°$ PM

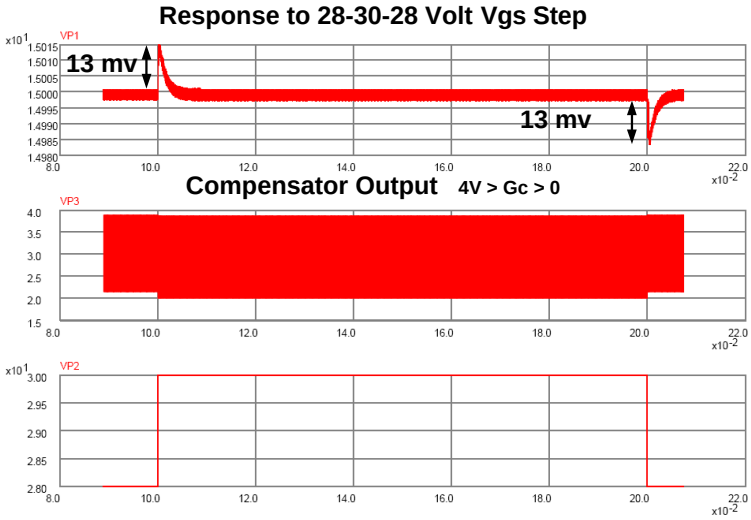

Figure 27: Dominant Pole with Zero Pair System response with V_g Disturbance

The material presented in section 6 demonstrates that the performance can be greatly enhanced by optimizing the compensator design. The DC errors and the

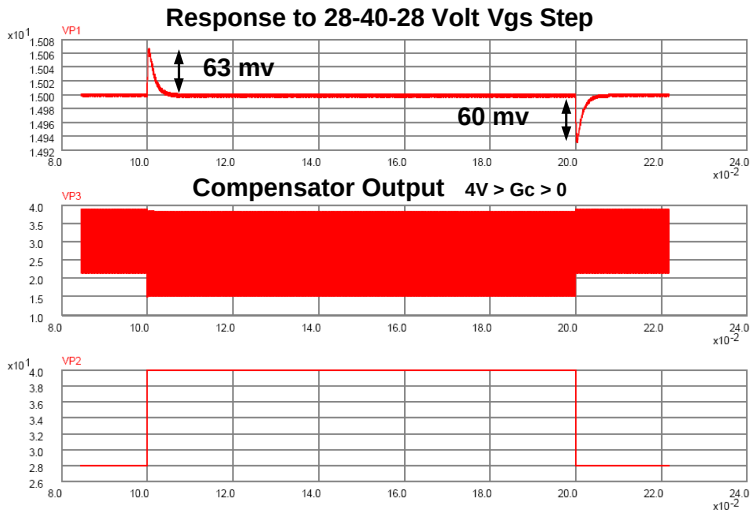

Figure 28: Dominant Pole with Zero Pair System response with V_g Disturbance

power converter resonance have essentially been eliminated and the disturbance recovery time has increased substantially. This is primarily due to improving the feedback effectiveness by extending the unity gain crossover frequency as high as possible, well above f_0 and the internal loop resonance. The component cost for this design is essentially equal to the other compensation methods discussed in this paper.

The design just presented can be further improved by using MATLAB plots showing more precise phase margin information and showing that f_{z1} can position from 100 to at 250 Hz and still maintain greater than 52° of worst case phase margin. Other design improvements can be shown, but a realistic system design also needs to account for component tolerances that establish boundaries for design sensitivity.

7 Conclusion

Key Points from this study: The Buck regulator power converter section has an inherently resonant second order transfer function derived from the inductor and capacitor in the final output stage. These storage elements present a sharply resonant response when excited by a step change in load current or input voltage. This is especially true of high efficiency designs which usually try to avoid losses by selecting idealized components, and it is actually these very desirable characteristics that produce the high Q behavior. The compensator designs covered in this paper need to correct for not only for the large DC error but also the ringing associated with the highly resonant output components. The ringing frequency and damping are directly related to the natural resonance of these devices and the load resistance as illustrated in section 3 and the expanded details provided in the appendix.

In section 4, the first compensator design uses a single dominant pole which demonstrates the ability to minimize the DC error with nearly infinite excess gain provided by the pole at zero frequency. The dominant pole compensator was shown to be capable of providing a stable closed loop response and very low DC error. However, to ensure stability in this design example with $\approx$3 dB of desired gain margin, the compensator requires a significantly low unity gain crossover frequency ($f_c = 75$ Hz). This is well below the natural resonant frequency ($f_0 = 1000$Hz) of the Power Converter output section. Because of this constraint, there is no excess loop bandwidth at f_0 with which to minimize the power converter natural resonant characteristics. This result is also demonstrated with the dominant pole compensation step response plots that show only a minor reduction of the ringing effects as compared with the original uncompensated error signal in the power converter stage.

In section 5.1, the design was enhanced with the addition of a zero at f_0 which was introduced in order to offset the 90° phase shift added by the dominant pole to the 180° phase shift associated with the power converter. The added zero's phase change of +45° at $f_z = f_0$ improves the open loop phase margin at f_0 to $-135°$. While the zero actually increases the gain by +3 dB which would tend to reduce gain margin by 3 dB at f_z, but the net effect is that the gain margin is actually improved to >3 dB because of the increase in frequency at which 180° of total phase shift occurs. The MATLAB plots in section 5 demonstrate the gain and phase margin improvements for this case.

For the >10 dB Gain Margin requirements, a further reduction in unity gain crossover frequency to $f_c = 33$ Hz is required as shown in the asymptotic plots. While the available open loop gain above 0 dB is further reduced with lower f_c, it is interesting to note that the damping of the output stage high Q resonance has actually improved. This is shown qualitatively by inspection of the step response plots and some further analysis is shown in the appendix to help quantify this.

Unfortunately with the added zero in both design cases (>3 dB and >10 dB GM), the system responses have low unity gain crossover frequencies which are well below the 1000Hz natural resonant frequency of the power converter stage. Hence no significant reduction of this error is achieved using this type of compensator design.

To improve the performance further, it is critical to move the unity gain cross over frequency to a value significantly higher than f_0. And in section 6 a new design is proposed which adds two zeros to the dominant pole design. Initially one zero is placed at $f_{z1} = 100$ Hz and the other at $f_{z2} = 1000$ Hz. The effect of the additional 90° of phase improvement at $f_0 = 10f_{z1}$ allows greater than 48° of phase margin over the entire frequency region of interest. This enables the unity gain crossover point to be adjusted higher and extend well beyond the power stage's natural resonance frequency f_0.

In the final open loop gain profile, it can be seen that the resonance peaking actually contributes extra open loop gain at these frequencies that are needed to further reduce the resonance error. The extra open loop gain realized with a higher unity gain crossover frequency f_c also enhances the step response recovery time and minimizes amplitude error to the reference power supply step change used to characterize the time response. It is shown that the new design in this section demonstrates the desired DC accuracy, provides a significant reduction of the loop resonance errors at f_0, and provides significant improvement in recovering from a loop disturbance.

The asymptotic plots were used to characterize the effects of different components in the system and they helped provide an improved understanding and a versatile tool for mapping the system response and compensation planning. In addition, the PECS time domain simulation software preformed well as a notable learning tool. It was invaluable not only for design verification, but it also provided a quick method to enhance the "art" of design. The tool provided a quick and fairly easy to use feedback method which provided reinforcement and helped to develop an intuitive feel for the trade-offs between various alternative methods for design.

References

[**1**] Richard Tymerski, PECS Simulator ©1999-2009, Portland, Oregon,tymerski@ece.pdx.edu

[**2**] MATLAB, ©1984-2007, The MathWorks Inc., www.mathWorks.com

[**3**] Robert W. Erickson and Dragan Maksimovic, Fundamentals of Power Electronics Second Edition. Springer Science+Business Media, LLC, 233 Spring Street, New York, NY 10013, USA, 2001.

Appendix

7.1 Dominant Pole Plot Contributions

Figure 29 shows the Dominant Pole Compensator $G_c(f)$ superimposed on the uncompensated loop $T_u(f)$. Since the vertical axis is log magnitude and dimensioned in dB, this figure shows a graphical construction method for design of the required compensator with an additive offset that produces the final open loop gain required to meet the specified 3 dB Gain Margin at $f_0 = 1$ kHz.

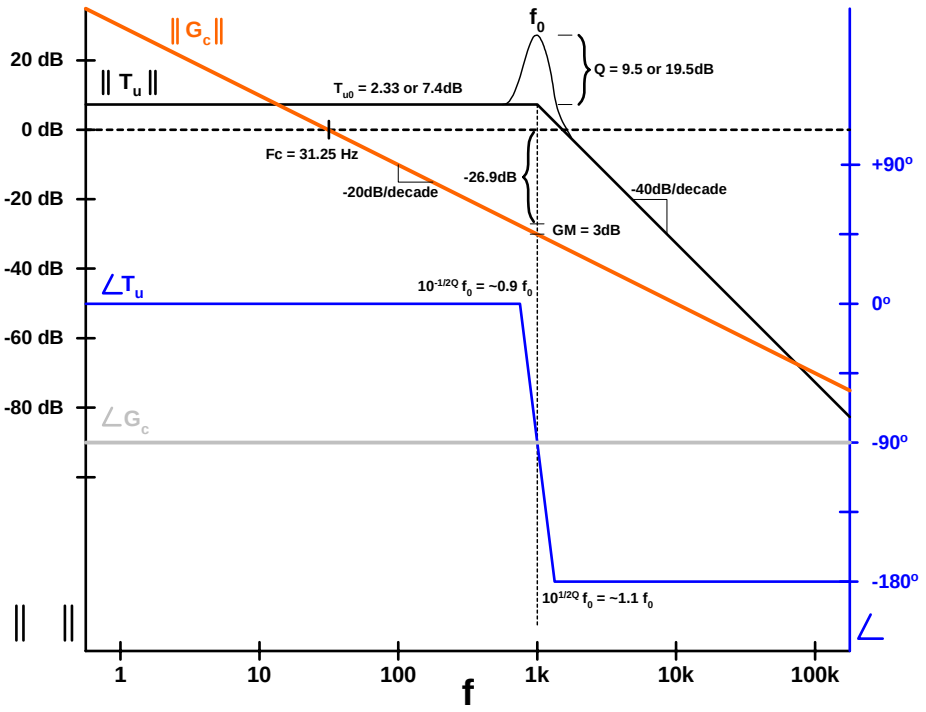

Figure 29: Dominant Pole Compensator Graphical Construction Plot for 3 dB GM

7.2 G_{vd} Step Response Resonance and Damping Analysis

Schematic figure 30 for testing Power converter response with fixed duty cycle and 2 V step input on V1 from 28 to 30 to 28 V.

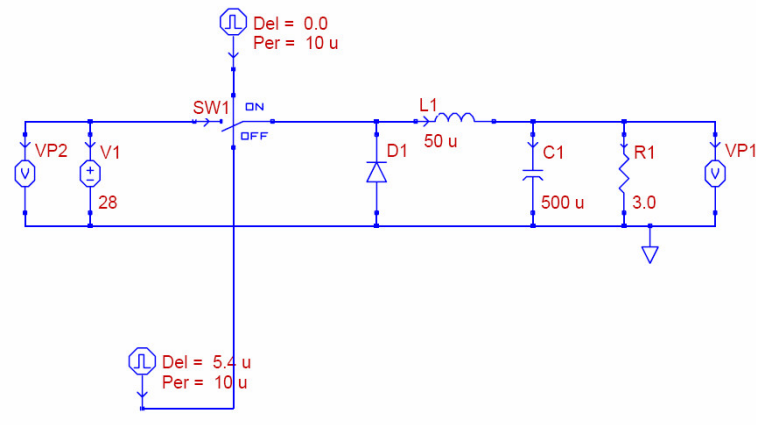

Figure 30: Open Loop Test Schematic for Power Converter Step Response

The step response for the open loop power converter is shown in figure 31. This is a PECS simulation plot using a fixed duty cycle and step change in Vg from 28 to 30 to 28 volts.

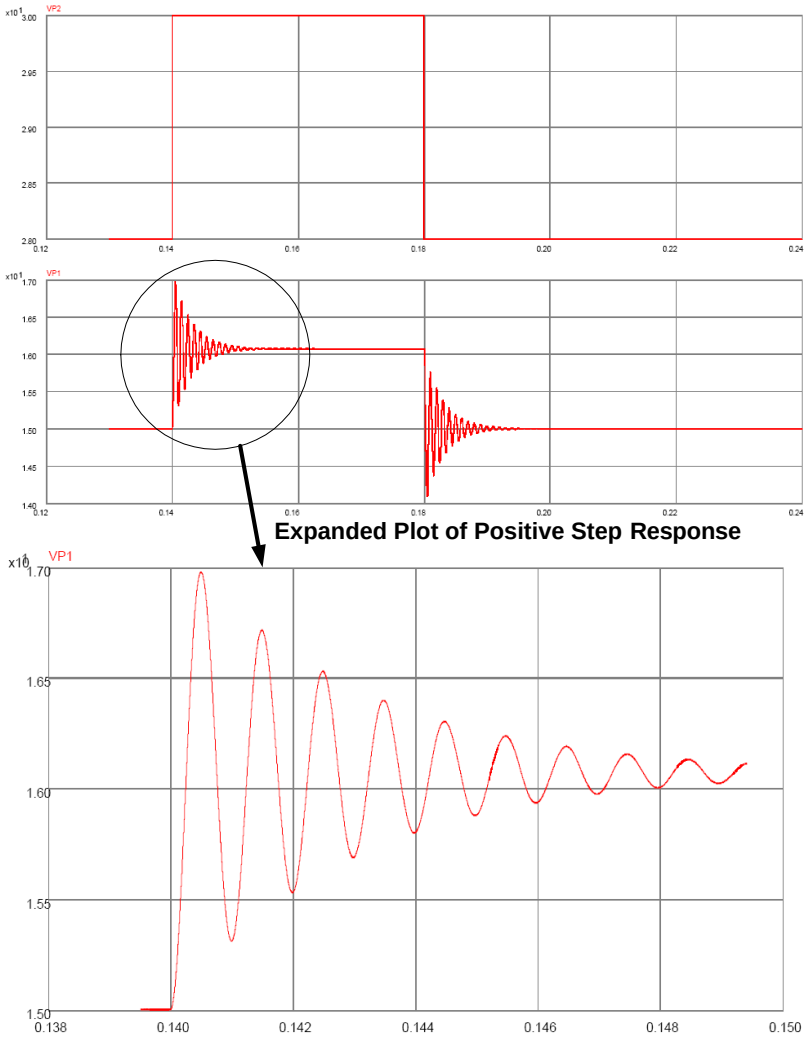

Figure 31: System step response with Vg Disturbance

The peak samples from the open loop power converter response plot in figure 32 are graphed and plotted versus the idealized LRC transfer function and the input stimulus. The reference data was taken using PECS simulation plot data. This graph shows open loop resonance error and is used as a reference for other damping measurement and the effects of negative feedback and phase margin on resonance damping.

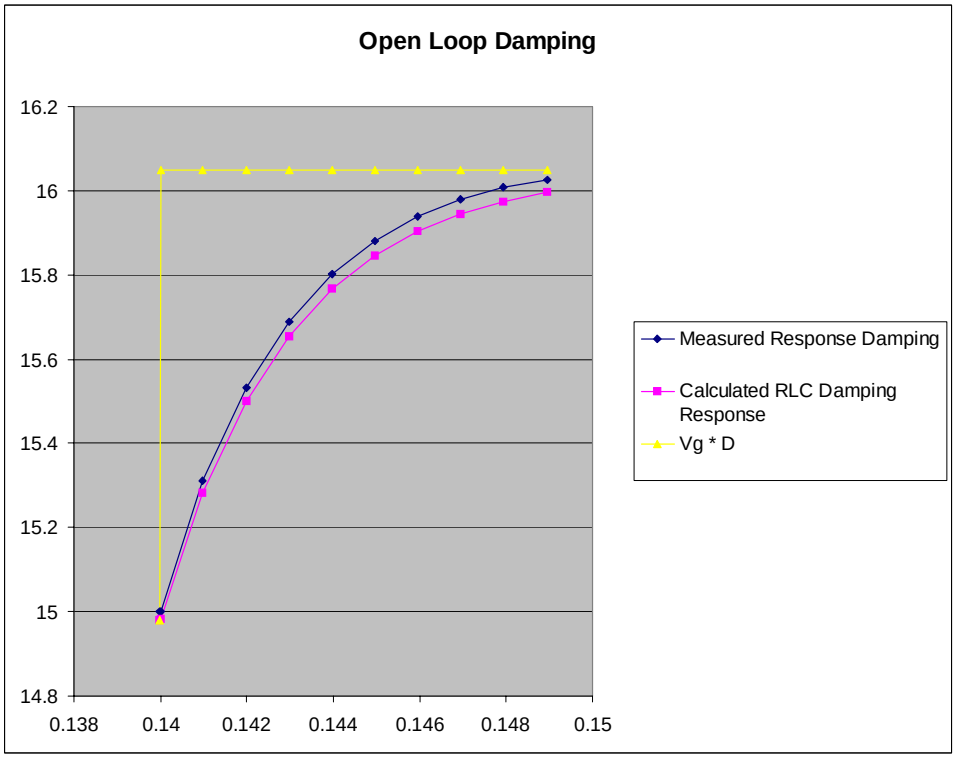

Figure 32: Power Converter G_{vd} Damping Test Data

7.3 Transient and Damping Analysis for pole-zero with 3dB GM

The step response for the closed loop design using a dominant pole and zero with >10 dB gain margin is shown in figure 33. This is a PECS simulation plot of the output voltage with a step change in Vg from 28 to 30 to 28 volts.

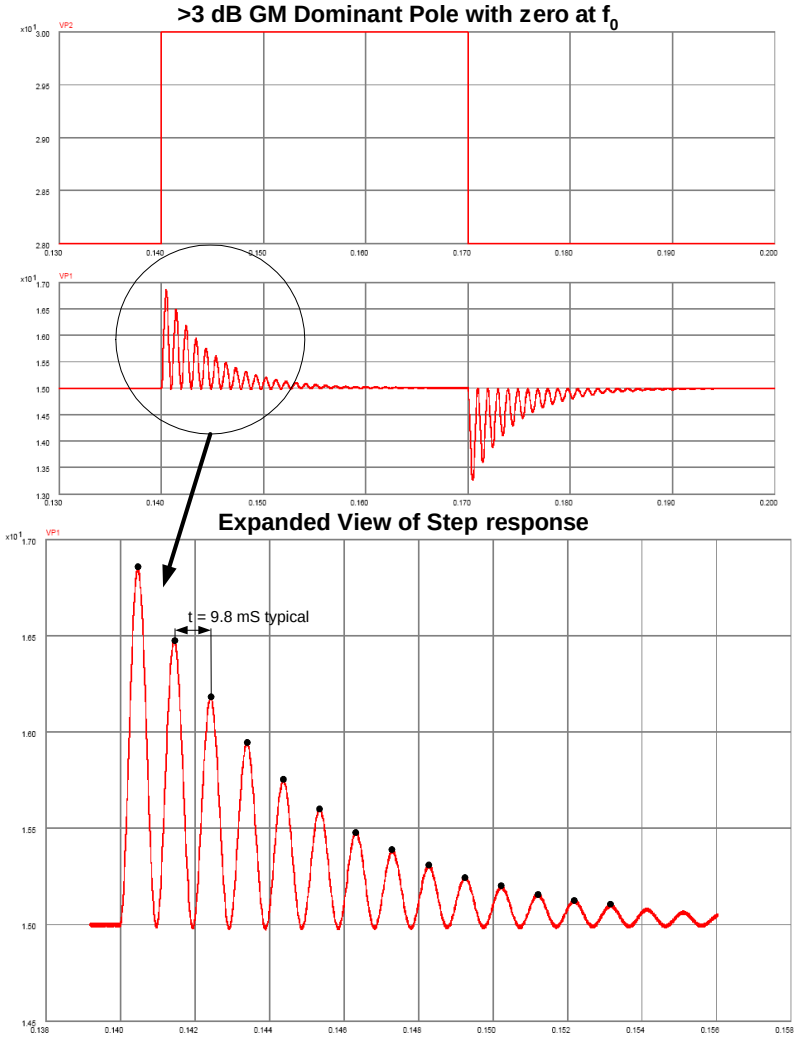

Figure 33: System step response with Vg Disturbance

The peak samples from the closed loop system response plot in figure 34 are graphed and plotted versus the idealized LRC transfer function and the input stimulus. The reference data was taken using PECS simulation plot data. This graph shows closed loop resonance error and is used as a reference for damping measurement and the effects of negative feedback and phase margin on resonance damping.

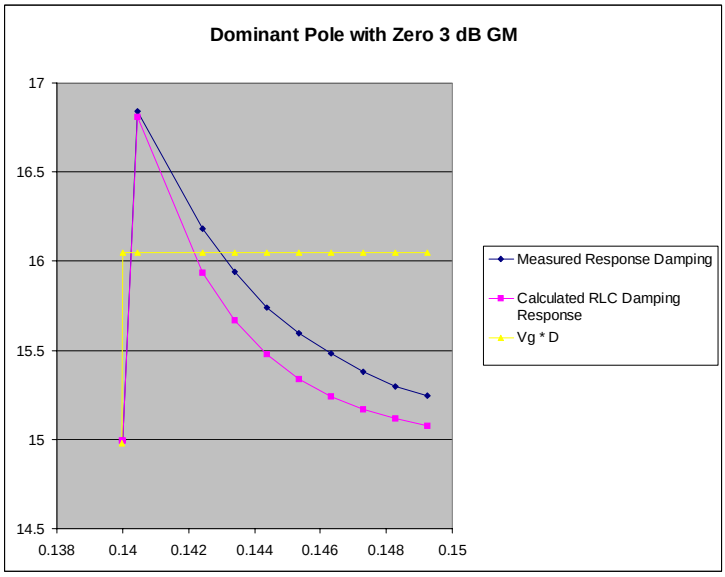

Figure 34: Closed Loop Damping Performance pole-zero with 3dB GM

7.4 Transient and Damping Analysis for pole-zero with 10dB GM

The step response for the closed loop design using a dominant pole and zero with greater than 10 dB gain margin is shown in figure 35. This is a PECS simulation plot of the output voltage with a step change in Vg from 28 to 30 to 28 volts.

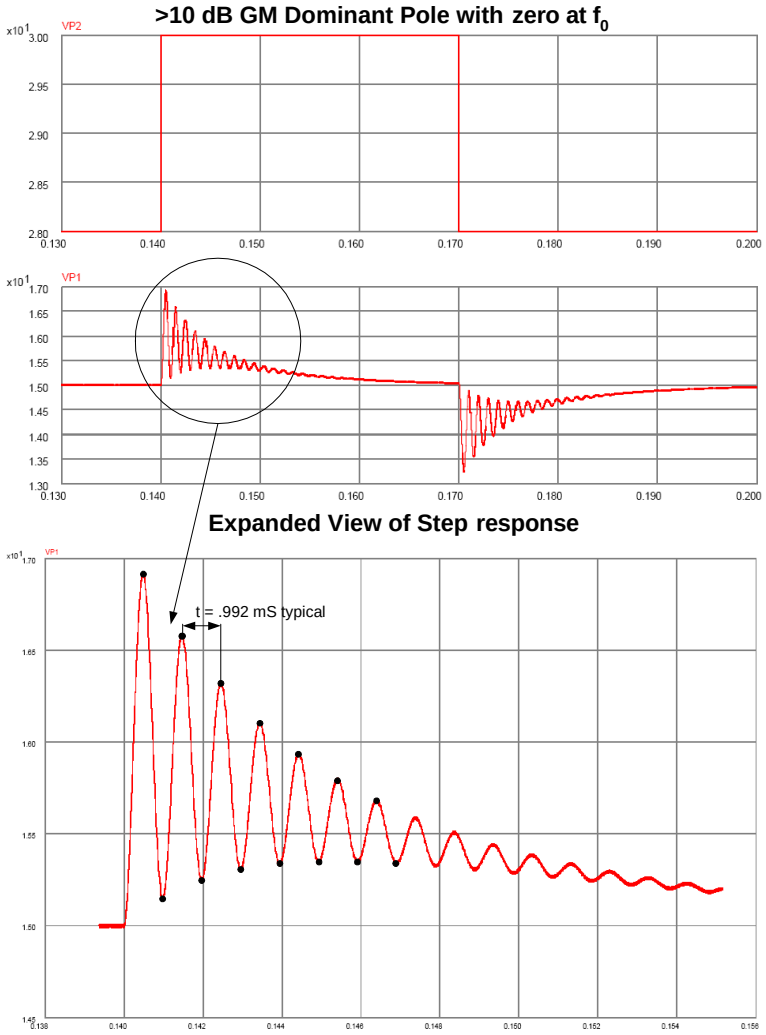

Figure 35: System step response with Vg Disturbance

The peak samples from the closed loop system response plot in figure 36 are graphed and plotted versus the idealized LRC transfer function and the input stimulus. The reference data was taken using PECS simulation plot data. This graph shows closed loop resonance error for the case with additional phase margin. It shows that the damping effects are enhanced with additional phase margin even when the excess gain margin is reduced as compared with the previous >3 dB GM case. This is useful because it shows important effects of negative feedback and phase margin on resonance damping.

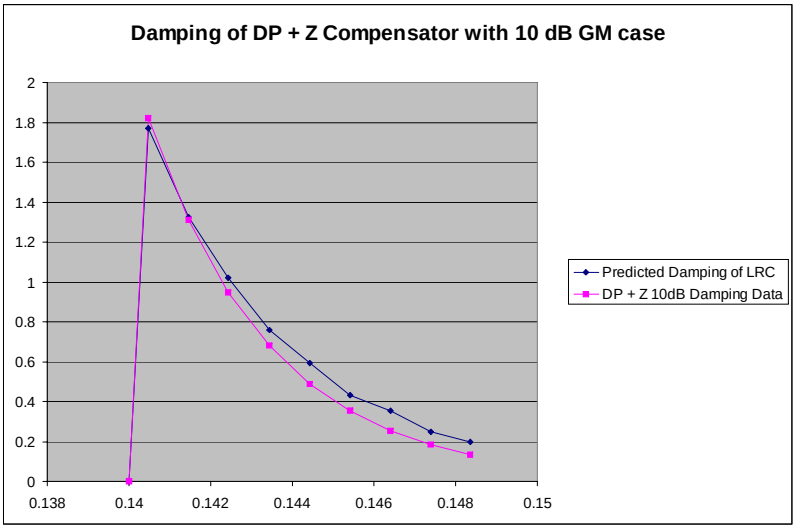

Figure 36: Closed Loop Damping Performance pole-zero with 10dB GM