Compensators for the Buck Converter: Design and Analysis

Portland State University
Department of Electrical and Computer Engineering
Portland, Oregon, USA

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Abstract

This paper discusses the design of a compensator for the buck DC switching converter. Three different compensators are designed and analyzed based on phase and gain margins. Op-amp implementations for each compensator are derived and tested with an example converter. The performance of the converters is examined based on transient response and rejection of steady-state error due to a step change in the input voltage.

Introduction

The buck converter is perhaps the simplest DC converter topology, yet one of the most useful. It is widely used in industry, it is a clear and simple example that is helpful in understanding the principles of switching converters, and it can be used to derive more complicated topologies. In light of this general usefulness, it is instructive to consider how one can use control systems to regulate the operation of such a converter. This serves not only to illustrate how switching converters can be controlled, but also results in a practical circuit for use in power supplies, voltage regulators, and so forth.

Since it is desirable to design an effective compensator for the buck converter, this paper will consider the various properties of three different compensation schemes. The first section will present a basic discussion of the buck converter, its open-loop and uncompensated closed-loop behavior, and introduce an example converter that will be used for all the designs. The next section will present a basic attempt to counteract some of the undesirable properties of the buck converter with a proportional-integral compensator. The third section will detail a somewhat more sophisticated attempt to improve performance by use of a lead compensator. The last compensator discussed will be the combination of the lead and proportional-integral compensators to obtain the benefits of both.

Each section will present the design of the compensator for the example converter given in the first section, derive an op-amp circuit to implement it, and evaluate the performance of the compensated system through simulation. The conclusion will summarize the results and compare the various designs.

The Uncompensated Buck Converter

The basic buck converter topology is shown in Figure 1. The function of this converter is transform a higher input DC voltage, V_g, into a lower output DC voltage, V. The conversion ratio, in steady-state, is $V = DV_g$, where D is the duty ratio of the switch. Thus, the output voltage is determined by both the input voltage and the switching duty cycle. In addition, non-ideal effects, most notably the discontinuous conduction mode, make the output voltage dependent on the load current. For this paper, however, the controlled variable is considered to be the duty cycle, with variations in the input voltage considered to be disturbances, and the load current assumed to be constant, with the converter operating in the continuous conduction mode. The response of a buck converter operating in steady-state to a step change in the input voltage is shown in Figure 2. In open-loop, the converter exhibits large overshoot, large steady-state error, and excessive oscillations.

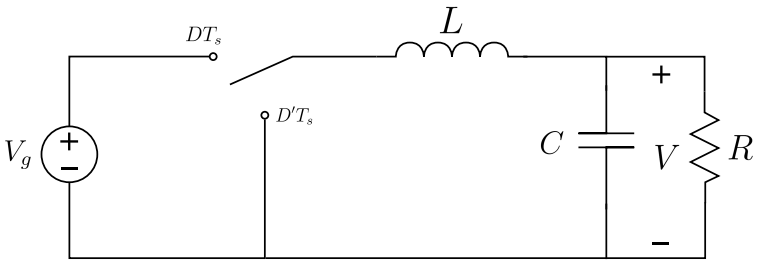

Figure 1: The ideal buck converter

Reference [1], Chapter 8 gives the small-signal averaged transfer function for the operation of the buck converter in the continuous conduction mode. This is the model that will be used in the following analysis. The model basically consists of two transfer functions, one which models the influence of the duty cycle on the output, $G_{vd}(s)$, and one which models the influence of the input voltage on the output, $G_{vg}(s)$. For the purposes of this paper, the first will be considered the control input, while the second is a source of disturbances. The general forms of the these transfer functions are the same.

$$G_{vd}(s) = \frac{G_{d0}}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \text{ and} \tag{1}$$

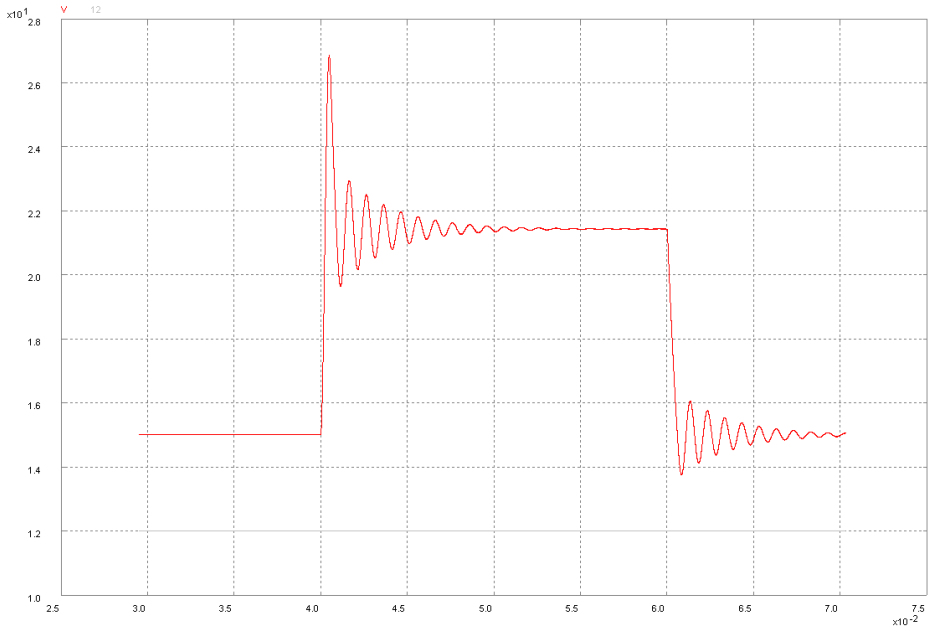

Figure 2: Response of open-loop buck converter to input voltage step

$$G_{vg}(s) = \frac{G_{g0}}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2}\ , \tag{2}$$

where

$$G_{g0} = D, \quad G_{d0} = \frac{V}{D}, \quad \omega_0 = \frac{1}{\sqrt{LC}}, \quad \text{and} \quad Q = R\sqrt{\frac{C}{L}}$$

To correct the undesirable behavior demonstrated in response to a change in the input voltage, the buck converter can be placed in a control loop, as shown in Figure 3, where $H(s)$ is the gain of the output sensor, $G_c(s)$ is the transfer function of the compensator, and the $\frac{1}{V_m}$ factor is the transfer function of the pulse-width modulator used to drive the transistor that implements the ideal switch shown above. Usually, $H(s)$ and $\frac{1}{V_m}$ will be simple gains. One method in classical control theory to analyze systems and design controllers, and the method that will be used here, is by using the loop gain. For the control loop shown in Figure 3, the loop gain is

$$T(s) = \frac{G_c(s)G_{vd}(s)H(s)}{V_m} \tag{3}$$

This paper will use an example converter to illustrate the design and effectiveness of the various compensators. Namely, the converter will have an input

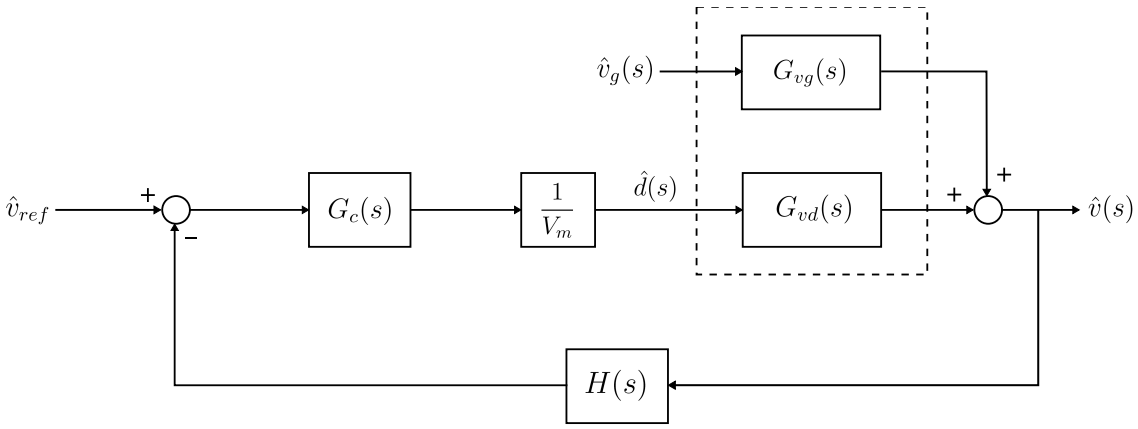

Figure 3: Buck converter control loop

voltage $V_g = 28$ V, an output voltage $V = 15$ V, and a load of $R = 3\ \Omega$. The capacitor and the inductor values will be $C = 500\ \mu$F and $L = 50\ \mu$H, respectively. The peak-to-peak amplitude, V_m, of the sawtooth driving the modulator will be 4 V, the sensor gain will be $H = \frac{1}{3}$ and the switching frequency $f_s = 100$ kHz. The designs will be evaluated based on their gain and phase margins, and on how the converter responds to a input voltage step from 28 V to 40 V and back to 28 V. To have a basis of comparison for the compensated converter, the behavior of the buck in an uncompensated configuration must be examined.

Using the control-to-output transfer function given earlier, these values can be used to derive a more concrete expression for the loop gain. Since the loop is as yet uncompensated, $G_c(s) = 1$.

$$T(s) = \frac{G_c(s)G_{vd}(s)H(s)}{V_m} = \left(\frac{H}{V_m}\right)\frac{G_{g0}}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

As can be seen, the uncompensated loop gain of the buck converter is a standard second-order system of the form

$$T(s) = \frac{T_o}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2}\ , \tag{4}$$

where

$$T_o = \frac{G_{d0}H}{V_m} = \frac{28}{(3)\,(4)} = 2.33$$

$$\omega_0 = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{(50\ \mu H)\,(500\ \mu F)}} = 2000\sqrt{10}\ \text{rad/s} \Rightarrow f_0 = 1\ \text{kHz, and}$$

$$Q = R\sqrt{\frac{C}{L}} = 3\ \Omega\sqrt{\frac{500\ \mu F}{50\ \mu H}} = 3\sqrt{10} = 9.49 \Rightarrow 19.5\ \text{dB}$$

A Bode plot of this loop gain is shown in Figure 4. The phase margin can be determined directly from the plot. In the asymptotic approximation, the closed-loop buck converter has a phase margin of 0°. Since the phase asymptote reaches but does not cross −180°, the gain margin can be said to be infinite. Thus, without any compensator, the buck converter has an infinite gain margin but a 0° phase margin. Such a system is stable but will exhibit oscillations and other behavior that is generally considered undesirable. A plot of the step response of the converter in this configuration is shown in Figure 5. As can be seen, the oscillations in the output voltage present in the open-loop case are still present, though reduced in amplitude by the application of feedback, and there is still a steady-state error to a change in input voltage. Both of these issues will be addressed in the compensator designs that follow.

Proportional-Integral Compensation

A simple but fairly effective way to improve the characteristics of the buck converter is to use a dominant-pole or integral compensator. This is simply a compensator with a single pole at $s = 0$ and a gain.

$$G_c(s) = \frac{G_{c0}}{s} \tag{5}$$

Although the plain integral compensator could be used for this purpose, it is difficult to obtain good performance using this type of compensator. It is more usual to use a proportional-integral or PI compensator, as discussed in Chapter 7 of [2] This is essentially the same as the integral compensator, but with a zero introduced at some higher frequency. The transfer function of the PI compensator is

$$G_c(s) = \frac{G_{c0}\left(1 + \frac{s}{\omega_z}\right)}{s} \tag{6}$$

As can be seen from the plot in Figure 6, this compensator provides a high gain at low frequencies, which falls off at −20 dB per decade and then levels out at the zero frequency, f_z. The phase is initially −90°, which increases by a rate of 45° per decade starting at $\frac{f_z}{10}$ to a maximum of 0° at $10f_z$. The benefit obtained by using a PI compensator is that the large low-frequency gain will eliminate steady-state error to step disturbances. In general, however, this cannot be attained while still having acceptable gain and phase margins using a simple PI compensator. The design shown here will concentrate on low-frequency gain at the expense of gain and phase margins, although these are still a consideration. The unity-gain crossover frequency should be placed before the major phase downturn in the compensated loop. The design here will use $f_z = \frac{f_0}{10} = 100Hz$ and place the unity-gain crossover at this same frequency, to avoid too much interaction in the phase responses while still providing higher gains.

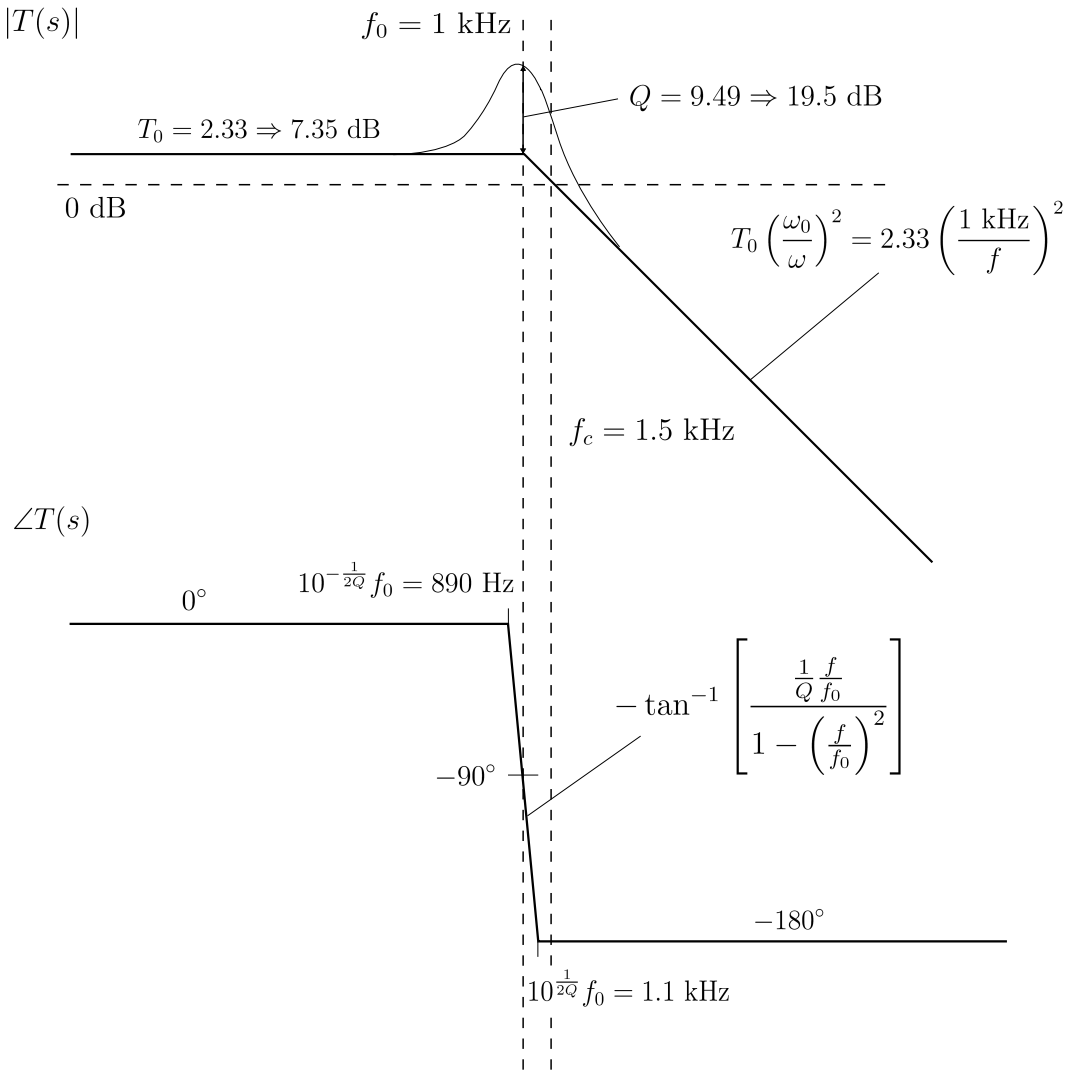

Figure 4: Uncompensated loop gain

The loop gain of the buck converter with the PI compensator is shown in Figure 7, which can be expressed as

$$T(s) = T_0 G_{c0} \frac{1 + \frac{s}{\omega_z}}{s\left(1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right)} \tag{7}$$

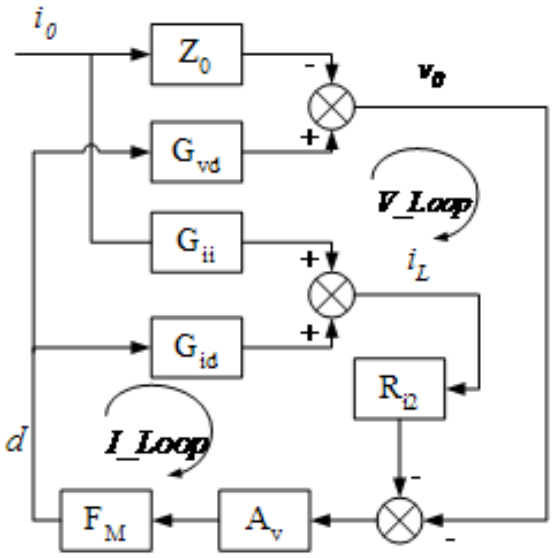

Figure 5: Step response of uncompensated buck converter

Using the expressions given on the Bode plot, the value of G_{c0} can be calculated. To find the low-frequency gain, one can simply use the gain expression at the new crossover frequency.

$$\frac{T_0 G_{c0}}{2\pi f_c'} = 0 \text{ dB} = 1$$

$$T_0 G_{c0} = 2\pi f_z$$

$$G_{c0} = \frac{2\pi\,(100 \text{ Hz})}{2.33}$$

$$G_{c0} = 270$$

Since only G_{c0} and f_z are needed to specify the compensator, the design is complete. The phase margin of this design is the amount by which the phase at the crossover frequency is above $-180°$. This can be found by evaluating the gain asymptote at f_z.

$$\phi_M = 180° + 45° \log\left(\frac{f_z}{f_0}\right)$$

$$\phi_M = 180° + 45° \log\left(\frac{100 \text{ Hz}}{1 \text{ kHz}}\right)$$

$$\phi_M = 135°$$

This is actually a surprisingly high phase margin, which is only due to the asymptotic approximation. Due to the Q of the original circuit, the gain will

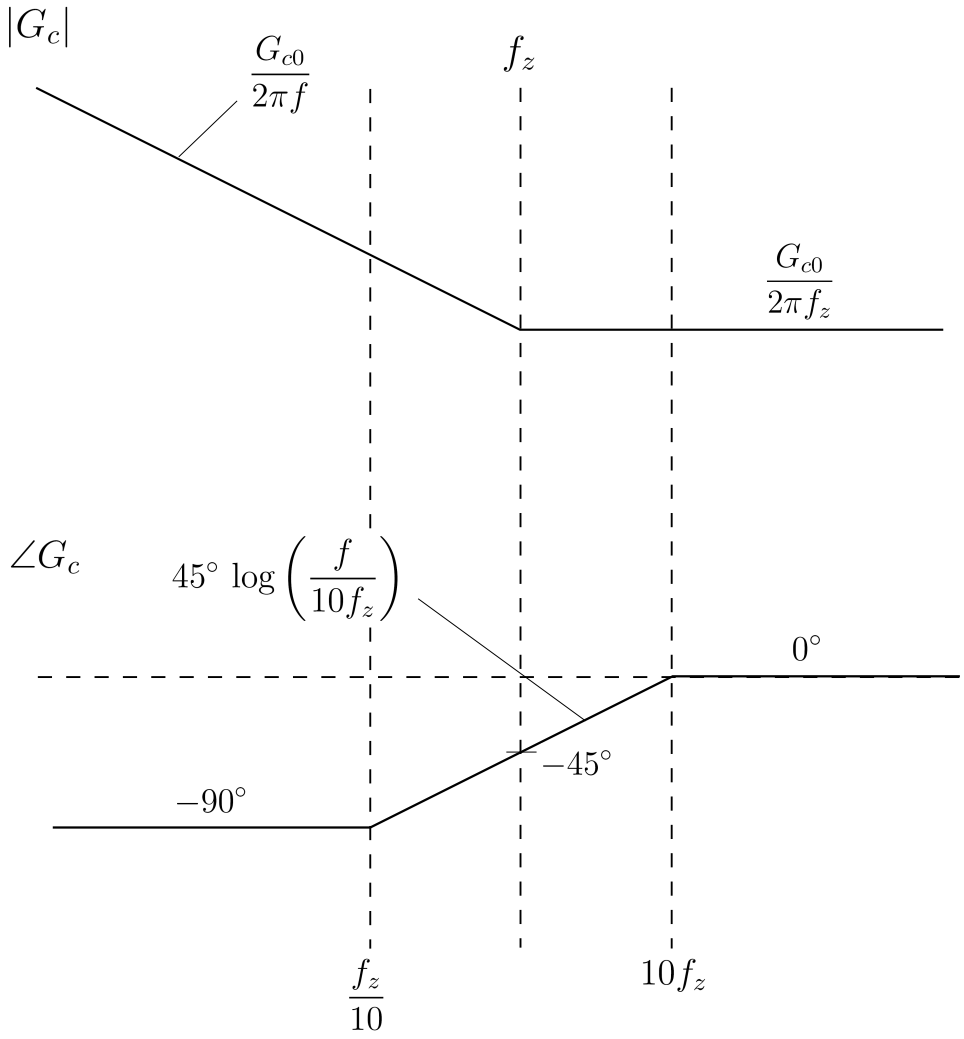

Figure 6: PI compensator transfer function

rise above 0 dB and cross again after the phase downturn, so the actual phase margin is close to 0°. The gain margin, as in the uncompensated case, is actually infinite, since the phase never actually crosses -180°, although the asymptote reaches it. Thus, the PI compensated system has essentially the same gain and phase margins as the uncompensated system, and will show similarly undesirable transient characteristics. The presence of higher low-frequency gain, however,

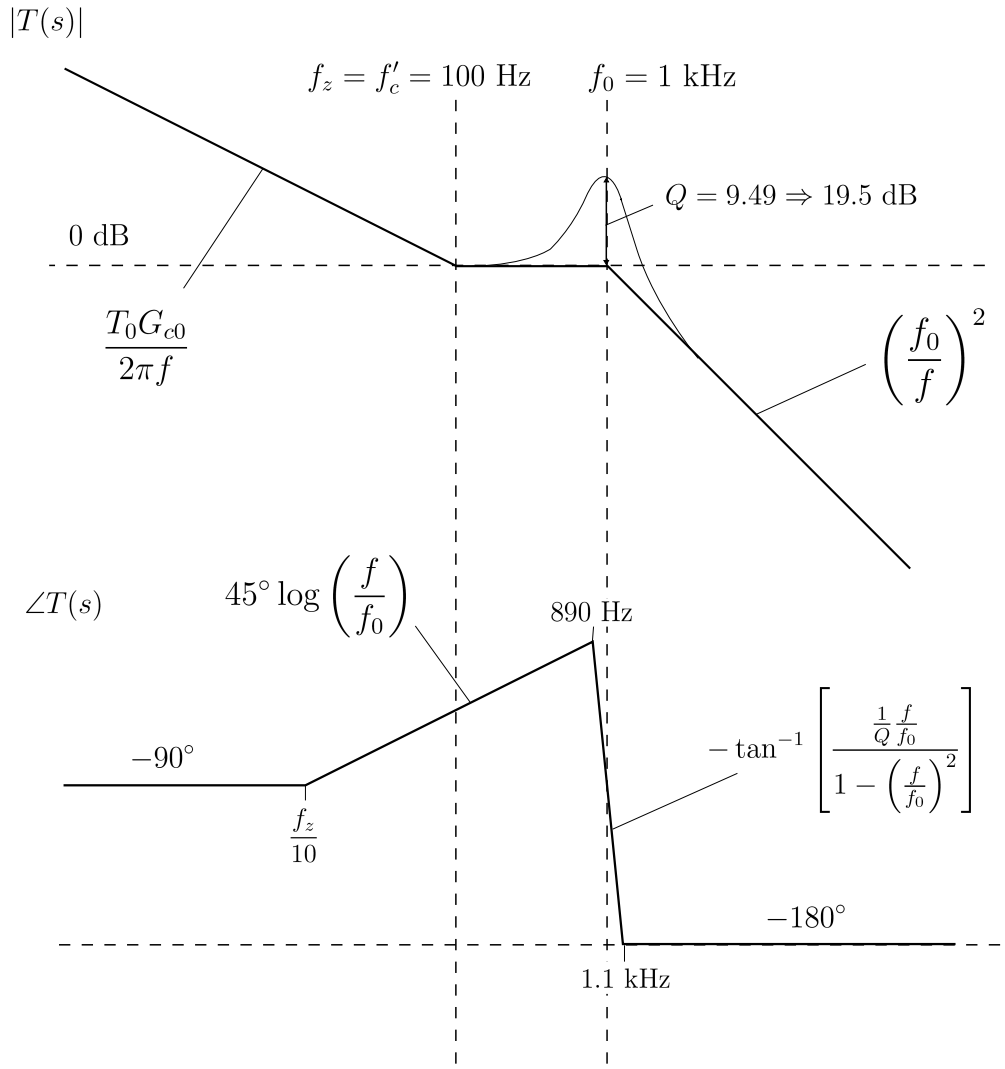

Figure 7: Loop gain with PI compensator

will eliminate the steady-state error seen in the uncompensated case.

To be able to simulate the behavior of the compensated buck converter, a control circuit must be derived to implement the PI compensator. Such a circuit

is shown in Figure 8. This circuit implements the transfer function

$$G_c(s) = -\frac{R_2}{R_1}\left(\frac{R_2Cs+1}{R_2Cs}\right) \tag{8}$$

In this circuit, the second resistor and the capacitor set the zero frequency, while the first resistor in combination with these values sets the gain of the compensator. If a value of $R_2 = 100$ kΩ is assumed, then the capacitor value must be

$$\omega_z = \frac{1}{R_2C} \Rightarrow 2\pi\,(100\text{ Hz}) = \frac{1}{(100\text{ k}\Omega)\,C}$$

$$C = \frac{1}{2\pi\,(100\text{ Hz})\,(100\text{ k}\Omega)} \Rightarrow C = 15\text{ nF}$$

Likewise, the value of R_1 to set the gain to the proper value can be found from this value for C.

$$G_{c0} = \frac{1}{R_1C} \Rightarrow 270 = \frac{1}{R_1\,(15\text{ nF})}$$

$$R_1 = \frac{1}{270\,(15\text{ nF})} \Rightarrow R_1 = 240\text{ k}\Omega$$

The reference voltage on the non-inverting input of the opamp for this circuit can be simply 5 V, since there is no direct connection to the output.

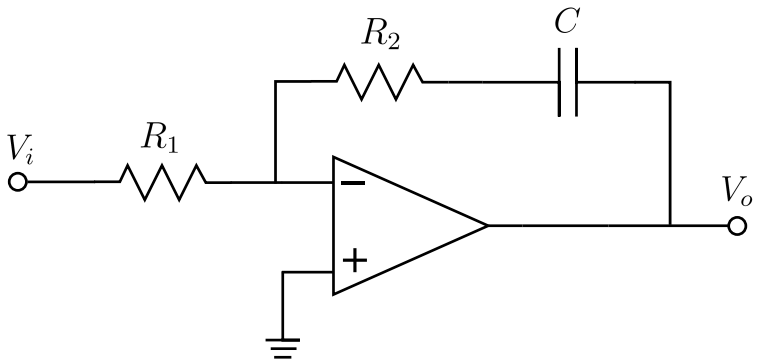

Figure 8: Op-amp circuit implementation of PI compensator

The simulated response of the buck with this PI compensator to a step disturbance is shown in Figure 9. As would be expected from the phase margin, the system displays large oscillations in the output voltage, although not nearly as large as those of the open-loop converter. The presence of the pole at $s = 0$, however, which is the main purpose of using such a compensator, is quite effective in removing steady-state error. Thus, although some of the transient characteristics are undesirable, the PI compensator is effective in regulating the output to the proper voltage. A method to improve the transient characteristics is examined in the design of the next compensator.

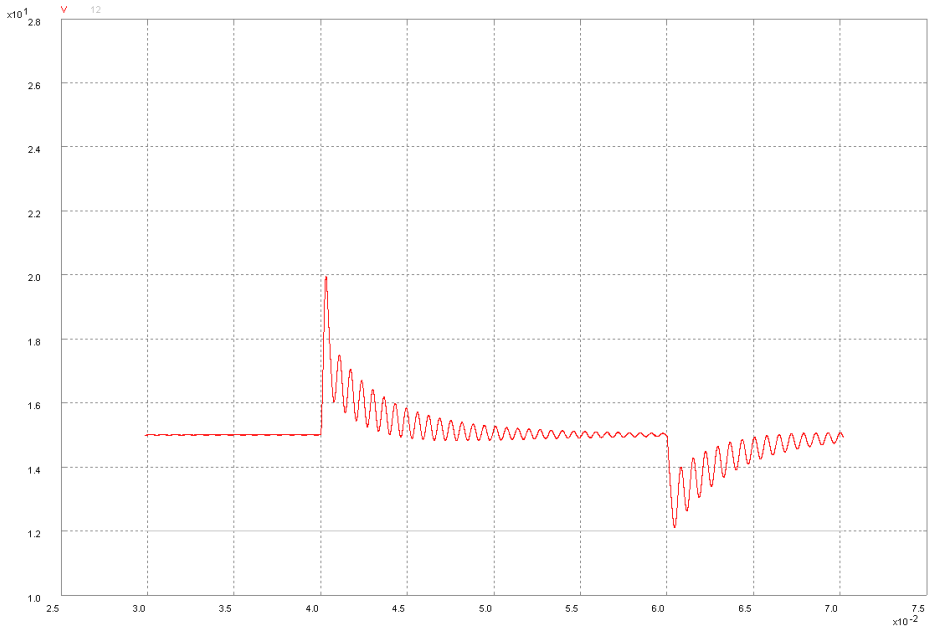

Figure 9: Step response of PI-compensated buck converter

Lead Compensation

A more sophisticated way to improve the performance of the buck converter is with a lead compensator. The transfer function of this compensator is

$$G_c(s) = G_{c0}\frac{\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_p}\right)}\ , \tag{9}$$

where $\omega_z < \omega_p$. As can be seen from the plot of the transfer function shown in Figure 10, the lead compensator provides both a phase boost that is adjustable based on the pole and zero frequencies, and a gain boost at higher frequencies that will result in a higher crossover frequency for the lead-compensated buck converter. Since the one of the most undesirable features of the uncompensated buck is its low phase margin, the phase boost should be chosen to improve the phase margin to an acceptable value. The new crossover frequency can be chosen arbitrarily. The design shown here will be to obtain a 45° phase margin and a crossover frequency of 5 kHz for the loop gain with a lead compensator.

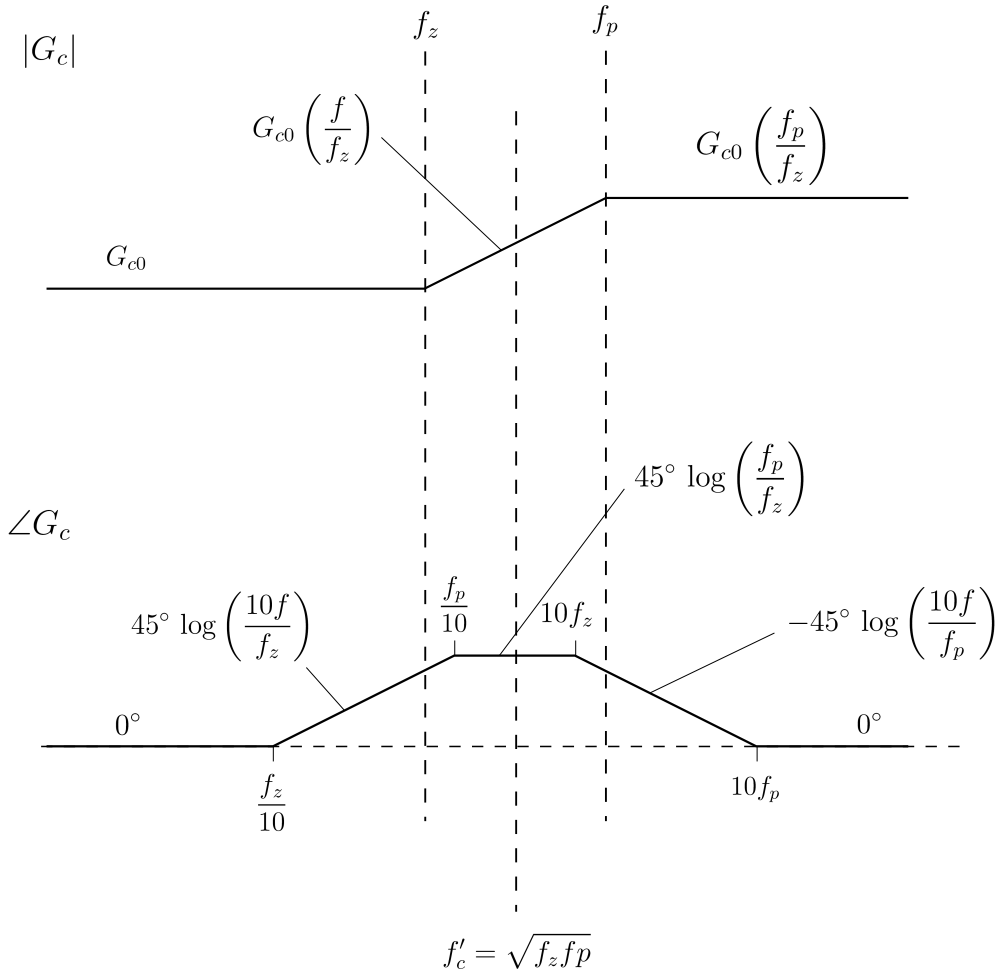

Figure 10: Lead compensator transfer function

When the compensator is placed in the loop, the loop gain of the buck converter system becomes

$$T(s) = T_0 G_{c0} \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)\left(1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right)} \tag{10}$$

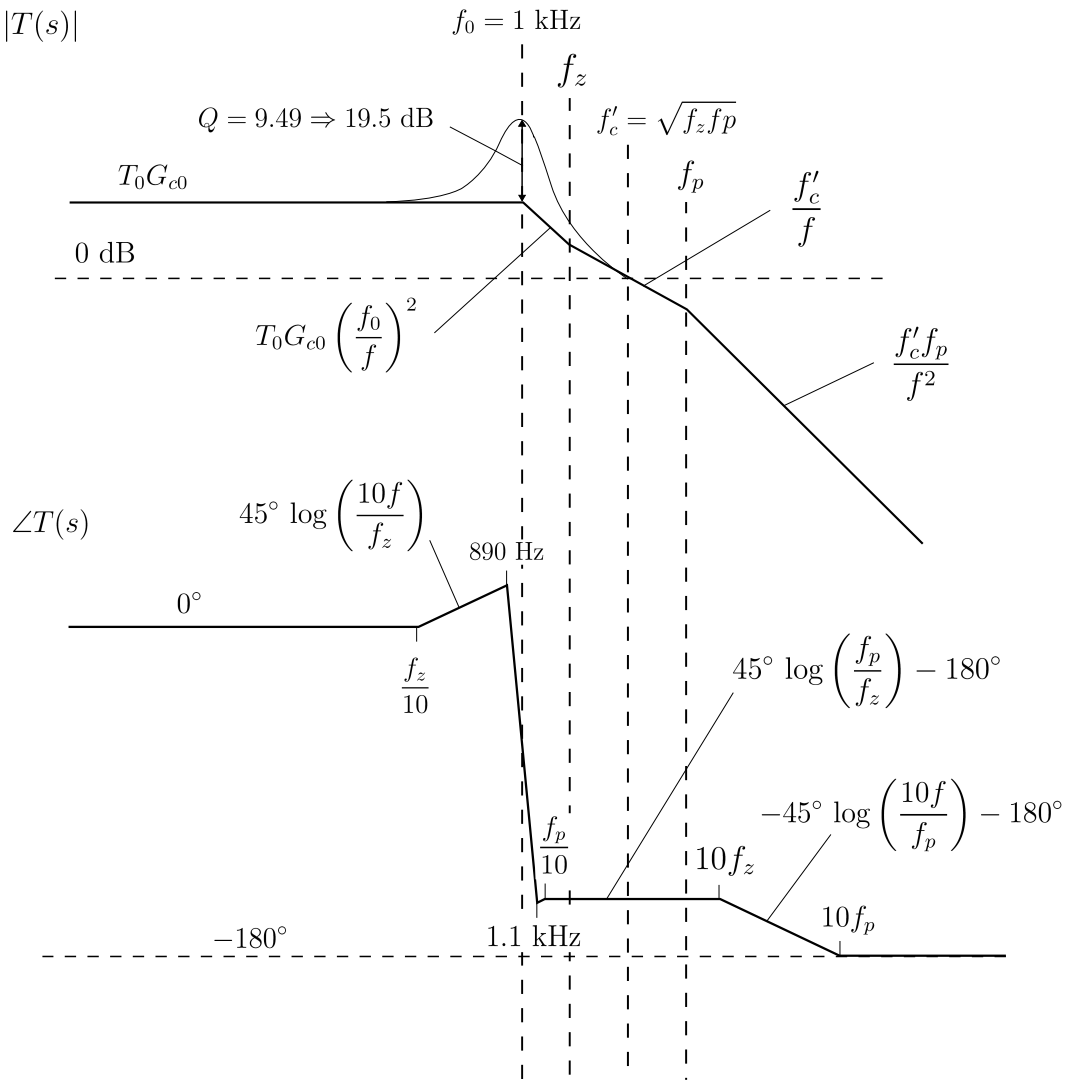

Figure 11: Loop gain with lead compensator

The asymptotic Bode plot of this loop gain is shown in Figure 11. The expressions shown can be used to place the pole and zero frequencies of the compensator to obtain the desired phase margin and unity-gain crossover. As can be seen, the phase margin of the system is equal to the phase of the lead compen-

sator at the new crossover frequency, f_c'.

$$\phi_M = \text{ Compensator phase at } f_c' = 45^\circ \log\left(\frac{f_p}{f_z}\right)$$

$$45^\circ = 45^\circ \log\left(\frac{f_p}{f_z}\right)$$

$$\frac{f_p}{f_z} = 10^1$$

$$f_p = 10 f_z$$

Also, f_c' will necessarily be the geometric mean of the pole and the zero frequency. Since the phase margin condition gives a relationship between the pole and zero frequencies, this can be used to solve for both.

$$f_c' = \sqrt{f_z f_p}$$

$$5 \text{ kHz} = \sqrt{10 f_z^2}$$

$$f_z = \frac{5 \text{ kHz}}{\sqrt{10}}$$

$$f_z = 1.58 \text{ kHz and } f_p = 15.8 \text{ kHz}$$

These relationships result in the pole and zero frequencies for the lead compensator. To complete the design, the required low-frequency gain G_{c0} of the compensator to place the unity-gain point at the appropriate frequency must be determined. This can be found by equating the values of the gain asymptotes at f_z.

$$T_0 G_{c0} \left(\frac{f_0}{f_z}\right)^2 = \frac{f_c'}{f_z}$$

Substituting the values of f_0 and T_0 for the example converter, and the values of f_z and f_c' as previously calculated, the gain G_{c0} of the compensator is

$$G_{c0} = \frac{1}{T_0} \left(\frac{f_z}{f_0}\right)^2 \frac{f_c'}{f_z}$$

$$G_{c0} = \frac{1}{2.33} \left(\frac{1.58 \text{ kHz}}{1 \text{ kHz}}\right)^2 \frac{5 \text{ kHz}}{1.58 \text{ kHz}}$$

$$G_{c0} = 3.4$$

The resulting compensated system has a phase margin of 45°, as designed for. The gain margin can be found by evaluating the gain at the point the phase crosses −180°. This occurs at $10 f_p$.

$$G_M = \text{ Gain below 0 dB at } 10 f_p$$

$$\text{Gain} = \frac{f_c' f_p}{f^2} = \frac{(5\text{ kHz})\, f_p}{(10 f_p)^2} = \frac{5\text{ kHz}}{100\,(15.8\text{ kHz})}$$

$$\text{Gain} = 0.00317 \Rightarrow -50\text{ dB}$$

$$G_M = 50\text{ dB}$$

Since the general desirable gain margin for a stable system is 10 dB, this is quite acceptable. In reality, since the phase only approaches $-180°$, the gain margin of the system will actually be infinite, as in the previous two cases. In any case, this compensated system has very good phase and gain margins.

With all of the parameters of the lead compensator determined, what remains is to implement the compensator using an op-amp circuit and simulate the closed-loop converter to evaluate its performance. A general circuit that can be used to implement any lead or lag compensator is shown in Figure 12. The transfer function of this circuit is

$$G_c(s) = -\frac{R_2}{R_1}\left(\frac{R_1 C_1 s + 1}{R_2 C_2 s + 1}\right) \tag{11}$$

The resistor ratio sets the low frequency gain, and the two resistor-capacitor pairs set the pole and zero frequencies. Two standard valued resistors that give nearly the required gain are $R_1 = 100\text{ k}\Omega$ and $R_2 = 330\text{ k}\Omega$. From these values, the capacitor values to set the pole and zero can be calculated.

$$\omega_z = \frac{1}{R_1 C_1} \Rightarrow 2\pi\,(1.58\text{ kHz}) = \frac{1}{(100\text{ k}\Omega)\, C_1}$$

$$C_1 = \frac{1}{2\pi\,(1.58\text{ kHz})\,(100\text{ k}\Omega)} \Rightarrow C_1 = 1.0\text{ nF}$$

$$\omega_p = \frac{1}{R_2 C_2} \Rightarrow 2\pi\,(15.8\text{ kHz}) = \frac{1}{(330\text{ k}\Omega)\, C_2}$$

$$C_2 = \frac{1}{2\pi\,(15.8\text{ kHz})\,(330\text{ k}\Omega)} \Rightarrow C_2 = 33\text{ pF}$$

It it also necessary to derive a value for the reference voltage on the non-inverting input of the op-amp. The sensed voltage from the output will be 5 V in steady-state as before, and the control voltage should be 2.14 V. Using these in combination with the resistor values for the lead compensator, the reference voltage can be found.

$$V_{ref} = \frac{R_2}{R_1 + R_2} V_{sense} + \frac{R_1}{R_1 + R_2} V_{control}$$

$$V_{ref} = \frac{330\text{ k}\Omega}{100\text{ k}\Omega + 330\text{ k}\Omega}\,(5\text{ V}) + \frac{100\text{ k}\Omega}{100\text{ k}\Omega + 330\text{ k}\Omega}\,(2.14\text{ V}) = 4.33\text{ V}$$

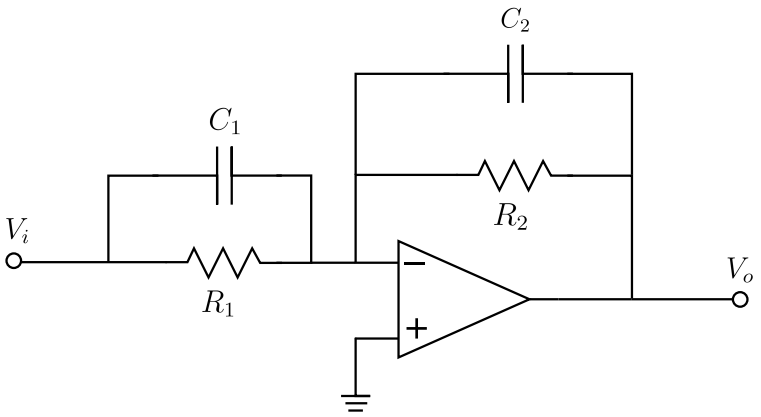

Figure 12: Op-amp circuit implementation of lead compensator

Using these values in the PECS simulator, the response of the lead-compensated buck converter to a step in the input voltage was simulated as before. The results of the simulation are shown in Figure 13. The lead compensator is quite effective in increasing the phase margin of the system. The oscillatory behavior evident in the output voltage of the uncompensated converter is not present, and the magnitude of the steady-state error due to the step is reduced, though not eliminated. Thus, the system with the lead compensator is very stable, but will still exhibit steady-state errors to a step disturbance. To fix this problem, the system type number must be increased by adding a pole at $s = 0$. This is the approach taken in the design of the next and final compensator.

Combined Lead and PI Compensation

Although both the PI compensator and the lead compensator were able to improve some aspects of the buck converter, neither was able to completely eliminate its undesirable properties. The lead compensator provided a good transient response, but had a steady-state error to step disturbances, since the compensated loop gain had a type number of 0. The PI compensator had a type number of 1 and thus was able to eliminate steady-state error in response to a step, but had undesirable transient characteristics. By combining the two compensators, one can use the advantages of each to design a more effective compensator. The transfer function for such a combined lead and PI compensator is

$$G_c(s) = \frac{G_{c0}\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{s\left(1+\frac{s}{\omega_p}\right)}, \tag{12}$$

where ω_{z2} is the zero introduced by the lead compensator and thus $\omega_{z2} < \omega_p$. Also, to separate the effects of the lead and PI portions of the compensator, it

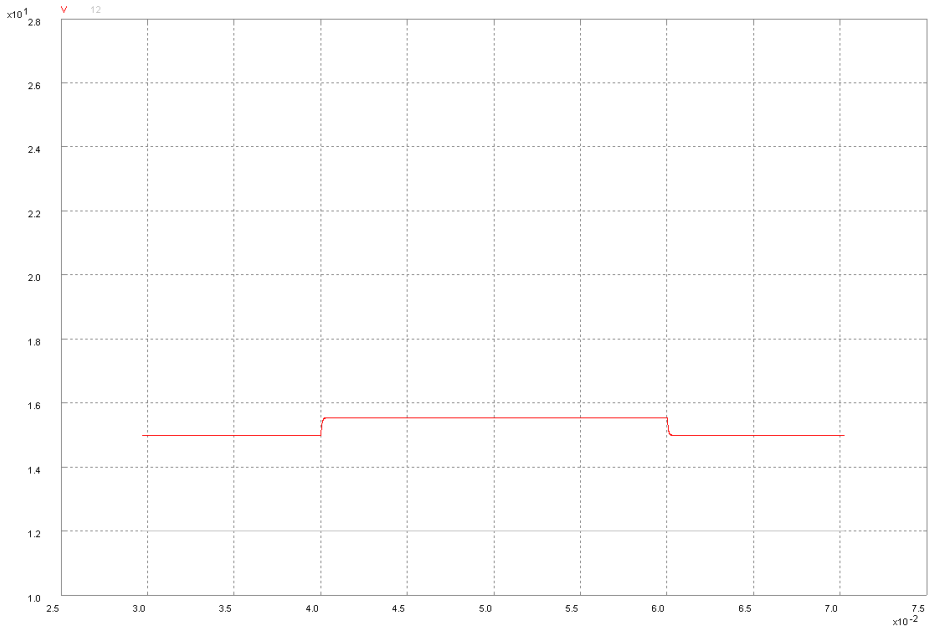

Figure 13: Step response of lead-compensated buck converter

will be assumed here that $\omega_{z1} < \omega_{z2}$. An asymptotic Bode plot of the transfer function of this compensator is shown in Figure 14. When ω_{z2} at a frequency 10 times or more greater than ω_{z1}, the design is separated into two essentially independent pieces, the design of a PI compensator at low frequencies and the design of a lead compensator at high frequencies.

A plot of the loop gain of the example converter with a combined lead and PI compensator is shown in Figure 15. To determine the design, the two zeros and the pole must be placed. For the phase response of the two compensator portions to have no interaction, ω_{z1} must be two decades below ω_{z2}. For a faster response, it would be good that ω_{z2} be as large as possible, but ω_{z2} should not be too large. The value used here is $f_{z2} = 2$ kHz, and thus $f_{z1} = 20$ Hz. As determined in the design of the lead compensator, to get a phase margin of 45°, $\omega_p = 10\omega_{z2}$, which means that $f_p = 20$ kHz. With the pole and zeros placed, the only factor that remains to determine is the gain. Since it is desirable to have a large gain at low frequencies, the combined compensator will be designed to have the gain factor $G_{c0}T_0$ be 1000. This gives a value of

$$G_{c0}T_0 = 1000 \Rightarrow G_{c0} = \frac{1000}{2.33} \Rightarrow G_{c0} = 430$$

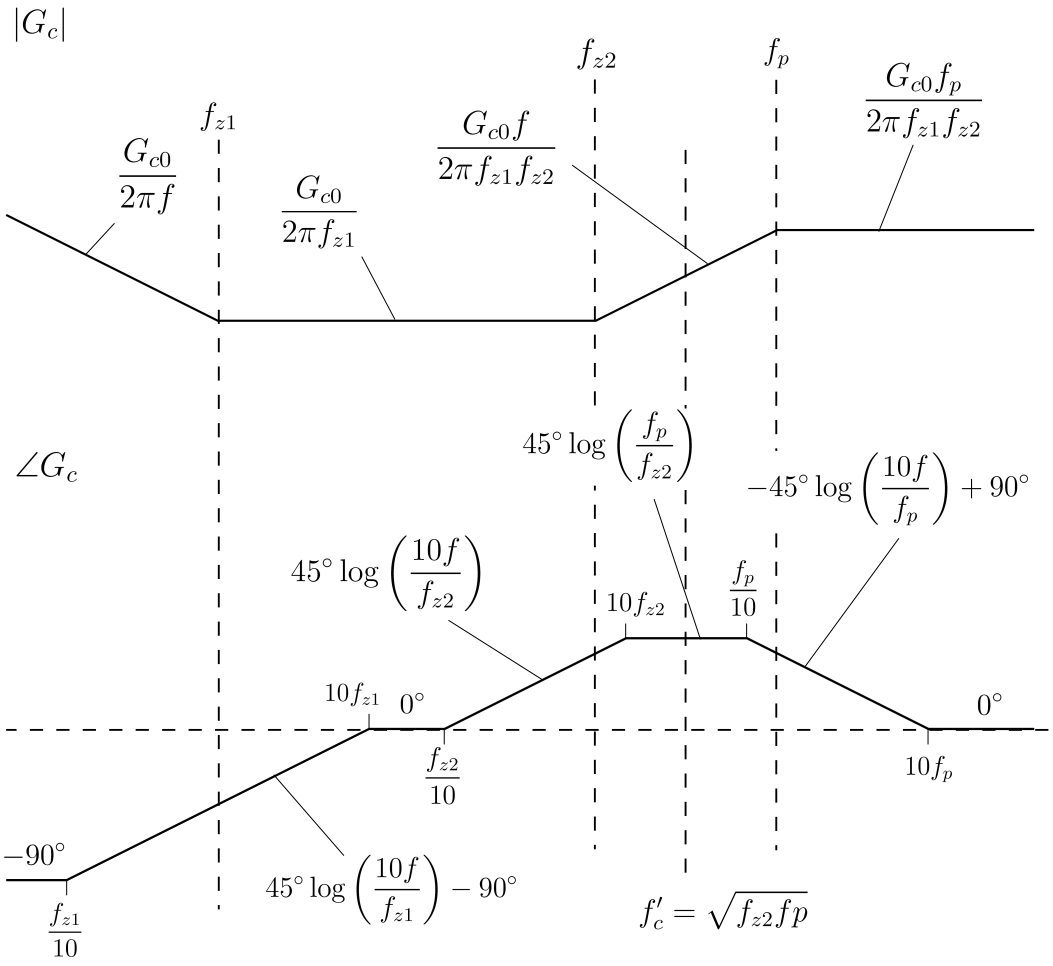

Figure 14: Lead and PI compensator transfer function

1 NextSection

The gain and phase margins can be found by evaluating the asymptotes at the respective crossover frequencies. The unity-gain crossover frequency is $f'_c =$

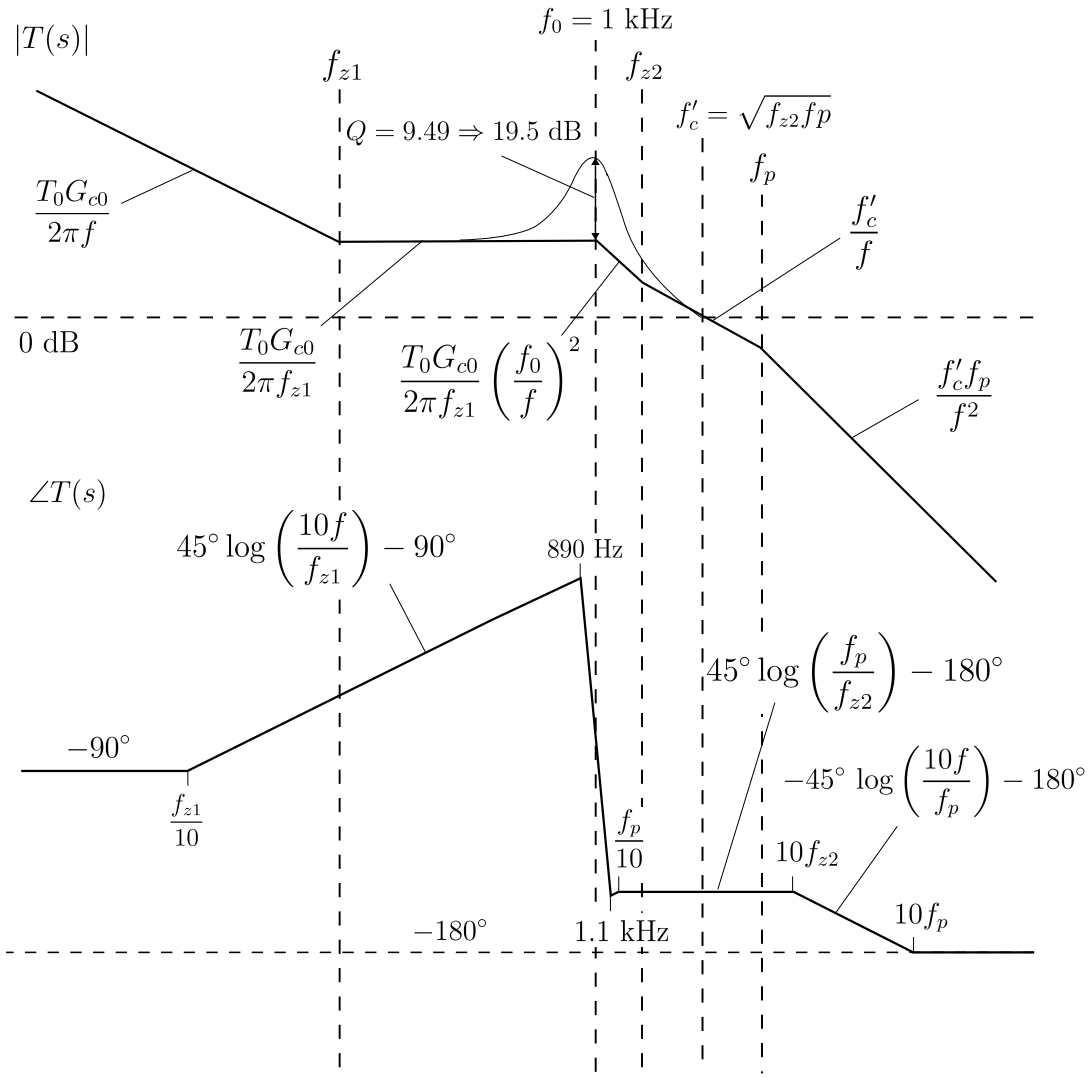

Figure 15: Loop gain with lead and PI compensator

$\sqrt{f_{z2} f_p} = 6.32$ kHz. The phase at this frequency is given by

$$\angle T(s) = 45^\circ \log\left(\frac{f_p}{f_{z2}}\right) - 180^\circ = 45^\circ \log\left(\frac{20 \text{ kHz}}{2 \text{ kHz}}\right) - 180^\circ = -135^\circ$$

The phase margin is thus

$$\phi_M = 180^\circ + \angle T(s) = 180^\circ - 135^\circ = 45^\circ$$

which is no surprise, since this is what was designed for. A gain margin value could be calculated as before, using $10\omega_p$ as the $-180°$ crossover frequency, but as previously discussed, the actual gain margin will be infinite. Thus, the combined compensator has a 45° phase margin, an infinite gain margin, and a pole at $s = 0$. This system should be very stable, exhibit good transient response, and completely compensate for step disturbances with no steady-state error.

The circuit implementation for the lead and PI compensator is simply a lead circuit as shown in Figure 12 cascaded with a PI circuit as shown in Figure 8. The same expressions given before can be used to find the new component values. The overall gain of the compensator must be 430. For simplicity, the gain of the lead section will be set to 4.3 and the gain of the PI section set to 100. A resistor pair that gives the required gain for the lead section is $R_{L1} = 27$ kΩ and $R_{L2} = 120$ kΩ. Using these values, the capacitor values to place the pole and the second zero are simply

$$\omega_{z2} = \frac{1}{R_{L1}C_{L1}} \Rightarrow 2\pi\,(2\text{ kHz}) = \frac{1}{(27\text{ k}\Omega)\,C_{L1}}$$

$$C_{L1} = \frac{1}{(27\text{ k}\Omega)\,(2\pi 2\text{ kHz})} \Rightarrow C_{L1} = 3.0\text{ nF}$$

$$\omega_p = \frac{1}{R_{L2}C_{L2}} \Rightarrow 2\pi\,(20\text{ kHz}) = \frac{1}{(120\text{ k}\Omega)\,C_{L2}}$$

$$C_{L2} = \frac{1}{(120\text{ k}\Omega)\,(2\pi 20\text{ kHz})} \Rightarrow C_{L2} = 68\text{ pF}$$

The PI section must provide a gain of 100 and place ω_{z1} at 20 Hz. If R_{I2} is assumed to be 100 kΩ, then the values of the capacitor and the remaining resistor can be found.

$$\omega_z = \frac{1}{R_{I2}C_I} \Rightarrow 2\pi\,(20\text{ Hz}) = \frac{1}{(100\text{ k}\Omega)\,C_I}$$

$$C_I = \frac{1}{2\pi\,(20\text{ Hz})\,(100\text{ k}\Omega)} \Rightarrow C = 82\text{ nF}$$

$$G_{I0} = \frac{1}{R_{I1}C_I} \Rightarrow 100 = \frac{1}{R_{I1}\,(82\text{ nF})}$$

$$R_{I1} = \frac{1}{100\,(82\text{ nF})} \Rightarrow R_{I1} = 120\text{ k}\Omega$$

These values can be used in PECS to simulate the response of the converter. A reference voltage of 5 V can be used, as with the PI compensator.

The simulated response of the combined compensator to the same step disturbance is shown in Figure 16. The nature of the improvement is evident. Just as with the PI compensator, the initial disturbance is fully compensated for and the output voltage returns to the set-point value. This is due to the high-low frequency gain, which tends to cause such disturbances to be rejected. As with the lead compensator, the voltage transitions smoothly and with no oscillations, since the phase margin of the system is within the acceptable range. By combining these benefits, this circuit represents a fairly good method of controlling the output of a buck converter

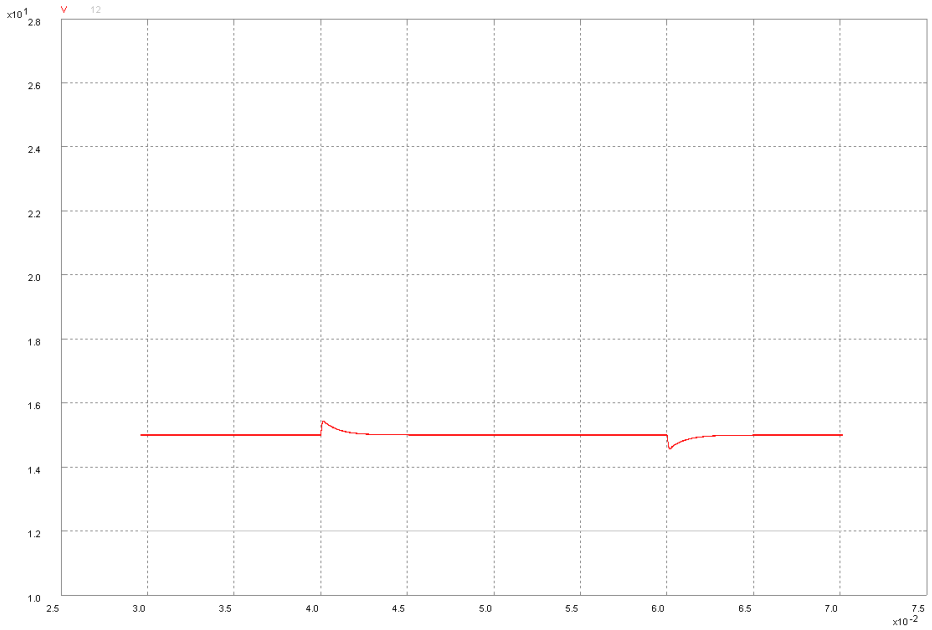

Figure 16: Step response of lead- and PI-compensated buck converter

Conclusion

This paper has discussed the design of three different compensators for the buck switching converter, and evaluated their performance based on phase margins and the response to an input voltage step. The first design was a PI compensator, which provided good voltage regulation but poor transient performance. The second design was a lead compensator, which by increasing the phase margin of the system yielded very good transient response, but which still demonstrated a steady-state error to a step. By combining these two approaches, the final lead and PI compensator provides an excellent regulator for the buck converter, which keeps the output voltage at the set value despite large

changes in the input voltage. These results could be applied to the construction of a practical compensator for an operating buck converter, or as an example of how to design controllers for other switching converter topologies.

References

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[2] Raymond T. Stefani, Bahram Shahian, Clement J. Savant, and Gene H. Hostetter. *Design of Feedback Control Systems*. Oxford University Press, fourth edition, 2002.

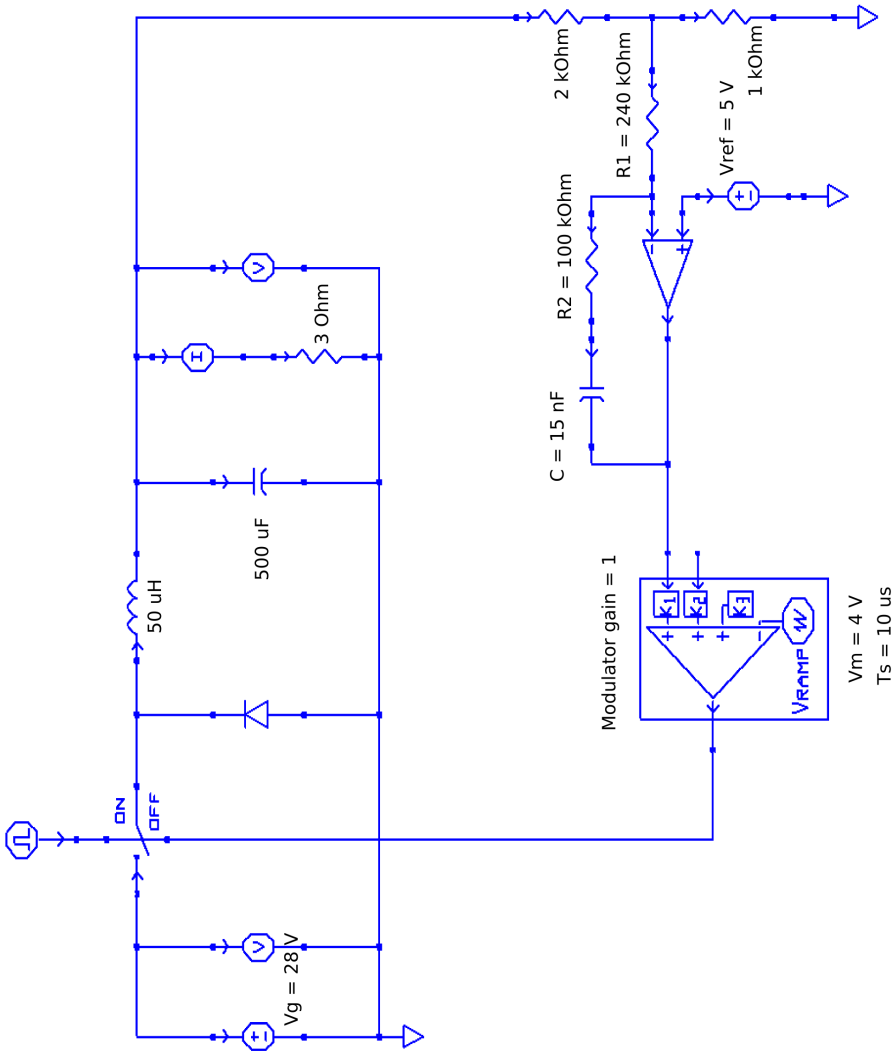

Figure 17: PECS schematic of PI-compensated buck converter

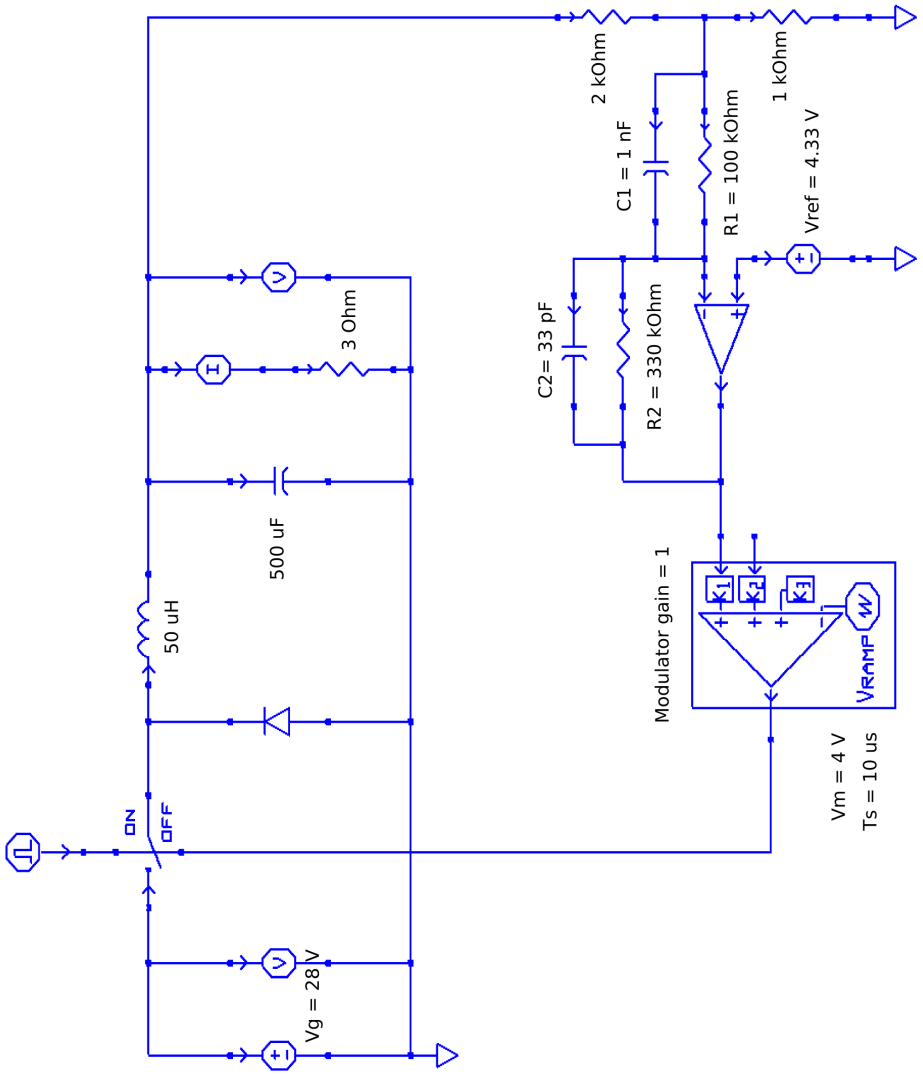

Figure 18: PECS schematic of lead-compensated buck converter

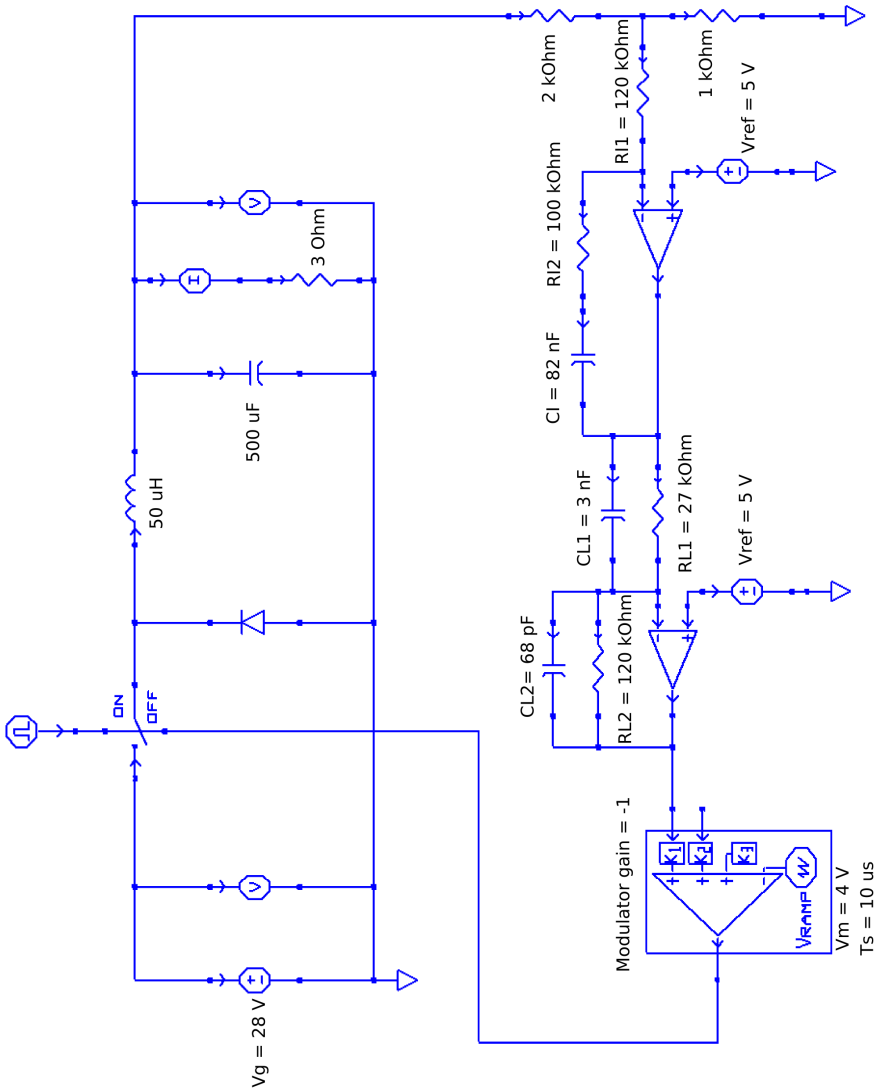

Figure 19: PECS schematic of lead - and PI-compensated buck converter