ECE317 Lab 5: **20251028**

Aim: To construct the QSpice model of the buck converter system with an integral compensator and to subsequently obtain the simulated output voltage response due to load step changes.

Task:

Previously you had implemented the QSpice schematic of Lab 6. With just some minor changes, the QSpice schematic for Lab 5 can be completed. The Lab 5 hardware schematic is shown below. Lab 5 uses a different compensator, namely an integral compensator.

Make the changes to Lab 6 to implement the QSpice schematic of Lab 5 and obtain the output voltage response due step load changes.

Lab 5 hardware schematic: