ECE317 Lab 4: **20251023**

Aim: To construct the QSpice model of the open loop buck converter system and to subsequently obtain the simulated output voltage response due to load step changes.

The following four pages feature the following:

Page #2: The complete hardware schematic for the closed loop dc-to-dc regulator that shows an example of the compensator that will be designed in Lab 6. In Lab 6 you will be designing your own version of this compensator.

Page #3: A QSpice implementation of the page #2 schematic that can be used for simulation.

Page #4: The response obtained from the QSpice schematic of page #3. It shows the output voltage response due to step load changes.

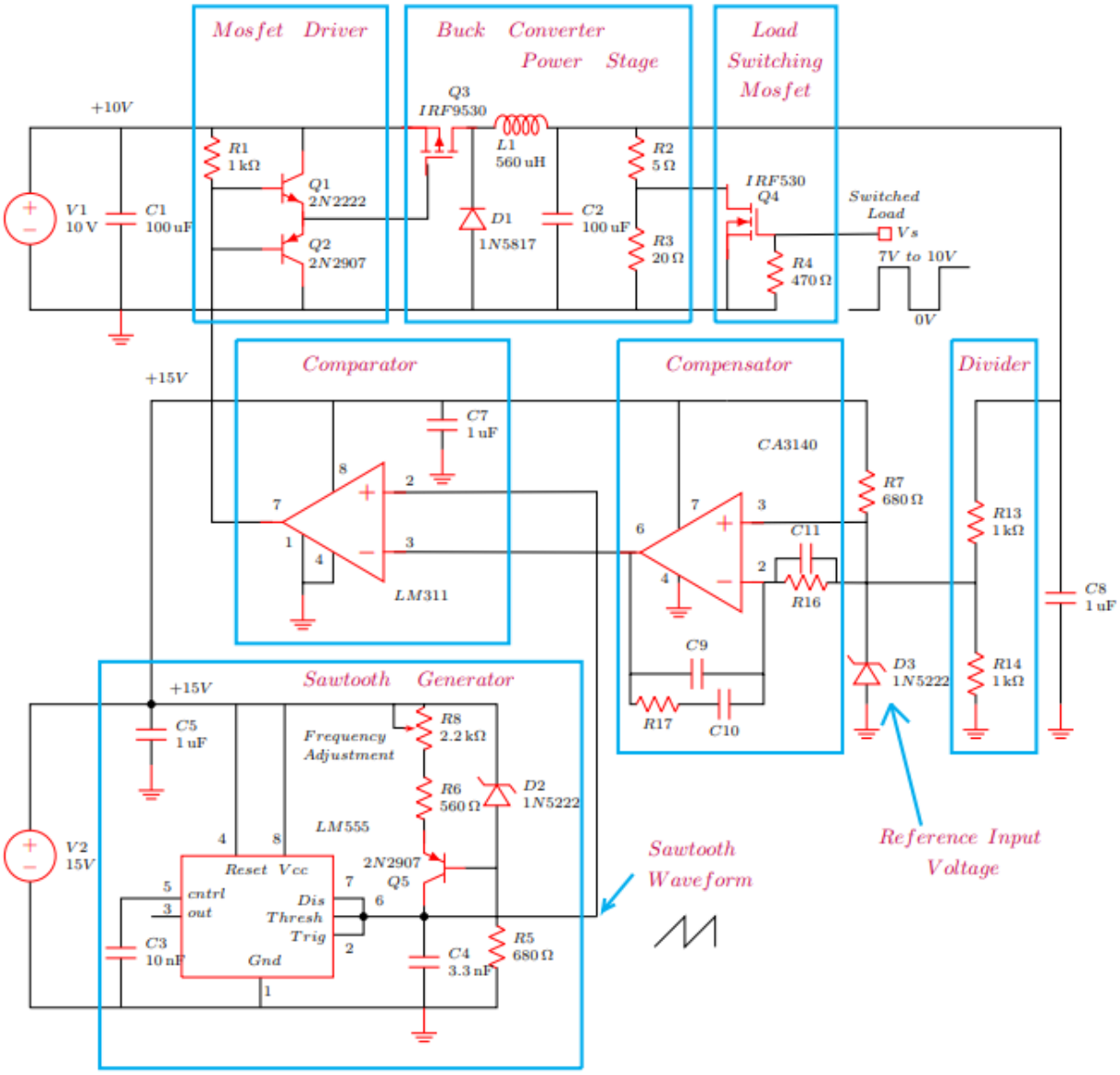
Page #5: The hardware schematic of the open loop buck converter system.

Perform the following tasks for Lab 4:

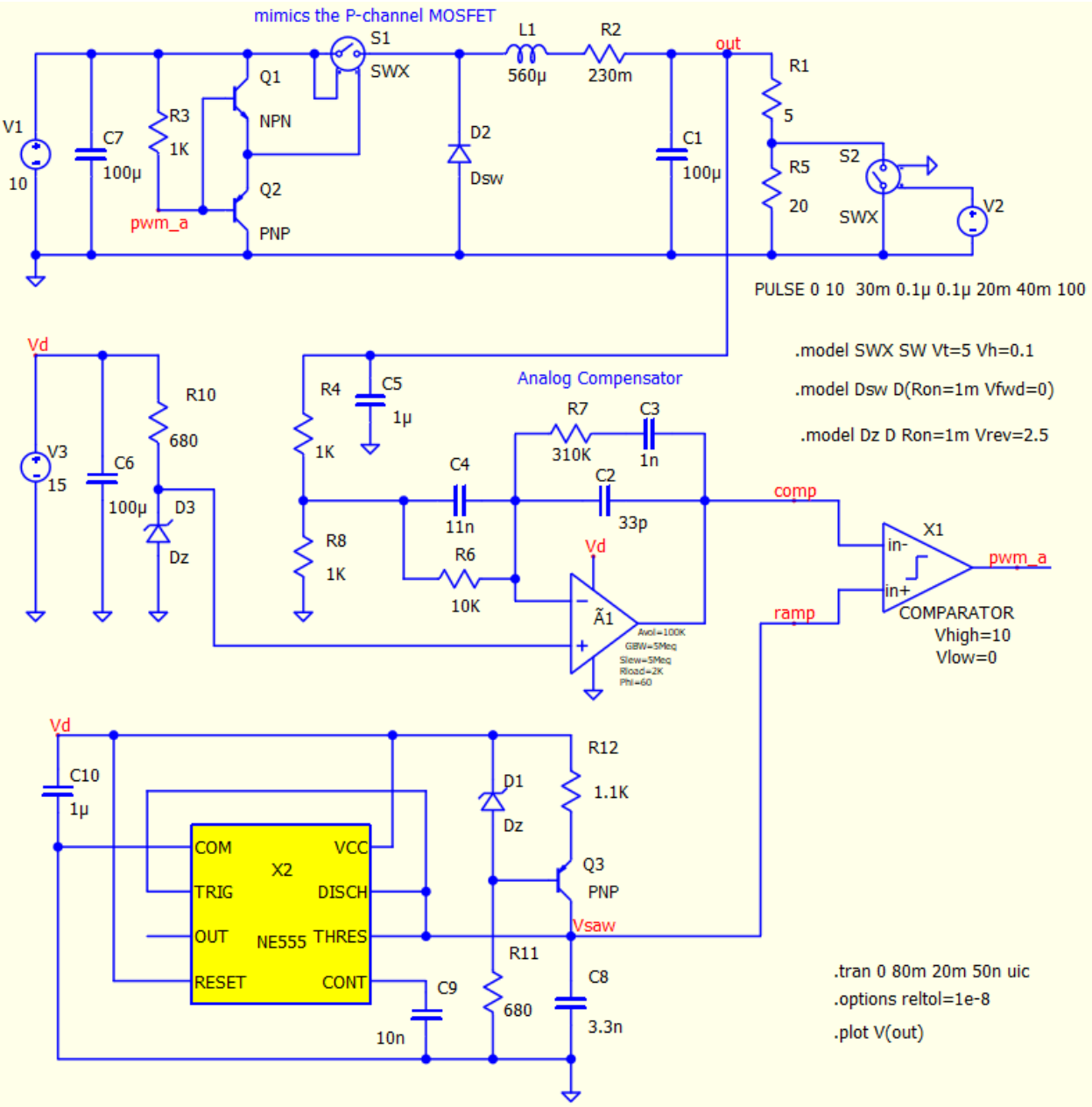
1) Initially implement the QSpice schematic of Lab 6 which is shown on page #3.
2) Run the completed schematic and verify that your results agree with those shown on page #4.
3) Once you have verified your simulation results, perform the following simple tweak. Ajust resistor R12 (which is part of the sawtooth subcircuit) such that the sawtooth waveform has a 40 kHz frequency. This can be done through a number of trial-and-error attempts monitoring the frequency at Vsaw as the value of R12 is adjusted.
4) Once all the above is completed, save your final schematic for later use in Lab 6.
5) Now to implement the open loop schematic of Lab 4, modify a copy of your just completed schematic such that it corresponds to the hardware schematic of page #5. There is no need to include components R7 and C6.
6) Adjust VR1 to achieve a DC voltage output of 5 V when the load is 25 ohms.
7) Using this schematic obtain the simulated output voltage response of due to a load step change.

The obtained response will be used later in Lab 6 to compare the different responses obtained in this lab (Lab 4), Lab 5 and Lab 6 (which will use your compensator design).

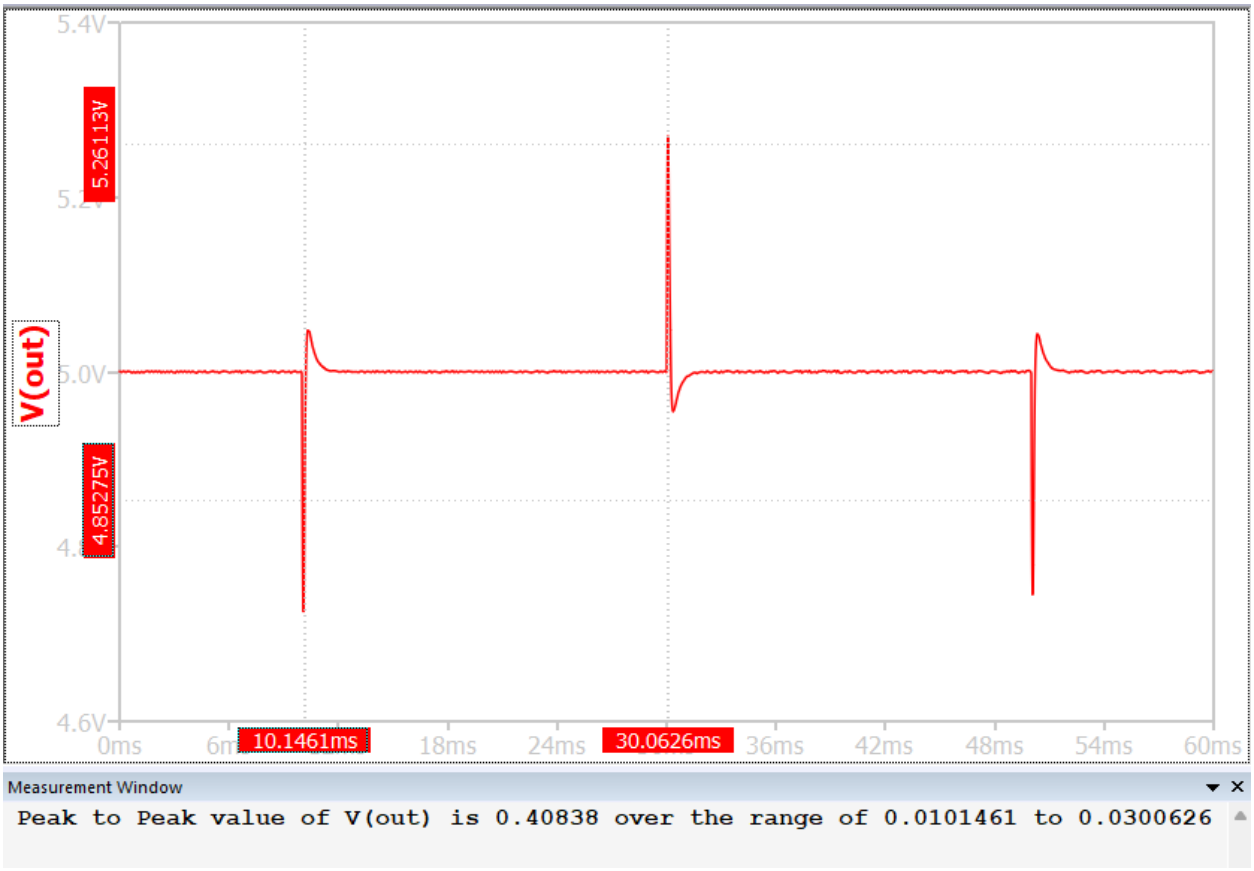
Lab 6 schematic:



QSpice model of Lab 6 schematic:



Lab 6 schematic simulated output voltage response due to step load changes:



Lab 4 schematic: