# Lab 3

## System Modelling of the dc-to-dc Buck converter

### 0.1 Objectives

The circuit simulator QSPICE will used to examine and characterize the steady state operating conditions of the dc-to-dc buck converter and will aid in the confirmation of the system transfer functions. The open loop response to step changes in the input voltage as well as step load changes are also examined using both QSPICE and Matlab. Matlab will also be used in examining the system transfer functions. Through these simulations the student will gain a better understanding of the operation of the buck converter circuit. The transfer functions verified here will be used later to design effective closed loop feedback control.

### 0.2 Background

The LCR network examined in the previous lab is used together with a single pole, double throw switch to derive a power processing circuit known as the dc-to-dc Buck converter. This circuit takes a dc voltage source at the input and transforms it to a lower value dc level at the output, whilst achieving a high power efficiency, typically in the 90% range. This is possible through the use of a high frequency switch.

The schematic of the buck converter is shown below in Figure 1. The converter schematic has been divided into 3 sections: 1) the input voltage source, $V_g$, 2) the single-pole double-throw switch, and 3) the LCR network which comprises the low-pass filter. To more accurately model the losses in the inductor a series resistor, $r_L$, is included. The output load to which the power is delivered in represented by resistance $R$.

The switch is operated in cyclical manner with period, $T_s$. At the start of each period the switch is in its upper position which connects the input source to the output filter. The switch stays in this position for length of time, $DT_s$, where $D$ is known as the *duty ratio* which takes a value $0 < D < 1$. At the end of the $DT_s$ subinterval the switch changes position to disconnect the input source.

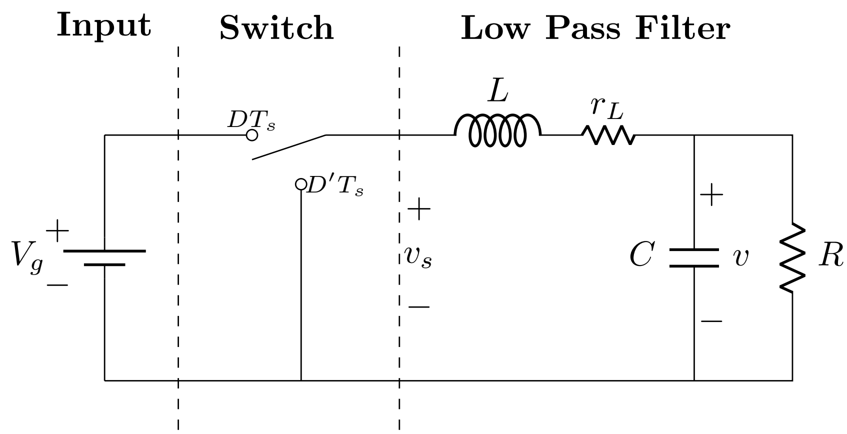
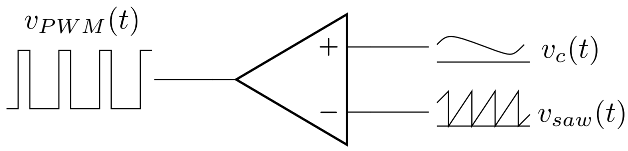


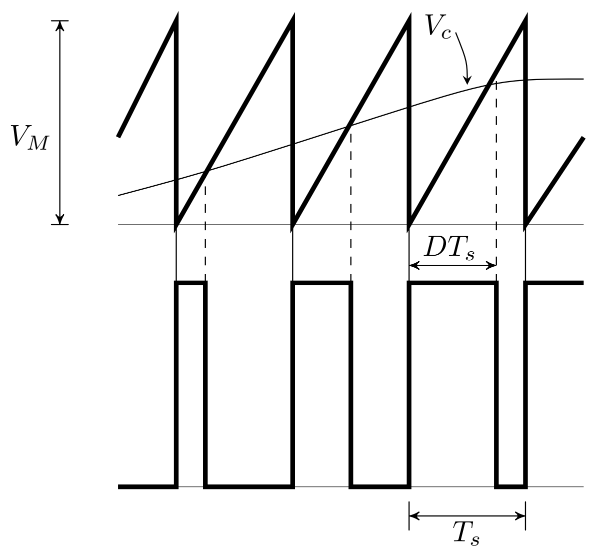

Figure 1: Dc-to-dc Buck converter.

The length of time remaining until the end of cycle is $D'T_s$ where $D' \equiv 1-D$. So we see that through the switching action the voltage $v_s$ appearing at the input of the low pass filter is a rectangular wave. The output of the filter is predominately a constant dc level, which corresponds to the average of the input waveform, together with a small ripple which represents the unfiltered residuals of the input waveform. Neglecting losses (which generally will be very small by design) the dc output voltage is given by $V = DV_g$. Given the range of $D$ we see that the output can be adjusted from 0 to $V_g$. Control of the output voltage is achieved by variation of the duty ratio. To denote a time varying quantity a lower case symbol will be used and thus a varying duty ratio is denoted by $d$. Also, to further highlight a signal that represents a deviation around a steady state average, we will use a caret '^', so that $\hat{d}$ is the small signal deviation around the average duty ratio $D$. Therefore, the time varying duty ratio $d(t)$ is comprised of an average (DC) value together with a deviation $\hat{d}$ around this average so that $d = D + \hat{d}$ or alternatively, $\hat{d} = d - D$.

To achieve a varying duty ratio given a control voltage, $v_c$, a pulse width modulator (PWM) circuit is used, see Figure 2. This is comprised of an op-amp comparator to which one of the inputs is connected to a sawtooth waveform, $v_{saw}$, which has a peak-to-peak amplitude of $V_M$ and period $T_s$. As shown in Figure (2b) a comparison of the control voltage, $v_c$, results in a rectangular output waveform of period, $T_s$, and duty ratio, $d$. Combining the PWM with the buck converter results in an open loop controlled buck converter shown in Figure 3. Through the use of the QSPICE simulator we will examine the steady state operation of this system.




(a)




(b)

Figure 2: (a) PWM comparator, (b) comparison of the control signal, $v_c$, with the sawtooth waveform $v_{saw}$, results in a variable pulse width rectangular waveform used to drive the switch in the buck converter.

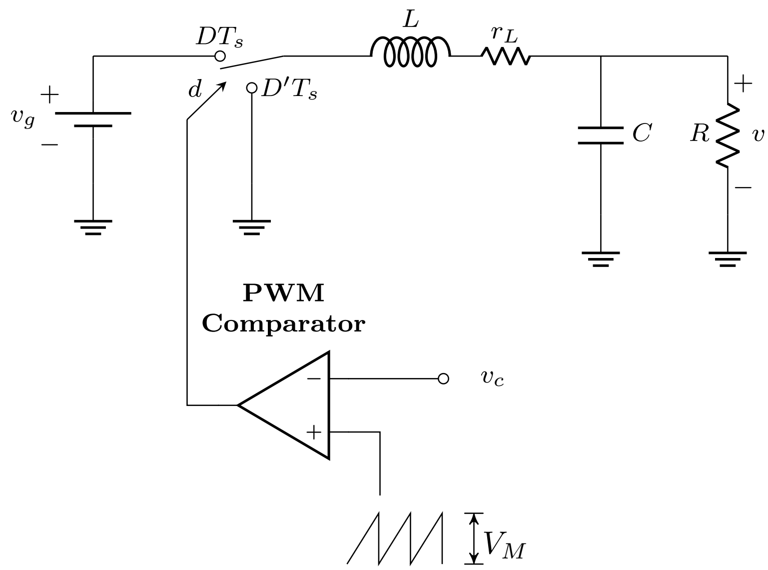



Figure 3: Open loop controlled buck converter. The duty ratio $d$ of the converter is set by the control voltage, $v_c$, via the PWM comparator.

## 0.3 System Transfer Functions

In a later lab we will design a closed loop controller for this system. To be able to do this using a classical control design methodology we will first need to determine important transfer functions of the system. We will consider three transfer functions. The first is the *control-to-output voltage* transfer function. This transfer function has two components: the *duty ratio to output voltage* transfer function of the buck converter power stage, $G_{vd}$, and the pulse width modulator transfer function, $G_{PWM}$.

Control-to-output transfer function:

$$\frac{\hat{v}}{\hat{v}_c} = G_{vd} \cdot G_{PWM} = \frac{\hat{v}}{\hat{d}} \cdot \frac{\hat{d}}{\hat{v}_c}$$

where the caret (ˆ) has been used to denote a small signal signal quantity. Note that since the modulator is nonlinear, a so-called *describing function* analysis method is used to determine the transfer function which ends up being a (frequency independent) constant gain given by:

$$G_{PWM} = \frac{\hat{d}}{\hat{v}_c} = \frac{1}{V_M}$$

The control-to-output transfer function plays a very important role in control design as it forms part of the loop gain which is important to stability and achieving good stability margins (both phase and gain).

The other two transfer functions of the buck converter we will consider are 1) the *input voltage to output voltage* transfer function and, 2) *output load current to output voltage* transfer function:

1. input voltage to output voltage transfer function: $G_{vg} = \frac{\hat{v}}{\hat{v}_g}$
2. output load current to output voltage transfer function: $\frac{\hat{v}}{\hat{i}_o} = -Z_{out}$

These transfer functions quantify how variations in the input quantity at various frequencies propagate to the output. That is, how much of an affect does input voltage variations or load current variations have on the output voltage. Ideally, in a voltage regulator system as we are considering here, we would like this to be zero. In this lab we will examine the Bode magnitude response to see what level of transmission is achieved in open loop operation. With a properly designed control system incorporating feedback, these input disturbance propagations through the system will be greatly diminished.

A block diagram model of the buck converter transfer functions which will be used in a later lab for controller design is shown in Figure 4. In this lab we'll do a partial verification of these transfer functions comparing them with previously derived results.

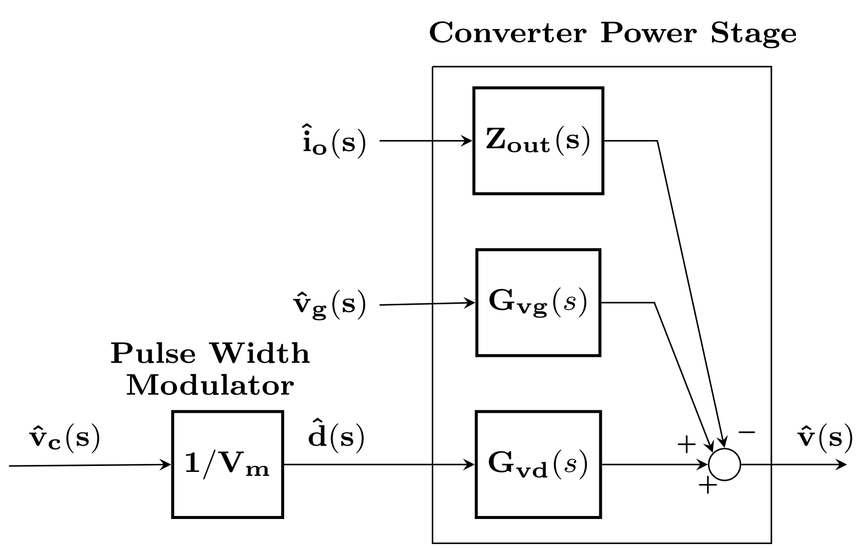



Figure 4: Block diagram model of the Buck converter along with the pulse width modulator.

For transfer functions $G_{vg}$ and $G_{vd}$ considering the signal flow from the input through to the output of the converter, one can readily assume a form as follows

$$G_{vg}(s) = \frac{\hat{v}_s}{\hat{v}_g} \cdot \frac{\hat{v}}{\hat{v}_s} = K_{vg} \cdot G_{LPF}(s)$$

and

$$G_{vd}(s) = \frac{\hat{v}_s}{\hat{d}} \cdot \frac{\hat{v}}{\hat{v}_s} = K_{vd} \cdot G_{LPF}(s)$$

where $\hat{v}_s$ represents the small signal voltage variations at the input of the output filter and where $K_{vg}$ and $K_{vd}$ are constant gains and $G_{LPF}(s)$ represents the transfer function of the second order low pass $LCR$ filter which, as seen in the previous lab, is given by

$$G_{LPF}(s) = \frac{1}{\left(\frac{s}{\omega_n}\right)^2 + 2\xi\frac{s}{\omega_n} + 1}$$

Note that the damping ratio, $\xi$, now includes the effect of inductor losses, as considered at the end of Lab. 2, by including $r_L$, the inductor ESR (equivalent series resistance). Constants $K_{vg}$ and $K_{vd}$ represent the effect of the switching elements in propagating variations of the input voltage level (for $G_{vg}$) or variations of the duty ratio (for $G_{vd}$) to the input of the low pass filter. $K_{vg}$ and $K_{vd}$ represent the DC gain of the relevant transfer functions and will be found through simulation below.

**Output load current to output voltage transfer function: $\frac{\hat{v}}{\hat{i}_o} = -Z_{out}$:**

The final transfer function that we'll consider is related to the output impedance of the buck converter. Despite the presence of switching which affected the two other transfer functions considered (i.e. $G_{vd}$ and $G_{vg}$), the output impedance is more straightforwardly determined as switching has no effect. The circuit configuration of the buck converter during the first ($DT_s$) subinterval is seen in Figure 5a, and during the remainder of the period (the $D'T_s$ interval) is seen in the Figure 5b. As independent sources are nulled for determination of impedances we can see that the output impedance, $Z_{out}$, are the same during the two subintervals and can be simply seen as a parallel connection of three impedances such that:

$$Z_{out} = (sL + r_L) \parallel \frac{1}{sC} \parallel R$$

You will be asked to evaluate this in a latter task.

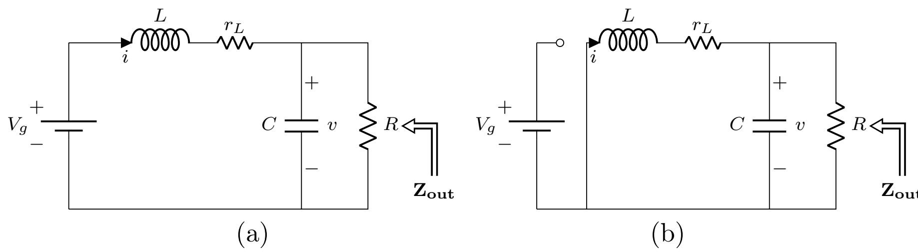



Figure 5: Buck converter configuration during (a) the first subinterval, $DT_s$, and (b) the second subinterval, $D'T_s$.

The actual transfer function of interest for us is that related to how output current variations, $\hat{i}_o$, lead to output voltage variations, $\hat{v}$. With reference to Figure 6 we see that the output current $i_o$ is given by

$$i_o = I_o + \hat{i}_o$$

where the capitalized symbol refers to the DC steady state value and the term with a caret (ˆ) indicates a small-signal variation. A similar expression can be written for the output voltage: $v = V + \hat{v}$

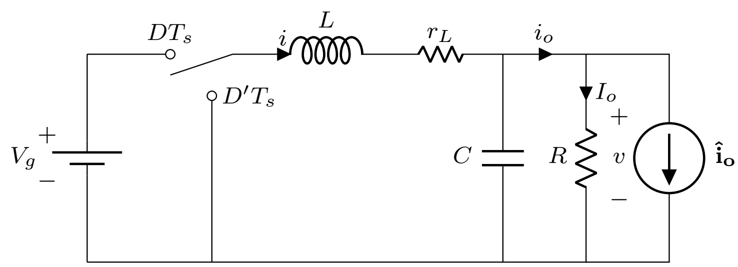



Figure 6: The effect of output current variations, $\hat{i}_o$, causing output voltage variations, $\hat{v}$, is quantified by transfer function $-Z_{out}$.

Consequently the small signal transfer function for the output impedance $Z_{out}$ is given by

$$Z_{out} = \frac{\hat{v}}{-\hat{i}_o}$$

and consequently the transfer function of interest $\frac{\hat{v}}{\hat{i}_o}$ which we would like to determine is given by

$$\frac{\hat{v}}{\hat{i}_o}(s) = -Z_{out}$$

Note however that in the simulation (and later in the lab with the hardware implementation), in order to achieve output current variations we will be stepping the load, that is, changing the load resistance between two different values. This however causes the system transfer functions to be modified somewhat. However, as seen in Lab. 2 the major change that occurs is that of varying the damping factor of the circuit. Nevertheless considering the convenience of performing a step load change in the lab, the approximation considered here will be accepted.

## 0.4 Tasks

This section outlines the tasks to be performed using the QSpice circuit simulator to examine and characterize the steady-state operating conditions of the DC-to-DC buck converter and to aid in the confirmation of the system transfer functions.

### General QSpice Notes:

- All references should now be understood as referring to "QSpice" and its built-in waveform viewer.
- Circuit schematics will be built and simulated in QSpice.
- Component naming and simulation commands will follow QSpice conventions. For plotting, you will typically use QSpice's waveform viewer to observe node voltages like `V(vp1)` or component currents like `I(S1)`.
- The PWM block is implemented in QSpice using a voltage comparator (e.g., an op-amp or a dedicated comparator component) and a sawtooth waveform generated by a Piecewise Linear (PWL) voltage source.

1. **Start-up transient:** In this first task we will examine the start-up transient and steady state operation of the buck converter.
    - **Action:** Open the QSpice circuit file for the buck converter with pulse width modulator. The QSpice schematic is shown in Figure 7
    - **Simulation Parameters:** Set up a transient analysis. In QSpice, this is typically done using a `.tran` simulation command. For example: `.tran 1u 60m 0 1u` (This command means: time step 1µs, stop time 60ms, start saving data at 0s, maximum time step 1µs). Adjust these values as per the original manual's intent:
        - *Final Time (Stop Time):* `60m` (for 0.06s)
        - *Time Step (Maximum Time Step):* `1u` (for $1 \times 10^{-6}$s)
        - *Start Saving Data Time:* `0`
    - **Action:** Run the simulation.

- **Analysis:** Plot the output voltage (e.g., `V(vp1)` if your output node is labeled `vp1`).
- **Note:** The large start-up transient is not of primary interest here as it is a large-signal phenomenon and may be easily avoided with a slight redesign. However, observe and note the steady-state value of the output voltage.

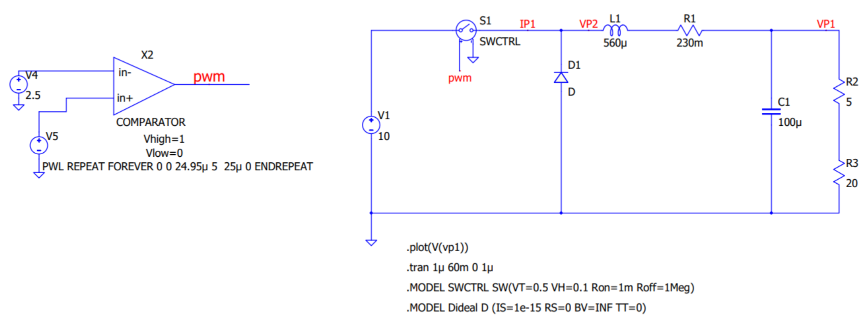



Figure 7: QSpice schematic of the Buck converter with pulse width modulator.

2. **Steady-state characteristics**: We will now rerun the simulation except we will only display the last few cycles of the response.

   - **Action:** Using the same QSpice circuit file as in Task 1 (Figure 7).
   - **Simulation Parameters:** Modify the transient analysis command to focus on the end of the simulation period. For example, to view the last few cycles before 60ms, you might set the *Start Saving Data Time* to approximately `59.88m` (for $5.9881 \times 10^{-2}$s from the original manual) and keep the *Stop Time* at `60m`. A QSpice command could be: `.tran 1u 60m 59.88m 1u`.
   - **Action:** Rerun the simulation.
   - **Analysis:**
     – Plot the output voltage (e.g., `V(vp1)`).
     – In QSpice's waveform viewer, you can add multiple traces to the same plot or create new stacked plots. Add plots for:
       ∗ The diode voltage (e.g., `V(vp2)` if the node across the diode is `vp2`, or by subtracting node voltages like `V(node_anode) - V(node_cathode)`).
       ∗ The switch current (e.g., `I(S1)` if your main switch is `S1`).
     – Arrange these plots one above the other if possible in the QSpice waveform viewer to observe relative timing relationships.

   Determine the following from the plots:

(a) The average output voltage (a visual estimate or use QSpice's waveform analysis tools if available for averaging over a cycle).

(b) The peak-to-peak output voltage (this is the output voltage 'ripple').

(c) The peak-to-peak diode voltage.

(d) The peak inductor current (e.g., `I(L1)`).

(e) The frequency of the waveforms (should correspond to your switching frequency).

(f) The duty ratio.

Explain how the duty ratio is set in this QSpice circuit, given the parameters of the sawtooth waveform (from the PWL source) and the control voltage (e.g., V4 = 2.5V in the QSpice schematic shown in Figure 7) (Hint: The duty ratio $D = V_{\text{control}}/V_{\text{sawtooth\_peak}}$).

3. $K_{vg}$ **and Step input voltage change:** We will now determine constant $K_{vg}$ using a step change of the input voltage and monitoring the resulting output voltage change, as was previously done in Lab 2. Recall from Lab 2 that

$$K_{vg} = \frac{\Delta v}{\Delta v_g} = \frac{v_{\text{final}} - v_0}{v_{g,\text{final}} - v_{g,0}}$$

where $v_{\text{final}}$ and $v_0$ represent the final (steady state) output level after the step has been applied and the value of the output before the application of the step input, respectively. Similarly for $v_{g,\text{final}}$ and $v_{g,0}$ which now refers to the input. We will apply a unit step input $\Delta v_g = 1V$ with $v_{g,\text{final}} = 11V$ and $v_{g,0} = 10V$.

- **Action:** Modify the main input voltage source (V1 in the QSpice schematic of Figure 7) in your QSpice circuit to produce step changes. Instead of a constant DC source, you can use a PWL (Piecewise Linear) source.
  - For a PWL source (V1), define time-voltage pairs: e.g., `PWL(0 10V 25m 10V 25.001m 11V 40m 11V 40.001m 10V)`.
  - This means: at t=0, V1=10V; up to t=25ms, V1=10V; at t=25.001ms, V1 steps to 11V; up to t=40ms, V1=11V; at t=40.001ms, V1 steps back to 10V. (The original manual suggests $t1 = 0.025s$ with $v1 = 11V$ and $t2 = 0.04s$ with $v2 = 10V$.)
- **Simulation Parameters:** Adjust the transient analysis *Start Saving Data Time* to shortly before the first step if needed, e.g., `20m`. A QSpice command could be: `.tran 1u 60m 20m 1u`.
- **Action:** Run the simulation.
- **Analysis:** Plot the output voltage (e.g., `V(vp1)`).

- **Determine:**
  - $K_{vg}$ using the equation above by measuring the steady-state output voltage before and after the input step.
  - The maximum peak-to-peak output voltage deviation $\Delta v$ during the transient.
  - The steady state error, *SSE*, which is $|v_{\text{final}} - v_0|$ (the absolute difference between the steady-state output values before and after the input change).

4. $K_{vd}$**:** To determine constant $K_{vd}$ we'll use a different input to that of task (3). A sinusoidal input at a low frequency, much lower than the low pass filter corner frequency, will drive the input of the modulator and the resulting sinusoidal output voltage of the converter will be monitored. To be clear about this, determine the filter corner frequency expressed in *Hz*. The sinusoidal source is attached as shown in Figure 8

   - **Action:**
     - Open the QSpice circuit file that includes a sinusoidal voltage source at the control input of the PWM comparator (e.g., shown in Figure 8).
     - Ensure the main input voltage (V1) is back to its constant DC value (e.g., 10V) and does not have the step changes from Task 3.
   - **Sinusoidal Source Parameters** (e.g., V2 in Figure 8):
     - *Peak Amplitude:* `0.2V`
     - *Frequency:* `100Hz`
     - *Phase:* `0 degrees`
     - *DC offset:* `2.5V` (This is crucial. The control voltage $v_c(t)$ should be $V_{\text{control\_DC}} + \hat{v}_c(t)\sin(\omega t)$. In the QSpice schematic shown in Figure 8, a DC source like V4 provides the 2.5V DC offset, and an AC source like V2 provides the sinusoidal variation. These are summed at the comparator input, effectively creating $v_c(t) = 2.5V + 0.2V\sin(2\pi \cdot 100t)$.)
   - **Simulation Parameters:** Use similar simulation parameters as in Task 3 (e.g., `.tran 1u 60m 20m 1u`), ensuring the simulation runs long enough to capture several cycles of the 100Hz sinusoid.
   - **Action:** Run the simulation.
   - **Analysis:**
     - Plot the driving sinusoidal control voltage (e.g., the voltage at the non-inverting input of the comparator, `V(in+)` if labeled, or the node where the AC and DC control components sum). Confirm its amplitude and frequency.

- Add a plot of the output voltage (e.g., `V(vp2)` if that's the output node in Figure 8).
- Measure the peak-to-peak amplitudes of the input control sinusoid ($\hat{v}_{c,pp}$) and the resulting output AC voltage ($\hat{v}_{pp}$).
- Determine the voltage gain: $Gain = \hat{v}_{pp}/\hat{v}_{c,pp}$.
- Note the phase relationship between the two waveforms. Are they in-phase or out-of-phase?

- **Determine $K_{vd}$:** Recall $\frac{\hat{v}}{\hat{v}_c}(s) = G_{PWM} \cdot G_{vd}(s)$. At a low frequency (100Hz), well below the LPF corner frequency, $G_{LPF}(s) \approx 1$. So, $G_{vd}(s) \approx K_{vd}$. Therefore, the measured $Gain \approx G_{PWM} \cdot K_{vd}$. With $G_{PWM} = 1/V_M$ (where $V_M$ is the peak amplitude of the sawtooth ramp, which is 5V from the PWL source in your QSpice circuits: e.g., (PWL REPEAT FOREVER 0 0 24.95u 5 25u 0 ENDREPEAT), you can calculate $K_{vd}$.

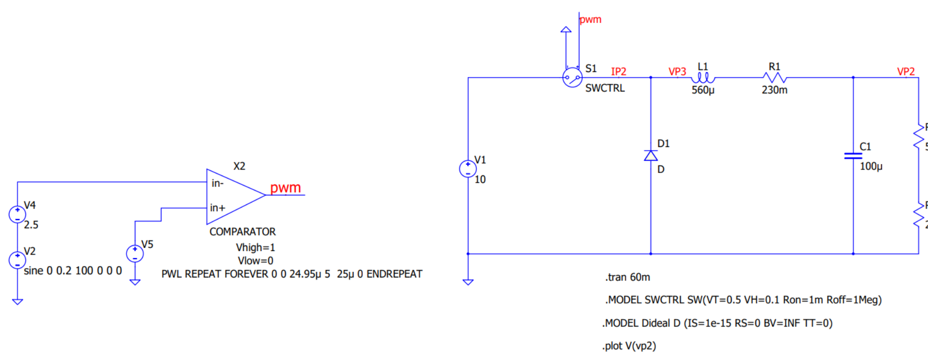



Figure 8: QSpice schematic: Buck converter with pulse width modulator driven by a sinusoidal voltage source.

5. **Step load change:** We next examine the output voltage change to a step in load. This test can be easily performed for an actual circuit and so will be undertaken subsequently on the hardware in the lab and will form the basis for examining how well the application of feedback improves on the open loop performance.

   Alter the buck converter QSpice circuit by adding a switch which is controlled by a pulse source as shown in Figure 9 .

   - **Action:**
     - Open the QSpice circuit file designed for step load changes (e.g., shown in Figure 9).

- In this circuit, a switch (e.g., S2) controlled by a pulse voltage source (e.g., V2: `PULSE(0 10 30m 1u 1u 10m 100m)`) is used to switch an additional load resistor (e.g., R3) in or out of the circuit.
- Ensure the initial state of the added switch (S2) correctly reflects the intended operation. The PULSE source parameters for V2 will control this. For `PULSE(Vinitial Von Vdelay Trise Tfall Ton Tperiod)`:
  * `Vinitial=0` (switch S2 initially controlled by low signal, likely OFF if SWCTRL model uses VT $> 0$)
  * `Von=10` (switch S2 controlled by high signal, likely ON)
  * `Vdelay=30m` (delay before pulse starts)
  * `Trise=1u`, `Tfall=1u` (very fast rise/fall)
  * `Ton=10m` (duration of the pulse, load R3 is switched in)
  * `Tperiod=100m` (pulse period, though only one pulse may matter depending on simulation stop time).
- Make sure no other step changes (like input voltage steps from Task 3) are active. The main input voltage (V1) should be a constant DC.

- **Simulation Parameters:** A command like `.tran 1u 55m 25m` (Stop time 55ms, Start saving data at 25ms) seems appropriate for the circuit in Figure 9. This ensures the system is in steady-state before the load change (e.g., at 30ms).
- **Action:** Run the simulation.
- **Analysis:** Plot the output voltage (e.g., `V(vp2)` if that's the output node in Figure 9).
- **Determine:** From this plot, determine the maximum peak-to-peak output voltage deviation, $\Delta v$, and the steady state error, *SSE*, resulting from the load change.

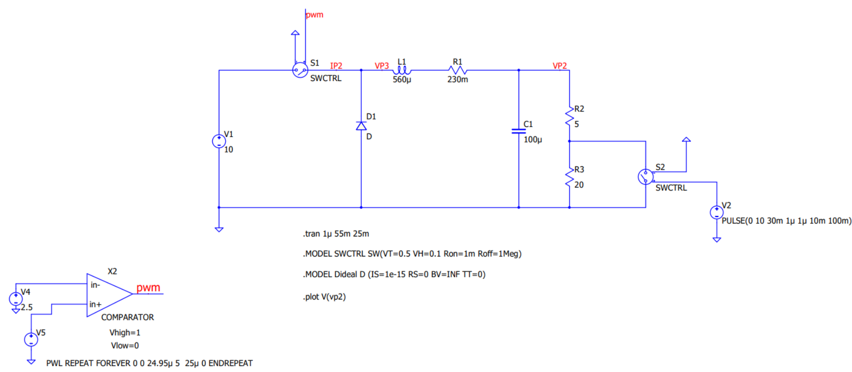



Figure 9: QSpice schematic: Buck converter with step load changes.

### Matlab

In the following tasks we will analyze the open-loop system using Matlab. We'll examine both disturbance input transfer functions and also use Matlab to perform time-domain simulations based on these transfer functions. In the model for the PWM modulator use a peak-to-peak ramp amplitude value of $V_M = 5$.

**Transfer functions**

1. **Loop gain:** Under the condition that there is no compensator, i.e. $G_c = 1$ and the desired output voltage and reference voltages are, $V = 5$ and $V_{ref} = 2.5$, respectively so that $H(s) = \frac{V_{ref}}{V} = \frac{2.5}{5} = 0.5$, determine the loop gain transfer function and use the Matlab *margin* command to obtain the Bode plot of this (uncompensated) loop gain. Have the plot display frequency in Hz. The command will also obtain the unity gain and $-180°$ phase crossover frequencies and the phase and gain margins of the system. Make note of these in your report. Matlab code to do this:

```
s = tf('s');
G_loop = ?; % input your loop gain expression as a function of
s
figure(1)
margin(G_loop)
h = gcr;
h.AxesGrid.Xunits = 'Hz'; % display the frequency in Hz
h.AxesGrid.TitleStyle.FontSize=12; % increase font size
h.AxesGrid.XLabelStyle.FontSize=12; % for readability
h.AxesGrid.YLabelStyle.FontSize=12;
```

2. **Input voltage to output voltage:** Using the model for the (open-loop) input source voltage to output voltage transfer function, $G_{vg}$, use the Matlab *bodemag* command to obtain the magnitude frequency response of this transfer function (with frequency in Hz).

3. **Output current to output voltage:** Using the model for the (open-loop) output current to output voltage transfer function, $-Z_{out}$, use the Matlab *bodemag* command to obtain the magnitude frequency response of this transfer function (with frequency in Hz).

   Be sure to include your Matlab code for (b) and (c) in your report. These magnitude responses show the gain at various frequencies of input disturbance in propagating to the output. With the subsequent incorporation of feedback these responses will be greatly reduced. Ideally we would like the response to be zero across all frequencies. Needless to say that this cannot be achieved perfectly in practice.

   **Open-loop simulations:**

   Note that the following simulations obtained using Matlab are based on the small-signal model only. Thus DC conditions and large signal effects are not modelled and consequently do not show up in the simulations. In order to more easily compare the Matlab simulations with those obtained from QSPICE we will simply add the average converter output voltage to the response obtained from Matlab.

4. **Input voltage step response:** Use the transfer function obtained above for $G_{vg}$ to obtain the response to 10% step input voltage change. Since the nominal input voltage level is *10* V, we therefore will use a unit step input. Use the Matlab *lsim* command to perform this simulation. Determine the maximum peak-to-peak output voltage deviation, $\Delta v$, and steady state error, *SSE*. Matlab code to do this:

```
Vg = 10;
D = 0.5;
V = D*Vg;
s = tf('s');
Gvg = ?  ; % input your expression for Gvg as a function of s
t = linspace(0.02, 0.06, 1000);
u = zeros(size(t));
ind = find(t>=0.025 & t<=0.04);% step is between 0.025<t<0.04
Vg_diff = 1;
```

```
u(ind) = u(ind) + Vg_diff;% form input vector containing the step
figure(2)
y = lsim(Gvg, u, t); % simulate the step response
plot(t,y+V) % add steady state voltage to the output and plot it
del_v = max(y) - min(y) % peak-to-peak voltage deviation
SSE = y(ind(end)) % steady state error
```

5. **Output current step response:** Based on discussion in a prior section of this lab, determine the converter output impedance, $Z_{out}$. We will use the transfer function $-Z_{out}$ to obtain the response for a step load change. In order for this to mimic the practical circuit as closely as possible you will first determine the value of the current step involved. Taking note of the load switching circuit shown in Figure 9, we see that the load switches between 25 ohm and 5 ohms. This results in the output current switching between $I_{o\_1} = \frac{V}{25}$ and $I_{o\_2} = \frac{V}{5}$, where we have assumed that the output voltage does not change appreciably. Thus the current step is $I_{o\_diff} = I_{o\_2} - I_{o\_1}$.

   Use the Matlab *lsim* command to perform a step response simulation to this load step. Determine the maximum peak-to-peak output voltage deviation, $\Delta v$, and steady state error, *SSE*. Matlab code to do this:

```
s = tf('s');
Zout = ?  ; % input your expression for Zout as a function of s
Vg = 10;
D = 0.5;
V = D*Vg;
Io_1 = V/25; % load current before step.  (25 ohm load)
Io_2 = V/5; % load current after step.  (5 ohm load)
Io_diff = Io_2 - Io_1; % current step
t = linspace(0.02, 0.06, 1000);
u = zeros(size(t));
ind = find(t>=0.025 & t<=0.04);% step is between 0.025<t<0.04
u(ind) = u(ind) + Io_diff;
figure(3)
y = lsim(-Zout, u, t);
plot(t,y+V)
del_v = max(y) - min(y)
SSE = y(ind(end))
```

## 0.5 Note

**Computing maximum peak-to-peak output voltage deviation, $\Delta v$, and steady state error, *SSE*:**

With reference to Figure 10 we see that the output voltage before the input step is at 5 V (see value at time = 0.2646). The input step occurs at time 0.30 causing the output to oscillate between max and min values of 5.996 and 3.199 before settling to new steady state output value of 4.816. Subsequently the input step reverts to its initial value at time 0.34 resulting in oscillations occurring between max and min values of 6.617 and 3.82. The quantity $\Delta v$ is determined as the difference between the maximum and minimum deviations in the step response, so that $\Delta v = 6.617 - 3.199 = 3.418$ V. The *SSE* (steady state error) is determined as the difference in the two steady state values, so that $SSE = 5.0 - 4.816 = 0.1840$ V.

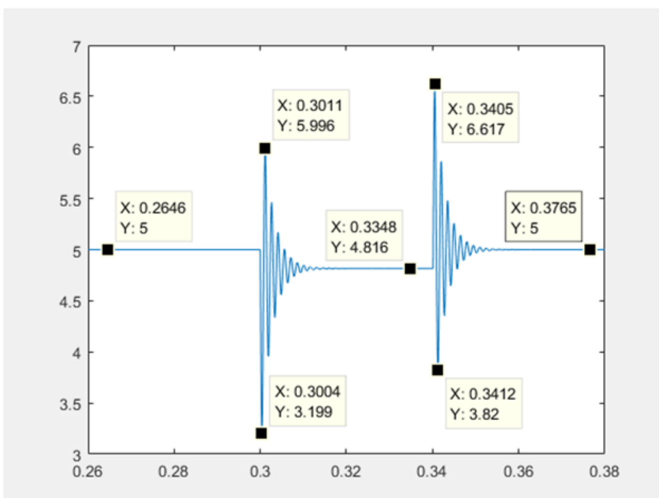



Figure 10: The plot shows the output voltage response to an input step change. This response is used to determine the maximum peak-to-peak output voltage deviation, $\Delta v$, and steady state error, *SSE*.

## 0.6 Results

Be sure to include a summary of your results by completing the following tables and including them in your report.

Transfer function DC gains:

| | From QSPICE: Tasks (3) and (4) | From model: Symbolic Model | From model: Symbolic formula evaluated |
|---|---|---|---|
| $K_{vg}$ | | | |
| $K_{vd}$ | | | |

Uncompensated stability margins and associated frequencies, from Task 6a:

| Gain Margin | Phase Crossover Frequency | Phase Margin | Gain Crossover Frequency |
|---|---|---|---|
| | | | |

Step response characteristics:

| | QSPICE Tasks (3) and (5) | Matlab Tasks (6d) and (6e) |
|---|---|---|
| $v_g$ step: $\Delta v$ | | |
| $v_g$ step: $SSE$ | | |
| $i_{out}$ step: $\Delta v$ | | |
| $i_{out}$ step: $SSE$ | | |

Provide answers to the following questions regarding the step response results:

1. Comparison of the results for $\Delta v$ for $i_{out}$ step changes obtained from QSPICE and Matlab differ more than one might expect. Provide a reason why. (Hint: look closely to how this is modelled).

2. From basic circuit considerations provide a simple symbolic expression for the *SSE* quantity found for a step in input voltage, $v_g$.

## 0.7 Postscript

In this lab we have developed a linear model for the buck converter system which resulted in deriving three transfer functions: 1) $G_{vd}$, 2) $G_{vg}$ and 3) $-Z_{out}$. These transfer functions quantify how the duty ratio control input, $\hat{d}$, and other (disturbance) inputs, $\hat{v}_g$ and $\hat{i}_o$, cause output voltage variations, $\hat{v}$. The pulse width modulator 'describing function' is much more involved to determine despite the simplicity of the final result being a constant, which was given here without further discussion. Together with transfer function, $G_{vd}$, the control voltage, $\hat{v}_c$, to output, $\hat{v}$, transfer function can be determined.

Through simulations, both at a circuit level (using QSPICE) and at a transfer function level (using Matlab), the model has been confirmed.

In subsequent labs a hardware implementation of these circuits will be examined with the final goal of designing an effective compensator for closed loop feedback control.