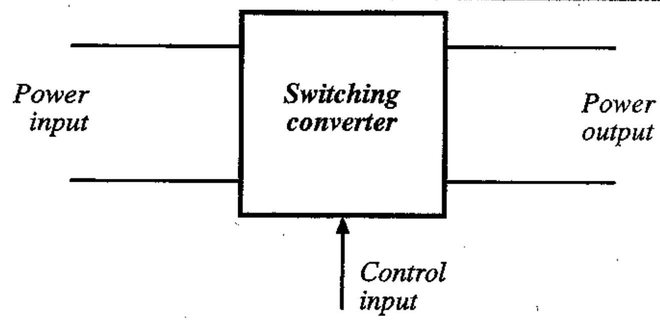
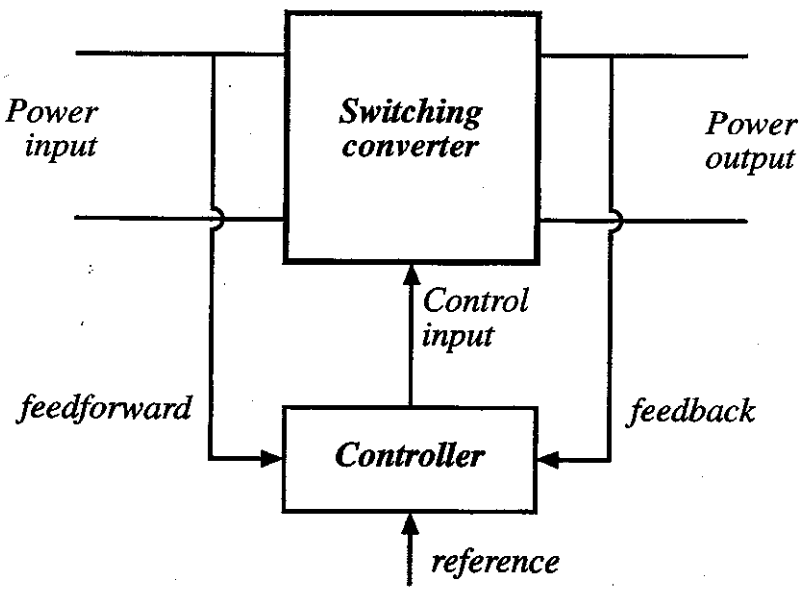
A CONTROL APPLICATION AREA

Introduction to Power Processing

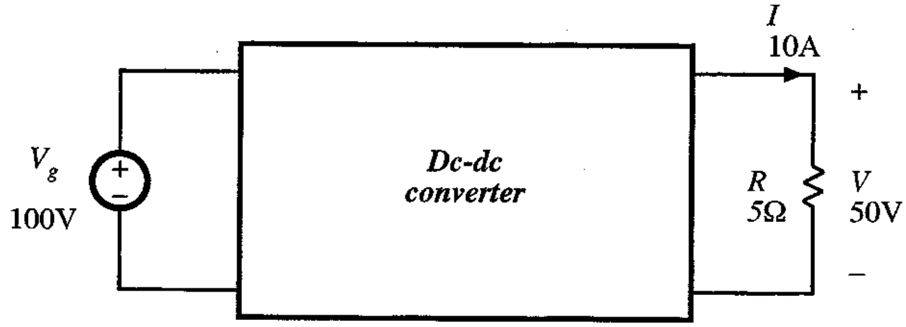


Dc-dc conversion:	Change and control voltage magnitude
Ac-dc rectification:	Possibly control dc voltage, ac current
Dc-ac inversion:	Produce sinusoid of controllable magnitude and frequency
Ac-ac cycloconversion:	Change and control voltage magnitude and frequency

Control is invariably required



A simple dc-dc converter example



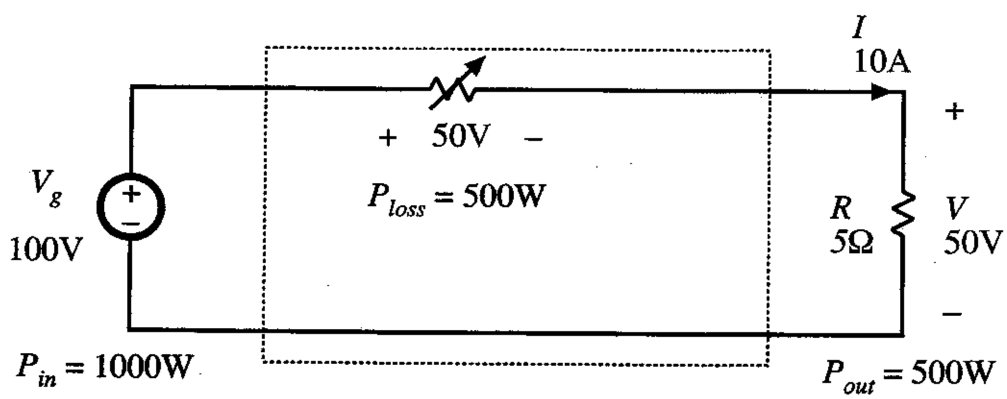
Input source: 100V

Output load: 50V, 10A, 500W

How can this converter be realized?

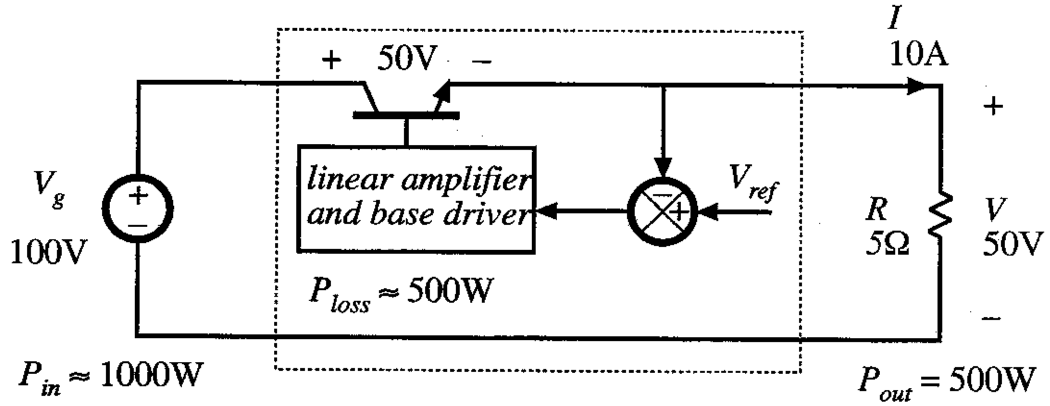
Dissipative realization

Resistive voltage divider

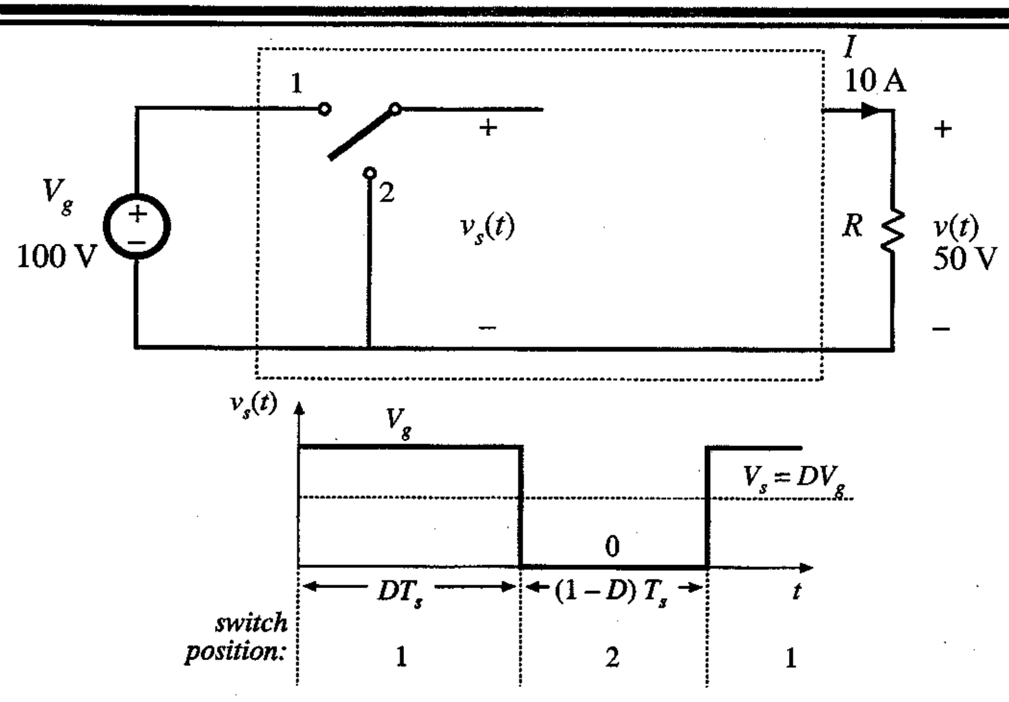


Dissipative realization

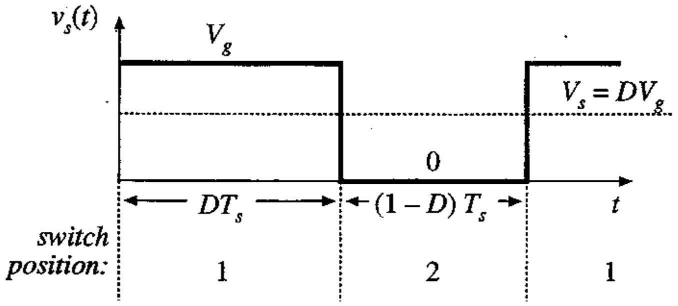
Series pass regulator: transistor operates in active region



Use of a SPDT switch



The switch changes the dc voltage level



D = switch duty cycle
$0 \le D \le 1$

T_s = switching period

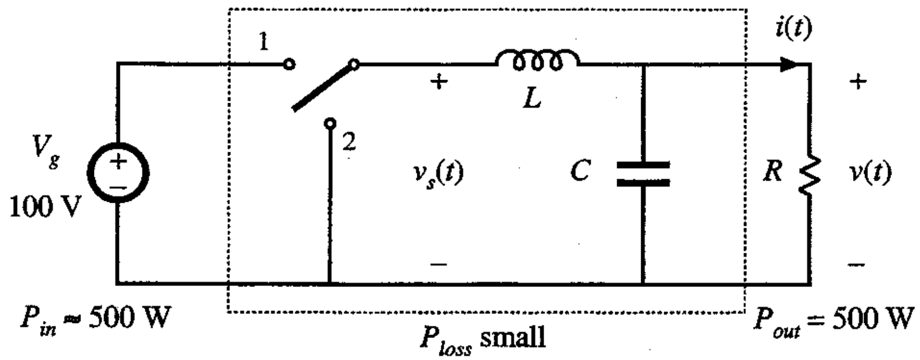
f_s = switching frequency
$= 1 / T_s$

DC component of $v_s(t)$ = average value:

$$V_s = \frac{1}{T_s}\int_0^{T_s} v_s(t)\,dt = DV_g$$

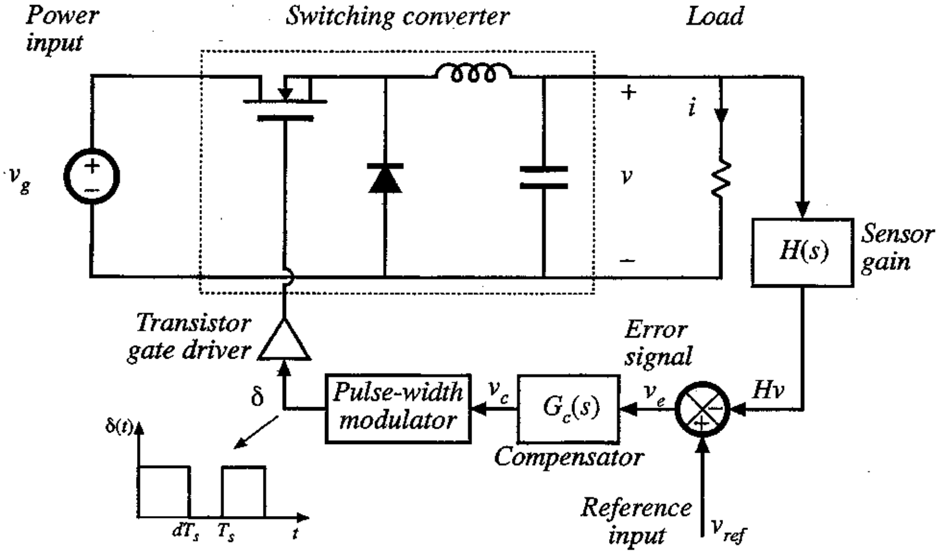
Addition of low pass filter

Addition of (ideally lossless) L-C low-pass filter, for removal of switching harmonics:

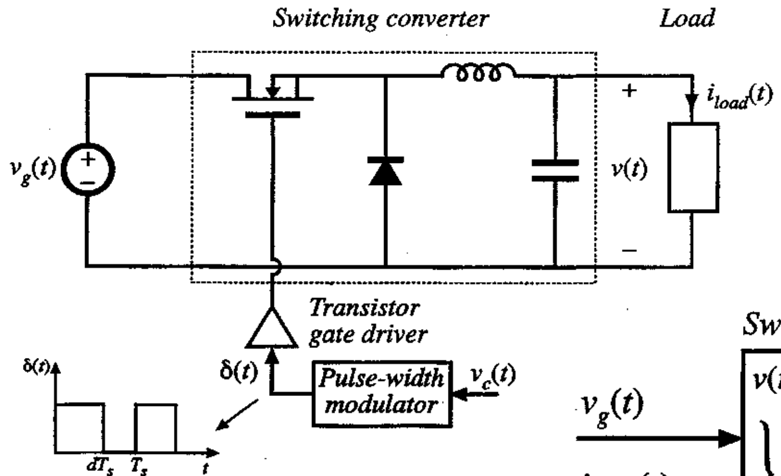


- Choose filter cutoff frequency f_0 much smaller than switching frequency f_s
- This circuit is known as the "buck converter"

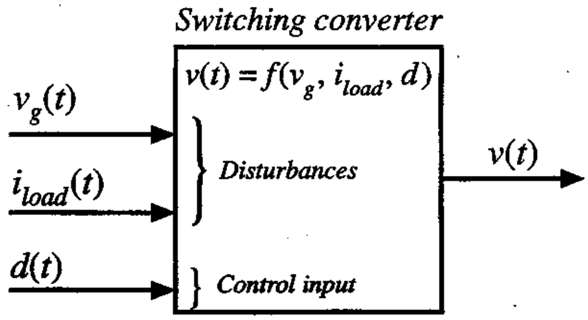
Addition of control system for regulation of output voltage



Introduction



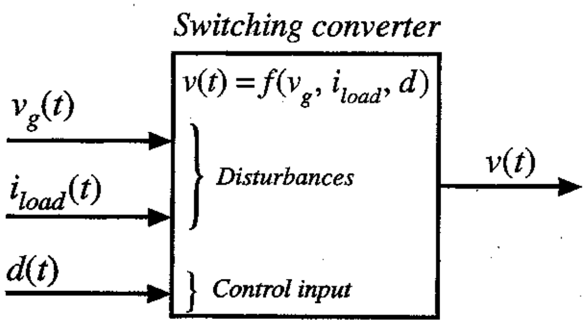
Output voltage of a switching converter depends on duty cycle d, input voltage v_g, and load current i_{load}.



The dc regulator application

Objective: maintain constant output voltage $v(t) = V$, in spite of disturbances in $v_g(t)$ and $i_{load}(t)$.

Typical variation in $v_g(t)$: 100Hz or 120Hz ripple, produced by rectifier circuit.



Load current variations: a significant step-change in load current, such as from 50% to 100% of rated value, may be applied.

A typical output voltage regulation specification: $5\text{V} \pm 0.1\text{V}$.

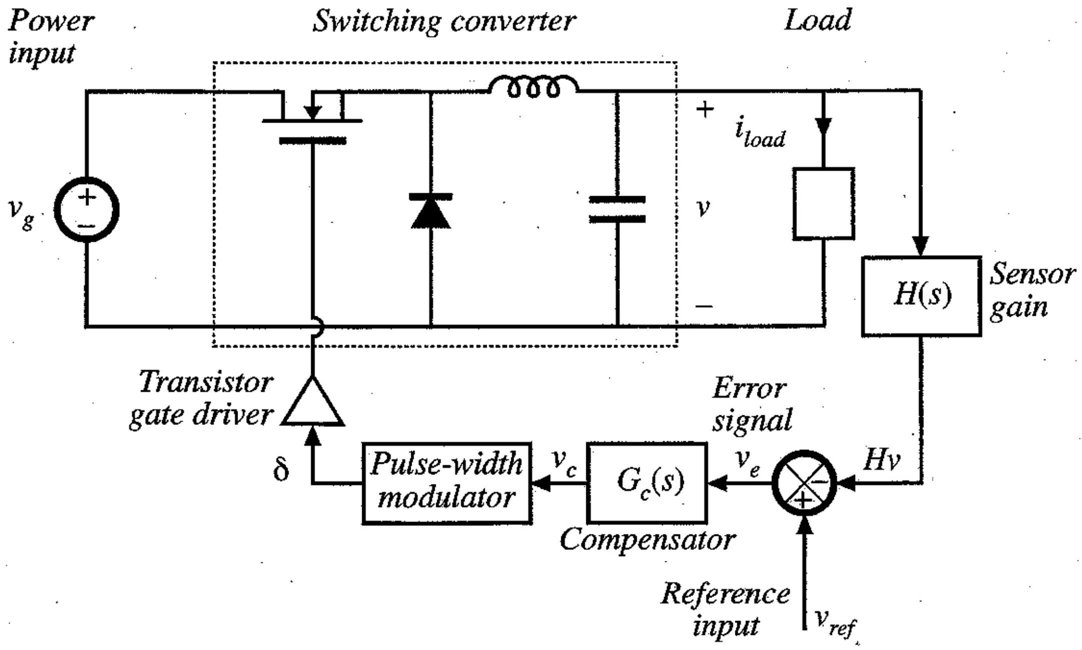
Circuit elements are constructed to some specified tolerance. In high volume manufacturing of converters, all output voltages must meet specifications.

The dc regulator application

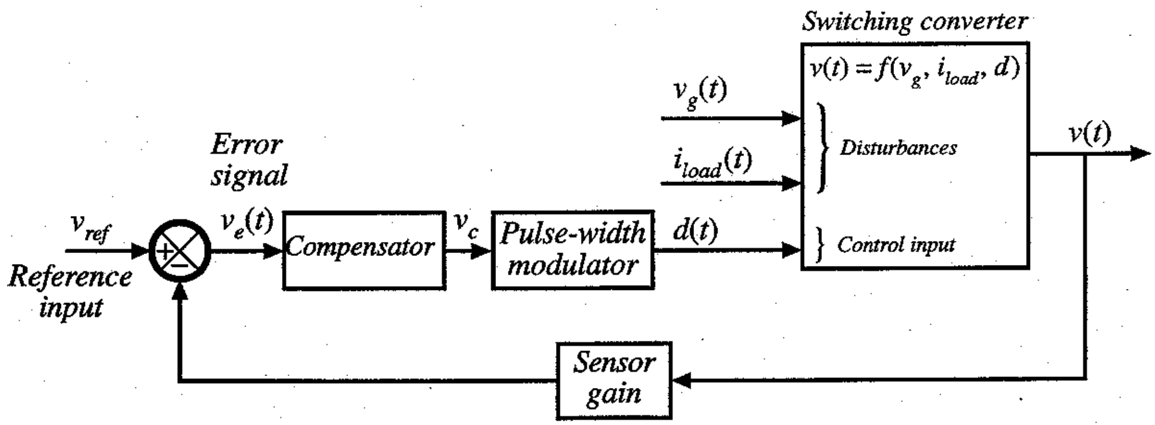
So we cannot expect to set the duty cycle to a single value, and obtain a given constant output voltage under all conditions.

Negative feedback: build a circuit that automatically adjusts the duty cycle as necessary, to obtain the specified output voltage with high accuracy, regardless of disturbances or component tolerances.

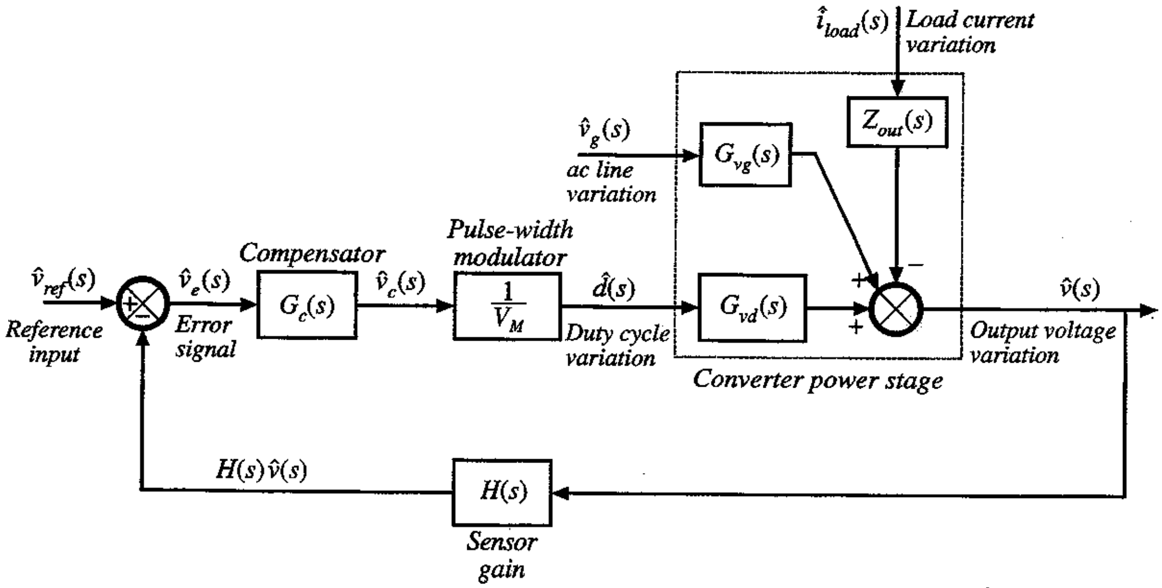
Negative feedback:
a switching regulator system



Negative feedback



Regulator system small-signal block diagram



Solution of block diagram

Manipulate block diagram to solve for $\hat{v}(s)$. Result is

$$\hat{v} = \hat{v}_{ref} \frac{G_c G_{vd} / V_M}{1 + H G_c G_{vd} / V_M} + \hat{v}_g \frac{G_{vg}}{1 + H G_c G_{vd} / V_M} - \hat{i}_{load} \frac{Z_{out}}{1 + H G_c G_{vd} / V_M}$$

which is of the form

$$\hat{v} = \hat{v}_{ref} \frac{1}{H} \frac{T}{1+T} + \hat{v}_g \frac{G_{vg}}{1+T} - \hat{i}_{load} \frac{Z_{out}}{1+T}$$

with $T(s) = H(s)\, G_c(s)\, G_{vd}(s) / V_M$ = *"loop gain"*

Loop gain $T(s)$ = products of the gains around the negative feedback loop.

Feedback reduces the transfer functions from disturbances to the output

Original (open-loop) line-to-output transfer function:

$$G_{vg}(s) = \left. \frac{\hat{v}(s)}{\hat{v}_g(s)} \right|_{\substack{\hat{d}=0 \\ \hat{i}_{load}=0}}$$

With addition of negative feedback, the line-to-output transfer function becomes:

$$\left. \frac{\hat{v}(s)}{\hat{v}_g(s)} \right|_{\substack{\hat{v}_{ref}=0 \\ \hat{i}_{load}=0}} = \frac{G_{vg}(s)}{1+T(s)}$$

Feedback reduces the line-to-output transfer function by a factor of

$$\frac{1}{1+T(s)}$$

If $T(s)$ is large in magnitude, then the line-to-output transfer function becomes small.

Closed-loop output impedance

Original (open-loop) output impedance:

$$Z_{out}(s) = - \left. \frac{\hat{v}(s)}{\hat{i}_{load}(s)} \right|_{\substack{\hat{d}=0 \\ \hat{v}_g=0}}$$

With addition of negative feedback, the output impedance becomes:

$$\left. \frac{\hat{v}(s)}{-\hat{i}_{load}(s)} \right|_{\substack{\hat{v}_{ref}=0 \\ \hat{v}_g=0}} = \frac{Z_{out}(s)}{1+T(s)}$$

Feedback reduces the output impedance by a factor of

$$\frac{1}{1+T(s)}$$

If $T(s)$ is large in magnitude, then the output impedance is greatly reduced in magnitude.

Feedback causes the transfer function from the reference input to the output to be insensitive to variations in the gains in the forward path of the loop

Closed-loop transfer function from $\hat{v}_{ref}$ to $\hat{v}(s)$ is:

$$\left.\frac{\hat{v}(s)}{\hat{v}_{ref}(s)}\right|_{\substack{\hat{v}_g=0 \\ \hat{i}_{load}=0}} = \frac{1}{H(s)} \frac{T(s)}{1+T(s)}$$

If the loop gain is large in magnitude, i.e., $\| T \| >> 1$, then $(1+T) \approx T$ and $T/(1+T) \approx T/T = 1$. The transfer function then becomes

$$\frac{\hat{v}(s)}{\hat{v}_{ref}(s)} \approx \frac{1}{H(s)}$$

which is independent of the gains in the forward path of the loop.

This result applies equally well to dc values:

$$\frac{V}{V_{ref}} = \frac{1}{H(0)} \frac{T(0)}{1+T(0)} \approx \frac{1}{H(0)}$$

Regulator design

Typical specifications:

- Effect of load current variations on output voltage regulation

  This is a limit on the maximum allowable output impedance

- Effect of input voltage variations on the output voltage regulation

  This limits the maximum allowable line-to-output transfer function

- Transient response time

  This requires a sufficiently high crossover frequency

- Overshoot and ringing

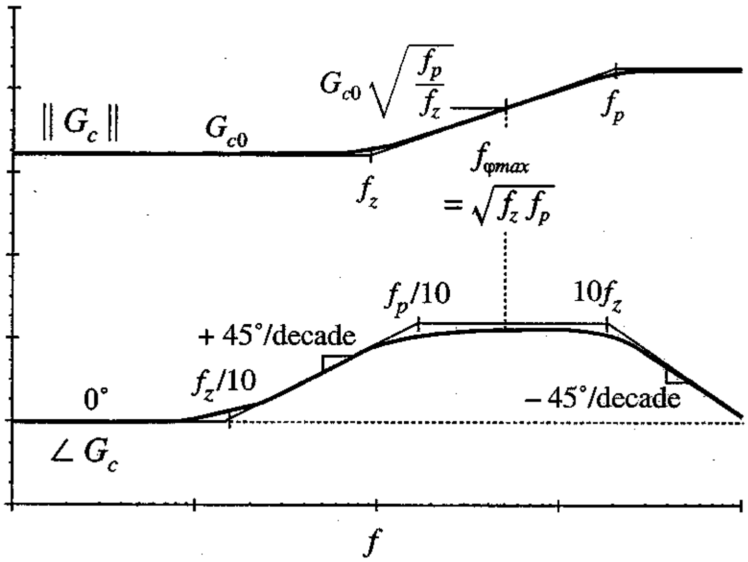
  An adequate phase margin must be obtained

The regulator design problem: add compensator network $G_c(s)$ to modify $T(s)$ such that all specifications are met.

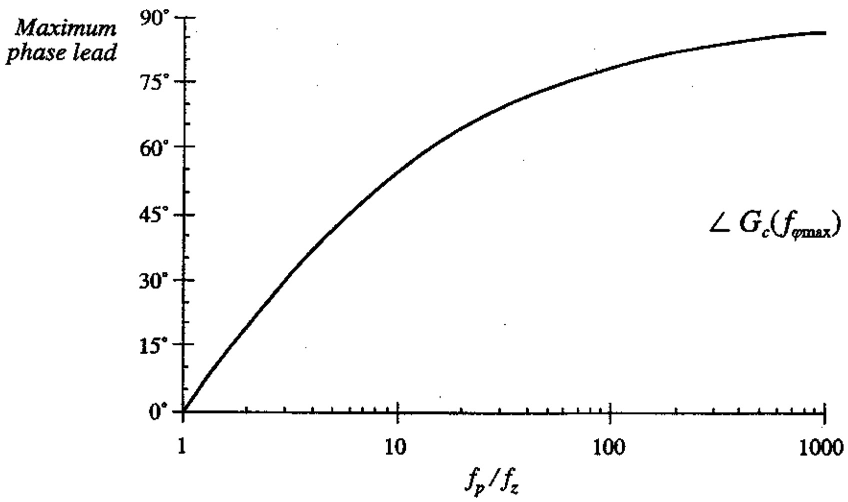
Lead (PD) compensator

$$G_c(s) = G_{c0}\frac{\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_p}\right)}$$

Improves phase margin



Lead compensator: maximum phase lead



$$f_{\varphi max} = \sqrt{f_z f_p}$$

$$\angle G_c(f_{\varphi max}) = \tan^{-1}\left(\frac{\sqrt{\frac{f_p}{f_z}} - \sqrt{\frac{f_z}{f_p}}}{2}\right)$$

$$\frac{f_p}{f_z} = \frac{1+\sin(\theta)}{1-\sin(\theta)}$$

Lead compensator design

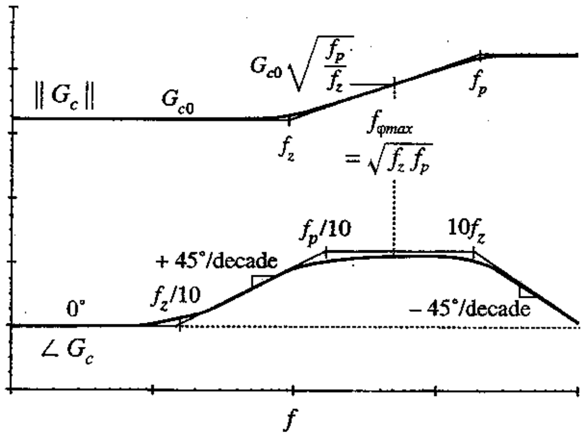
To optimally obtain a compensator phase lead of θ at frequency f_c, the pole and zero frequencies should be chosen as follows:

$$f_z = f_c \sqrt{\frac{1-\sin(\theta)}{1+\sin(\theta)}}$$

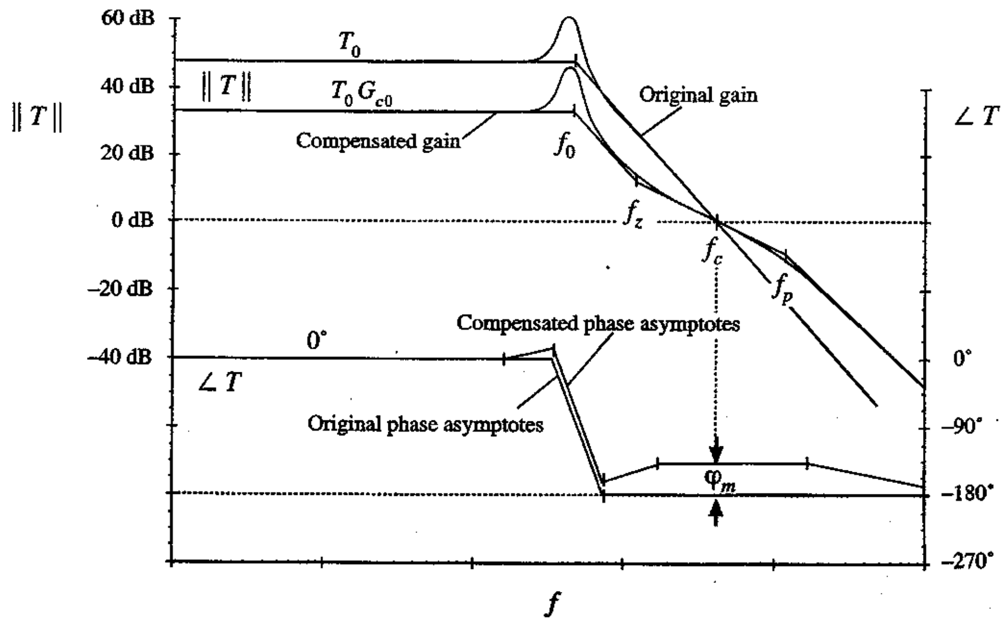
$$f_p = f_c \sqrt{\frac{1+\sin(\theta)}{1-\sin(\theta)}}$$

If it is desired that the magnitude of the compensator gain at f_c be unity, then G_{c0} should be chosen as

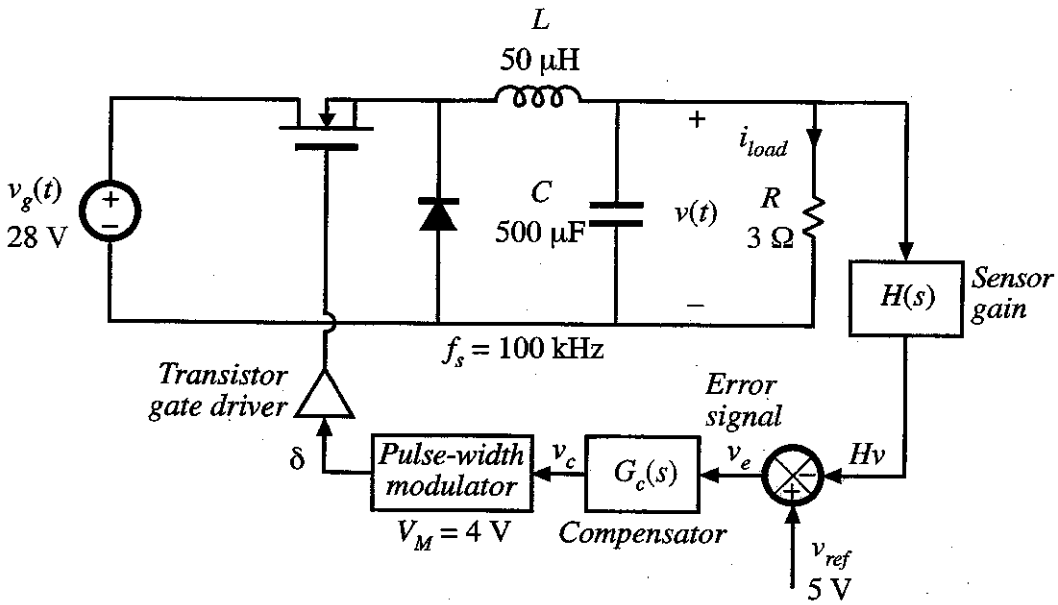
$$G_{c0} = \sqrt{\frac{f_z}{f_p}}$$



Example: lead compensation



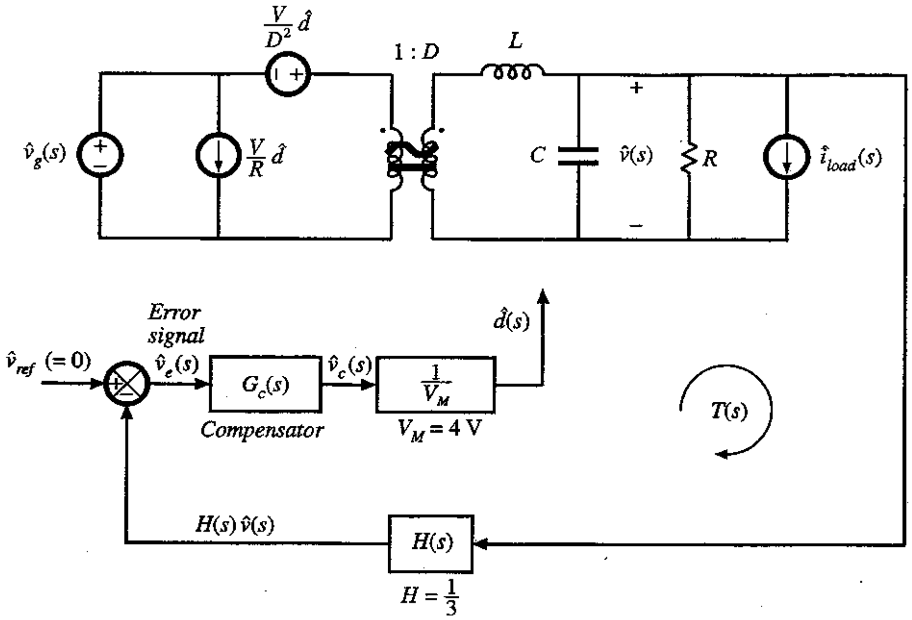
Design example



Quiescent operating point

Input voltage	$V_g = 28\text{V}$
Output	$V = 15\text{V},\ I_{load} = 5\text{A},\ R = 3\Omega$
Quiescent duty cycle	$D = 15/28 = 0.536$
Reference voltage	$V_{ref} = 5\text{V}$
Quiescent value of control voltage	$V_c = DV_M = 2.14\text{V}$
Gain $H(s)$	$H = V_{ref}/V = 5/15 = 1/3$

Small-signal model



Open-loop control-to-output transfer function $G_{vd}(s)$

$$G_{vd}(s) = \frac{V}{D}\frac{1}{1 + s\frac{L}{R} + s^2LC}$$

standard form:

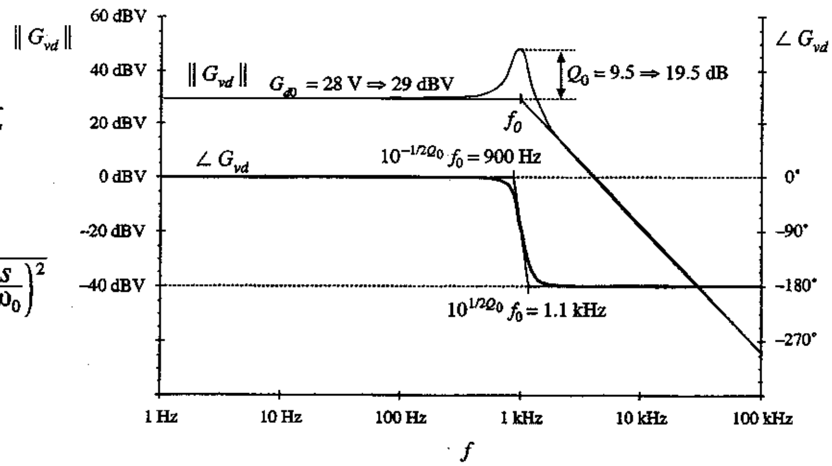
$$G_{vd}(s) = G_{d0}\frac{1}{1 + \frac{s}{Q_0\omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

salient features:

$$G_{d0} = \frac{V}{D} = 28\text{V}$$

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{LC}} = 1\text{kHz}$$

$$Q_0 = R\sqrt{\frac{C}{L}} = 9.5 \Rightarrow 19.5\text{dB}$$



Open-loop line-to-output transfer function and output impedance

$$G_{vg}(s) = D \frac{1}{1 + s\frac{L}{R} + s^2 LC}$$

—same poles as control-to-output transfer function standard form:

$$G_{vg}(s) = G_{g0} \frac{1}{1 + \frac{s}{Q_0 \omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

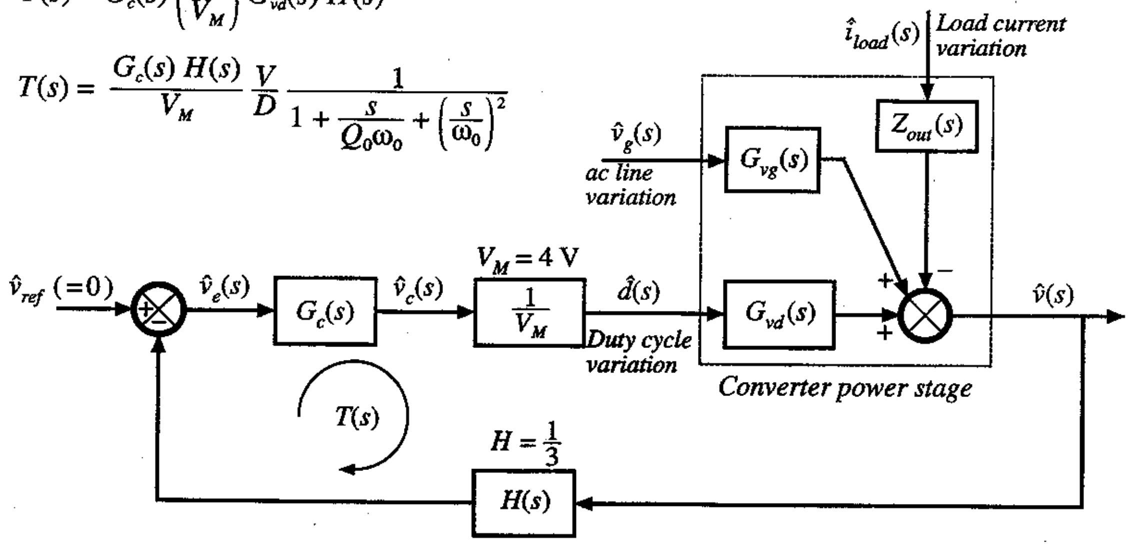
Output impedance:

$$Z_{out}(s) = R \parallel \frac{1}{sC} \parallel sL = \frac{sL}{1 + s\frac{L}{R} + s^2 LC}$$

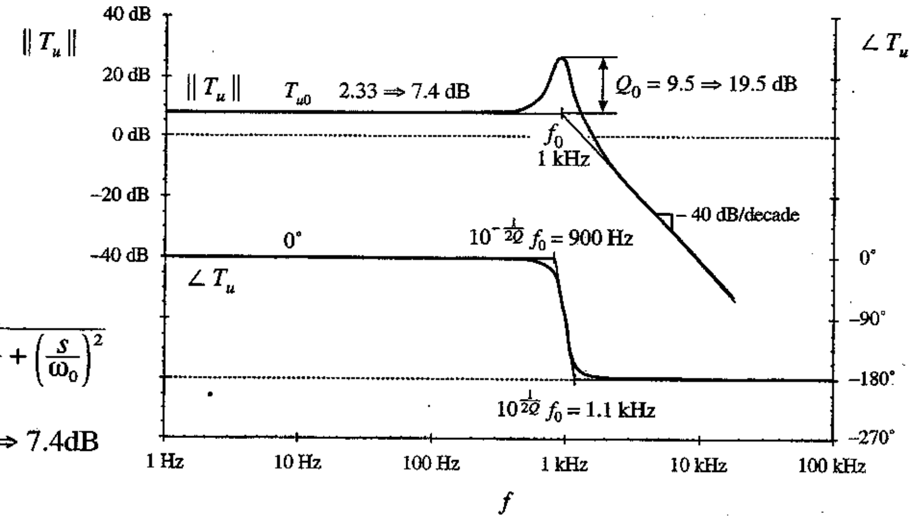
System block diagram

$$T(s) = G_c(s) \left(\frac{1}{V_M}\right) G_{vd}(s)\, H(s)$$

$$T(s) = \frac{G_c(s)\, H(s)}{V_M} \frac{V}{D} \frac{1}{1 + \frac{s}{Q_0 \omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$



Uncompensated loop gain (with $G_c = 1$)



With $G_c = 1$, the loop gain is

$$T_u(s) = T_{u0} \frac{1}{1 + \frac{s}{Q_0 \omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

$$T_{u0} = \frac{H}{D} \frac{V}{V_M} = 2.33 \Rightarrow 7.4\text{dB}$$

$f_c = 1.8$ kHz, $\varphi_m = 5°$

Lead compensator design

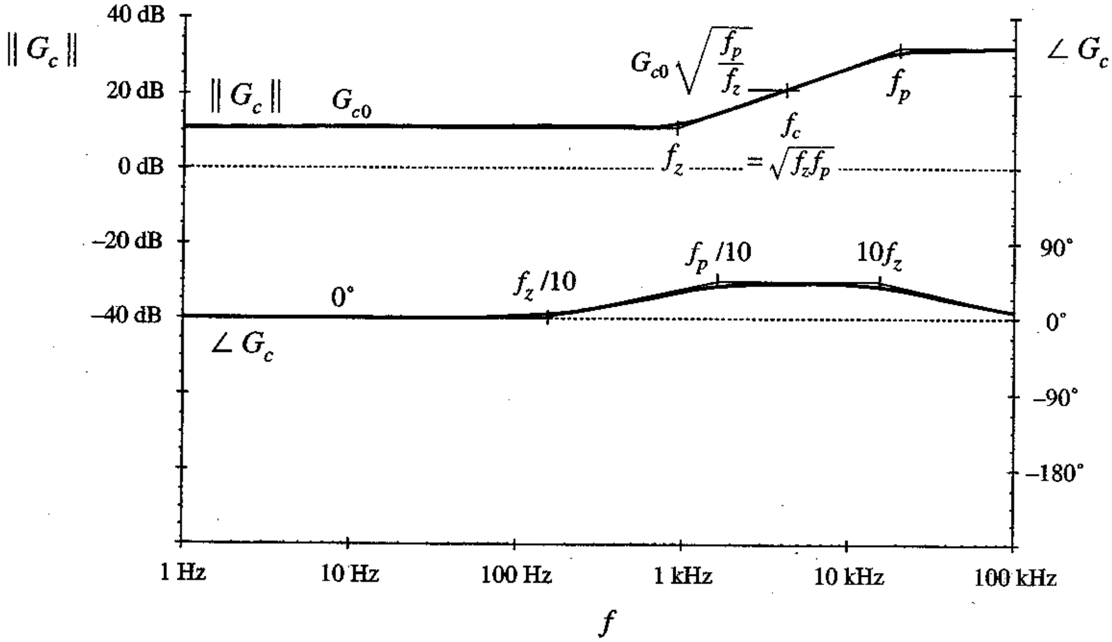
- Obtain a crossover frequency of 5 kHz, with phase margin of 52°
- T_u has phase of approximately – 180° at 5 kHz, hence lead (PD) compensator is needed to increase phase margin.
- Lead compensator should have phase of + 52° at 5 kHz
- T_u has magnitude of – 20.6 dB at 5 kHz
- Lead compensator gain should have magnitude of + 20.6 dB at 5 kHz
- Lead compensator pole and zero frequencies should be

$$f_z = (5\text{kHz}) \sqrt{\frac{1 - \sin(52°)}{1 + \sin(52°)}} = 1.7\text{kHz}$$

$$f_p = (5\text{kHz}) \sqrt{\frac{1 + \sin(52°)}{1 - \sin(52°)}} = 14.5\text{kHz}$$

- Compensator dc gain should be $G_{c0} = \left(\frac{f_c}{f_0}\right)^2 \frac{1}{T_{u0}} \sqrt{\frac{f_z}{f_p}} = 3.7 \Rightarrow 11.3\text{dB}$

Lead compensator Bode plot



Loop gain, with lead compensator

$$T(s) = T_{u0}\, G_{c0} \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)\left(1 + \frac{s}{Q_0\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right)}$$