Introduction to Power Processing

Switching converter

Power input
\[\text{Control input}\]
Power output

- **Dc-dc conversion**: Change and control voltage magnitude
- **Ac-dc rectification**: Possibly control dc voltage, ac current
- **Dc-ac inversion**: Produce sinusoid of controllable magnitude and frequency
- **Ac-ac cycloconversion**: Change and control voltage magnitude and frequency

Control is invariably required

Controller

Feedforward
\[\text{Reference}\]
Feedback
A simple dc-dc converter example

Input source: 100V
Output load: 50V, 10A, 500W
How can this converter be realized?

Dissipative realization

Resistive voltage divider

\[ P_{in} = 1000\text{W} \]

\[ P_{out} = 500\text{W} \]

\[ P_{loss} = 500\text{W} \]
Dissipative realization

Series pass regulator: transistor operates in active region

\[ P_{\text{in}} \approx 1000\text{W} \quad P_{\text{out}} = 500\text{W} \]

Use of a SPDT switch
The switch changes the dc voltage level

\[ V_s \]

\[ v_s(t) \]

\[ V_s = D V_g \]

\[ D = \text{switch duty cycle} \quad 0 \leq D \leq 1 \]

\[ T_s = \text{switching period} \]

\[ f_s = \frac{1}{T_s} = \text{switching frequency} \]

DC component of \( v_s(t) \) = average value:

\[ V_s = \frac{1}{T_s} \int_0^{T_s} v_s(t) \, dt = DV_g \]

Addition of low pass filter

Addition of (ideally lossless) \( L-C \) low-pass filter, for removal of switching harmonics:

- Choose filter cutoff frequency \( f_0 \) much smaller than switching frequency \( f_s \)
- This circuit is known as the "buck converter"
Addition of control system for regulation of output voltage

Introduction

Output voltage of a switching converter depends on duty cycle \( d \), input voltage \( v_g \), and load current \( i_{load} \).
The dc regulator application

Objective: maintain constant output voltage $v(t) = V$, in spite of disturbances in $v_g(t)$ and $i_{load}(t)$.

Typical variation in $v_g(t)$: 100Hz or 120Hz ripple, produced by rectifier circuit.

Load current variations: a significant step-change in load current, such as from 50% to 100% of rated value, may be applied.

A typical output voltage regulation specification: 5V ± 0.1V.

Circuit elements are constructed to some specified tolerance. In high volume manufacturing of converters, all output voltages must meet specifications.

The dc regulator application

So we cannot expect to set the duty cycle to a single value, and obtain a given constant output voltage under all conditions.

Negative feedback: build a circuit that automatically adjusts the duty cycle as necessary, to obtain the specified output voltage with high accuracy, regardless of disturbances or component tolerances.
Negative feedback:
a switching regulator system

---

Negative feedback
Regulator system small-signal block diagram

Solution of block diagram

Manipulate block diagram to solve for \( \varphi(s) \). Result is

\[
\varphi = \varphi_{\text{ref}} \frac{G_d G_{vd} / V_M}{1 + H G_d G_{vd} / V_M} + \varphi_s \frac{G_{vd}}{1 + H G_d G_{vd} / V_M} - \dot{i}_{\text{load}} \frac{Z_{\text{out}}}{1 + H G_d G_{vd} / V_M}
\]

which is of the form

\[
\varphi = \varphi_{\text{ref}} \frac{T}{1 + T} + \varphi_s \frac{G_{vd}}{1 + T} - \dot{i}_{\text{load}} \frac{Z_{\text{out}}}{1 + T}
\]

with \( T(s) = H(s) G_d(s) G_{vd}(s) / V_M = \text{"loop gain"} \)

Loop gain \( T(s) = \text{products of the gains around the negative feedback loop.} \)
Feedback reduces the transfer functions from disturbances to the output

Original (open-loop) line-to-output transfer function:

\[ G_{op}(s) = \left. \frac{\hat{v}(s)}{\hat{v}_p(s)} \right|_{\dot{i}_{\text{load}} = 0, \theta = 0} \]

With addition of negative feedback, the line-to-output transfer function becomes:

\[ \left. \frac{\hat{v}(s)}{\hat{v}_p(s)} \right|_{\theta_{\text{ref}} = 0} = \frac{G_{op}(s)}{1 + T(s)} \]

Feedback reduces the line-to-output transfer function by a factor of

\[ \frac{1}{1 + T(s)} \]

If \( T(s) \) is large in magnitude, then the line-to-output transfer function becomes small.

Closed-loop output impedance

Original (open-loop) output impedance:

\[ Z_{out}(s) = -\left. \frac{\hat{v}(s)}{-\hat{i}_{\text{load}}(s)} \right|_{\dot{\theta} = 0, \hat{\theta}_p = 0} \]

With addition of negative feedback, the output impedance becomes:

\[ \left. \frac{\hat{v}(s)}{-\hat{i}_{\text{load}}(s)} \right|_{\theta_{\text{ref}} = 0} = \frac{Z_{out}(s)}{1 + T(s)} \]

Feedback reduces the output impedance by a factor of

\[ \frac{1}{1 + T(s)} \]

If \( T(s) \) is large in magnitude, then the output impedance is greatly reduced in magnitude.
Feedback causes the transfer function from the reference input to the output to be insensitive to variations in the gains in the forward path of the loop.

Closed-loop transfer function from $\dot{v}_{\text{ref}}$ to $\dot{v}(s)$ is:

$$\left. \frac{\dot{v}(s)}{\dot{v}_{\text{ref}}(s) \left| \right.} \right|_{i_\text{load}=0} \left. = \frac{T(s)}{H(s) \left(1 + T(s)\right)} \right.$$

If the loop gain is large in magnitude, i.e., $\|T\| > 1$, then $(1+T) \approx T$ and $T/(1+T) \approx T/T = 1$. The transfer function then becomes

$$\left. \frac{\dot{v}(s)}{\dot{v}_{\text{ref}}(s) \left| \right.} \right|_{i_\text{load}=0} \left. = \frac{1}{H(s)} \right.$$

which is independent of the gains in the forward path of the loop.

This result applies equally well to dc values:

$$\left. \frac{V}{V_{\text{ref}}} \right|_{s=0} = \frac{T(0)}{1 + T(0)} \approx \frac{1}{H(0)}$$

Regulator design

Typical specifications:

- Effect of load current variations on output voltage regulation
  
  This is a limit on the maximum allowable output impedance

- Effect of input voltage variations on the output voltage regulation
  
  This limits the maximum allowable line-to-output transfer function

- Transient response time
  
  This requires a sufficiently high crossover frequency

- Overshoot and ringing
  
  An adequate phase margin must be obtained

The regulator design problem: add compensator network $G_c(s)$ to modify $T(s)$ such that all specifications are met.
Lead (PD) compensator

\[ G_c(s) = G_c(0) \left( \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}} \right) \]

Improves phase margin

\[ f_{q_{\text{max}}} = \sqrt{f_z f_p} \]

Lead compensator: maximum phase lead

\[ f_{q_{\text{max}}} = \sqrt{f_z f_p} \]

\[ \angle G_c(f_{q_{\text{max}}}) = \tan^{-1} \left( \frac{\sqrt{\frac{f_p}{f_z}} - \sqrt{\frac{f_z}{f_p}}}{2} \right) \]

\[ \frac{f_p}{f_z} = \frac{1 + \sin(\theta)}{1 - \sin(\theta)} \]
Lead compensator design

To optimally obtain a compensator phase lead of \( \theta \) at frequency \( f_c \), the pole and zero frequencies should be chosen as follows:

\[
\begin{align*}
    f_z &= f_c \sqrt{\frac{1 - \sin(\theta)}{1 + \sin(\theta)}} \\
    f_p &= f_c \sqrt{\frac{1 + \sin(\theta)}{1 - \sin(\theta)}}
\end{align*}
\]

If it is desired that the magnitude of the compensator gain at \( f_z \) be unity, then \( G_{c0} \) should be chosen as

\[
G_{c0} = \frac{f_z}{f_p}
\]

Example: lead compensation
Design example

Quiescent operating point

Input voltage \( V_s = 28V \)
Output \( V = 15V, I_{load} = 5A, R = 3\Omega \)
Quiescent duty cycle \( D = 15/28 = 0.536 \)
Reference voltage \( V_{ref} = 5V \)
Quiescent value of control voltage \( V_c = DV_M = 2.14V \)
Gain \( H(s) \) \( H = V_{ref}/V = 5/15 = 1/3 \)
Small-signal model

Open-loop control-to-output transfer function $G_{vd}(s)$

\[ G_{vd}(s) = \frac{V}{D} \left( \frac{1}{1 + \frac{sL}{R} + s^2LC} \right) \]

Standard form:

\[ G_{vd}(s) = G_{\infty} \frac{1}{1 + \frac{s}{Q_0 \omega_0} + \left( \frac{s}{\omega_0} \right)^2} \]

Salient features:

- $G_{\infty} = \frac{V}{D} = 28$V
- $f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi \sqrt{LC}} = 1$kHz
- $Q_0 = R \sqrt{\frac{C}{L}} = 9.5 \Rightarrow 19.5$dB
Open-loop line-to-output transfer function and output impedance

\[ G_{w}(s) = D \frac{1}{1 + s\frac{L}{R} + s^2LC} \]

Same poles as control-to-output transfer function standard form:

\[ G_{w}(s) = G_{w0} \frac{1}{1 + \frac{s}{Q_{w} \omega_{0}} + \left(\frac{s}{\omega_{0}}\right)^2} \]

Output impedance:

\[ Z_{\text{out}}(s) = R \parallel \frac{1}{sC} \parallel sL = \frac{sL}{1 + s\frac{L}{R} + s^2LC} \]

System block diagram
Uncompensated loop gain (with \( G_c = 1 \))

\[
T_u(s) = T_{u0} \frac{1}{1 + \frac{s}{Q_0\omega_0} + \left(\frac{s}{\omega_0}\right)^2}
\]

\[
T_{u0} = \frac{H}{D} \frac{V}{V_M} = 2.33 \Rightarrow 7.4\text{dB}
\]

\[
f_c = 1.8\text{ kHz}, \quad \phi_m = 5^\circ
\]

Lead compensator design

- Obtain a crossover frequency of 5 kHz, with phase margin of 52°
- \( T_u \) has phase of approximately \(-180^\circ\) at 5 kHz, hence lead (PD) compensator is needed to increase phase margin.
- Lead compensator should have phase of +52° at 5 kHz
- \( T_u \) has magnitude of \(-20.6\) dB at 5 kHz
- Lead compensator gain should have magnitude of +20.6 dB at 5 kHz
- Lead compensator pole and zero frequencies should be
  \[
f_c = (5\text{kHz}) \sqrt{\frac{1 - \sin (52^\circ)}{1 + \sin (52^\circ)}} = 1.7\text{kHz}
\]
  \[
f_p = (5\text{kHz}) \sqrt{\frac{1 + \sin (52^\circ)}{1 - \sin (52^\circ)}} = 14.5\text{kHz}
\]
- Compensator dc gain should be \( G_0 = \left(\frac{f_c}{f_p}\right)^2 \frac{1}{T_w} \sqrt{\frac{f_c}{f_p}} = 3.7 \Rightarrow 11.3\text{dB} \)
Lead compensator Bode plot

\[ \| G_c \| = \begin{cases} G_{c0} \sqrt{\frac{f_p}{f_z}} & \text{for } f \geq f_p \\ f_z & \text{for } f < f_p \end{cases} \]

\[ \angle G_c = \begin{cases} f_z/10 & \text{for } f \geq f_p \\ 10f_z & \text{for } f < f_p \end{cases} \]

Loop gain, with lead compensator

\[ T(s) = T_0 \cdot G_0 \cdot \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p} \left(1 + s/Q_0 \omega_0 + \left(\frac{s}{\omega_0}\right)^2\right)} \]

\[ \| T \| = 8.6 \Rightarrow 18.7 \text{ dB} \]

\[ Q_0 = 9.5 \Rightarrow 19.5 \text{ dB} \]

\[ \angle T = 0^\circ \text{ at } 900 \text{ Hz} \]

\[ \angle T = 170 \text{ Hz} \text{ at } 14 \text{ kHz} \]

\[ \angle T = 17 \text{ kHz} \text{ at } 1.7 \text{ kHz} \]

\[ \angle T = 14 \text{ kHz} \text{ at } 1 \text{ kHz} \]

\[ \angle T = 1 \text{ kHz} \text{ at } 1.4 \text{ kHz} \]