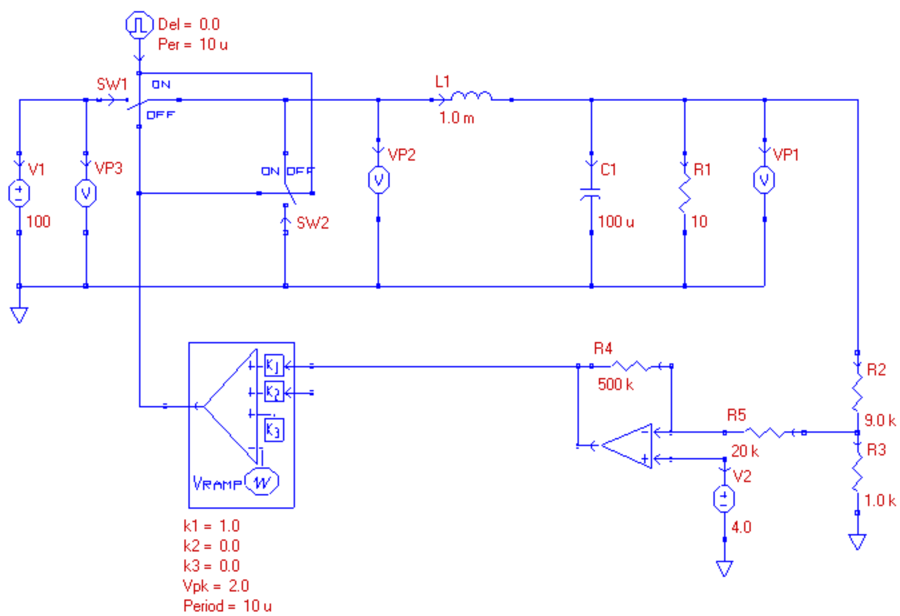
ECE311

Project

Aim: To design a controller for the Buck converter discussed in class and shown below. The performance of your closed loop design is compared with open loop performance and the performance of a proportional compensator design (given below) through simulation. Your designed system performance should improve on the proportional compensator design.

Tasks: The PECS schematic of the Buck regulator is shown below with a *proportional* compensator.



The parameters of the Buck regulator are: V_g = 100*V*, V_{out} = 40*V*, *L*=1 *mH*, $C=100\,\mu F$, V_M =2*V* (V_M is the peak-to-peak amplitude of the sawtooth waveform used in the Pulse Width Modulator (*PWM*), and f_s = 100*kHz*. The reference voltage used is V_{ref} = *4 V*.

The first task to be performed is to determine open loop performance, i.e. without a compensator present. Be sure to set the correct steady state duty cycle value to produce a *40 V* output before stepping the input source. Performance can be assessed by examining the response to a 10% input voltage disturbance in the output. The input voltage should be stepped from *100V* to *110V* to *100V*. This should be performed with a circuit simulator such as PECS.

The step response should also be obtained using the model of the system with Matlab/Simulink. The model used is given in Figure 6.1 on page 84 of the instructor's book. For simplicity you can delete the Z_{out} transfer function block in the figure. The transfer functions used in the figure are shown on page 78 of the instructor's book. This is for both the Buck converter and the PWM.

Design a compensator for the Buck regulator which features at least one pole and one zero in its transfer function. The design methodology to be used is fully explained in the instructor's book specifically in Chapter 3 with further application to the Buck converter in Chapter 6. This methodology involves using asymptotic Bode plot construction of the desired loop gain from which simplified equations may be derived for use in the design process. This methodology does not inherently rely on trial and error iteration and so you are requested not to use such an approach.

You will need to choose an appropriate compensator transfer function (subject to the constraint stated above of having at least one pole and one zero). Extra credit will be given to students who choose a compensator that does *not* appear in Table 6.2 on page 122 of the instructor's book. (I'm hoping to get some novelty from some (if not all) students).

Sketch and fully annotate the magnitude and phase asymptotes of the compensated loop gain as shown in many place in the instructor's book. (Note: providing these plots is an integral part of the design methodology and so it is worth ***50% of the grade*** towards your report).

Determine the compensator parameters from simplified equations derived from you asymptotic plots (a reminder again: do not use a trial and error approach for this). Use Matlab to verify your design using the MARGIN command. Also, obtain a step response of your closed loop system using Matlab/Simulink.

As a final step in the design, implement the compensator as a circuit. The table of compensators on pages 124 and 125 in the instructor's book may be helpful in this regard. Simulate your closed loop system using a circuit based simulator, such as PECS.

Report and Presentation:

Write up a clearly written report presenting your results. Be sure to include all your Matlab/Simulink code. This normally should go into the appendix. (There needs to be complete transparency as to how your results have been produced).

The due date for this is at the start of your presentation to the class during finals week. It should be emailed to the instructor (tymerski@ece.pdx.edu).

In your report be sure to present a cogent summary in your conclusion. Clearly state why your design gives the best performance compared to two benchmarks discussed below.

The following is a non-exhaustive list of items you need to provide in your report:

1) The transfer function of the controller, with the particular pole and zero values determined.
2) Sketch of the magnitude and phase asymptotic Bode plots of the compensated loop gain fully annotated. (this alone is worth **50% of the grade** for the report)
3) A Matlab Bode plot of the loop gain, using the MARGIN command, verifying (2).
4) Step response of your closed loop design using Matlab/Simulink.
5) Step responses of your closed loop system obtained using a circuit simulator (such as PECS).
6) A comparison table similar to Table 6.2 on page 122 of the instructor's book, to show a comparison of performance of three systems:
   i) Open loop system (do not close the loop)
   ii) Closed loop system using proportional control (shown above)
   iii) Your closed loop design

   Feel free to use whatever other performance metrics you like for the comparison.

7) Include all Matlab code and Simulink and circuit simulator (PECS) schematics.