Carbon Nanotube Transistors: Modeling and Circuits

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Low-Power Process-Tolerant and High Performance VLSI Research

- Wireless Communications
  - Low Power
  - Coding / Modulation
- High Speed Arithmetic
  - Sharing Multiplier for Vector Scaling
- Low Complexity
  - Differential / Redundant Coeff.
  - Distributed Multiplication
  - Filter / Image Compression
- Modeling
  - Random Dopant
  - LER
- Self-Calibrating Design
  - Delay sensor
  - Leakage sensor
- Carbon Nano-tubes
  - Circuits
  - Interconnects
  - Architecture
- Non-Si Circuits & Arch.
- Process Variations
- Testing
- Low Power VLSI Signal Processing
- Subthreshold Leakage
  - Transistor Stacking
    - Multiple Vt
    - Dynamic Vt
- Leakage Control
- Gate Leakage, Diode Jn. Tunneling, GIDL
- Low Leakage Memory
  -- Dynamic Vt
  -- DRG Cache
- Digital Sub-threshold Logic
  - Ultra Low Power
  - Self Adjusting Vt
- Noise Immune Circuits
  - DCSL, SFL
- microArchitecture
  - Reconfigurable Cache
    - Gated Vdd, Clocking
    -- Dynamic Vdd
- SOI
  - DG-SOI
  - 3D-SOI
- Predictable Arch.
  - Array Based
- Professor Kaushik Roy
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Performance/Power Aware Computing & Comm

- NSF
- DARPA
- Northrup-Grumman
- MARCO GSRC
- SRC
- Intel
- ATT/Lucent
- HP
- IBM
- Convergys

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Nanotechnology: Modeling & Circuit Architecture

- Circuit Simulations of Carbon Nanotube FETs
  - Ballistic FETs: Circuit Performance
  - Schottky Barrier FETs: CMOS-like Applications

- Nanometer Scaled Ckts & Interconnects
  - Performance Estimation
  - Power Est. & Low-Power Des.

- Nanotechnology
  - Nano Circuit and Architecture
  - Process Compensation/Fault Tolerance
  - Modeling and Simulations

- Ballistic Carbon Nanotube FETs
  - SPICE Compatible Modeling
  - Schottky barrier FETs

- Dynamically Reconfigurable Cache Design
  - Analysis
  - Optimization
CNTFETs 1998 - 2005

IBM: Martel et al., APL, 73, 2447, 1998

Javey, et al., Nano Letters, 4, 1319, 2004
Modeling of CNFETs for Circuit Simulations

- Development of a framework for simulation and performance/power estimation of non-silicon devices/circuits/systems is essential.
- This will guide not only the device optimization but also facilitate development of novel circuit techniques for CNFETs.
Circuit Simulation Strategies

1. A top-of-the-barrier circuit compatible model for MOS CNFETs (Purdue).

2. A mixed mode simulation environment consisting of an NEGF treatment of CNFETs (Purdue) and a circuit simulator, for both MOS CNFET and SB CNFET.
Carbon Nanotubes: Structure & Synthesis

Diameter (d): ~ 0.5-5 nm, Length: ~ 10 nm - 10 cm

Growth: Chemical Vapor Deposition

Li, et al, JPC, 2001
Three Types of CNFETs: (a) SBFET

Tunneling limited current. Gate electrostatics will control the tunneling barrier.

“Carbon nanotubes as Schottky barrier transistors”
Heinze et al., PRL, 89, 106801, 2002
Appenzeller et al., PRL, 89, 126801, 2002

Javey, et al., Nano Letters, 4, 1319, 2004
Three Types of CNFETs: (b) MOSFET

Electrons do not see any tunneling barrier in the “on” state. Gate electrostatics control the top-of-the-barrier.
Three Types of CNFETs: (c) BTBT FET

Electrons tunnel from valance band to conduction band. Gate electrostatics control the bands in the intrinsic region. Not limited by thermionic emission.

BTBT FET

Appenzeller, PRL, vol 93, 19, 2005
Ineffective tunneling barriers.

Simulation studies,
Lundstrom, IEDM, 2005
Top of the barrier ballistic MOSFET model

\[ U_{SCF}(Q) = -qV_G \left( \frac{C_G}{C_\Sigma} \right) - qV_D \left( \frac{C_D}{C_\Sigma} \right) - qV_S \left( \frac{C_S}{C_\Sigma} \right) + \frac{qQ(U_{SCF})}{C_\Sigma} \]

\[ Q(U_{SCF}, \mu_1, \mu_2) = Q_S(U_{SCF}, \mu_1) + Q_D(U_{SCF}, \mu_2) \]

\[ Q(V_G, V_S, V_D) \]

\[ I_D(V_G, V_S, V_D) \]
Ballistic CNFETs with 1D Electrostatics

\[ n_{CNT} = \int_{E_C}^{+\infty} \frac{D(E)}{2} \left[ f(E - \mu_S) + f(E - \mu_D) \right] dE \]

- Self-consistent

\[ \psi_S = V_G - \frac{Q_{CNT}}{C_{INS}} \]

- \( I_{DS} \) is determined by \( \psi_S \)
A top of the barrier model: The SPICE Equivalent

Assumes 1D electrostatics and ballistic transport

Obtain $\psi_S$ as analytical functions of $V_{ds}$ and $V_{gs}$.

Compute 1D current from $\psi_S$.

Obtain the drain and source charges from $V_{ds}$ and $V_{gs}$.

Differentiate charge w.r.t. $V_g$ to obtain gate capacitors.
Designing with CNFETs

- Use of high K dielectric gives better gate control.
- High mobility gives higher $I_{on}$
- The intrinsic device shows several Tera Hertz of ring oscillator frequency.
Electrical Conductance

Quantum conductance limit for an ideal SWNT:

\[ G_Q = \frac{2e^2}{h}, \quad M = \frac{4e^2}{h} \]

\[ R_Q = \frac{1}{G_Q} = \frac{h}{4e^2} \approx 6.5\text{kohm} \]

G: conductance  
R: resistance  
M: number of “channels” = 2

Sources of extra resistance (nonideal):

**CONTACTS:** tunneling and Schottky barriers  
**CHANNEL:** defects and phonons
Performance Prediction: CN MOSFETs in Circuits

- CNTs can be arranged in parallel to achieve a MOSFET with a high $\mu$ channel.
- Higher $I_{on}$ for same $I_{off}$
- Symmetric PMOS and NMOS makes transistor sizing simpler.

- Arranged parallel CNTs (1.4nm dia) in the channel of a 50nm long MOSFET.
- Oxide capacitance and overlap lengths were kept constant.
- The first order (top of the barrier) model shows CNFETs can be more than 4 times faster than MOSFETs in the 50nm technology generation.
CNTFET Simulations: Intrinsic Device Performance

- Simulations of digital logic blocks have been done and performance of CNFETs has been evaluated (tool currently being used by Prof. Harris (U. Florida))
- Parasitics will play an important role.
- Ultra high integration density providing more than 10X area reduction – power density can be high!
Ultra High Performance CNTFETs: Role of Parasitics

The parasitics play an all important role in determining the CNFET performance.

The NASA Institute for Nanoelectronics and Computing

Purdue University
Issues in CNFET-based Digital Design

- High power and power density
- High defect density
Ultra-Low Power Techniques

- Subthreshold operation
- Multi-valued operation
- Energy recovery
Digital Subthreshold Operation

- Lower currents and lower capacitance
- Transfer characteristics are sharper.
Si Subthreshold Operation Works!

- TSMC 0.35um
- 72 I/O pins, 84 PGA package
- Vdd=300mV
- Leakage current monitor
- Self-substrate bias
Multi-valued Logic for Lower Power

A Ternary Inverter and its Voltage Transfer Characteristics

- The nanotube diameter determines the bandgap and hence the threshold voltage of the device.
- Dual diameter (and hence threshold voltage) can be used to design a novel multi-valued logic family.
Multi-valued Logic

- Simulations show that the power consumption of the proposed logic family is lower than the binary logic family at iso-performance.
• High integration density and high current density would aggravate the problem of extreme on-chip power density in nano-scaled technologies
Energy Recovery for On-Chip Power Density Reduction

- On-chip power density reduces by orders of magnitude by efficient use of energy recovery techniques.
Energy Recovery: Fabricated Chip

Operates at 200Mhz

Energy Recovery Clocking:
Sinusoidal clock used
70% energy recovered from Clock
Types of Carbon Nanotube FETs

- Top Gate
- ZrO₂
- Bottom Gate

Band Diagram:

- \( \Phi_b = E_g / 2 \)

Diagram:

- Intrinsic CNT
- Schottky barrier
- n⁺
- E_c/E_V [eV]
- x [nm]
CN SBFET: Ambipolar Conduction

midgap CNT SBFET

\[ V_D = 0.4V \]

\[ I_D [\mu A] \]

\[ V_G [V] \]

- \( V_G < V_D/2 \) hole conduction
- \( V_G > V_D/2 \) electron conduction
Device Characteristics

**CNT SBFET**

**CNT MOSFET**

Ambipolar Conduction

Unipolar Conduction
CMOS Inverter with Ambipolar FETs

By shifting $V_{FB}$ by $V_{DD}/2$, we get a useable FET (joint work with Professor Lundstrom)

NOTE: the p-FET and the n-FET are the same device!
MOS CNFETs have more current (and higher $g_m$).

The MOS CNFET has better Noise Margin and sharper VTC than the SB CNFET.
For transistor stacks in the "off" state, we can have $V_{GS} < 0$. Are these useable in CMOS logic?
Current vs. input vector

- '01' is the maximum leakage condition
- A stack is functionally operational when $V_{FB}$ is fixed at $V_{DD}/2$

CMOS type logic is possible using ambipolar CNT SBFETs with proper $V_{FB}$ design
CMOS logic with stacked transistors

For $I_{ON} / I_{OFF} \sim 1000$, $V_X \sim 10\text{mV}$.

Hence, $V_{FB} = V_{DD}/2$ is sufficient for a 2T stack.
Current in a stack: CNT MOSFET vs CNT SBFET

The CN MOSFET stack shows a higher $I_{on}-I_{off}$ ratio at iso – $I_{off}$ conditions.
A three valued memory cell for higher memory density
The transfer characteristic shows that the two curves meet at three points.

- Two of these are metastable points.
- Three of them are stable operating points located at (0,0), \((V_{dd}/2, V_{dd})\) and \((V_{dd}, V_{dd}/2)\)

A three valued memory element is possible.
CNT as Interconnects

- An all CNT design
- Parasitics will play an important role as the intrinsic gate capacitance is extremely small
- Ultra-small and high reliability
- Cu can handle a max. current density of \( \sim 10^6 \text{ A/cm}^2 \) whereas CNTs can handle more than \( 10^8 \text{ A/cm}^2 \)
- Mechanically strong and no electromigration effects
Developed an **RLC Model for CNT Interconnects**:  

- Incorporates quantum as well as electrostatic capacitances  
- Models the kinetic (or self) inductance
Modeling Resistance

Non Linear Resistance Model has been verified with experimental data*

*Ji-Yong, et. al., cond-mat/0309641, Sept. 28, 2003
Performance of a single CNT

Delay vs length of a single CNT interconnect. The ITRS prediction has been marked.
Comparison of delay of 20 parallel CNT interconnects with copper interconnect having the same equivalent width (w=80nm)
Limitations of CNT Interconnects

• CNT interconnects are severely limited by the contact resistances and kinetic inductance.

• High current densities do not result in high performance.

• Can only be used in relatively slower circuits where the device resistances are high.
Nanotube as a 1-D Nanoconductor

- The wave propagation is slowed down by the kinetic inductance.
- Below 100 GHz, the propagation is RC-limited anyway: the series R (~ 10 kOhm/um) overwhelms the inductance.
- The series resistance is much larger than that of conventional macroscopic interconnect.

⇒ “A single nanotube will be SLOW as an interconnect in general” (Ref: [Sayeef05])

Note: a single CNT could still be used as a local interconnect if the load is another nanoscale CNT-based structure ⇒ RC ~ 25 fs (Ref: [Burke04]). DC power distribution might be another option.
Bundles of CNT as High-Speed Interconnects

- If enough CNTs are used, the performance may be better than copper.
- “Nanotube bundles can be 80% faster than copper for the 45-nm node”

Ref: [Naeemi05]

Ref: [Sayeef05]
20nm vias with CNTs: Infinion Technologies

- Etch via stop on catalyst
- Particle formation
- Nanotube growth
- Single MWCNT in 20 nm via at lithographically defined location
High Defect Density: Failure Probability in SRAM Memory Cells in Scaled Silicon Tech.

- Intrinsic Fluctuation of $V_{th}$ due to random dopant effect
- $P_{Fault} = P_{AF} U P_{RF} U P_{WF}$
- In 45nm technology $\sigma_{V_{th}} \approx 30mV \rightarrow P_{Fault} > 1.0 \times 10^{-3}$
- Large number of faulty cells in nano-scale SRAM under process variation

MONTE CARLO simulation using BPTM 45nm tech.
Fault Statistics in 64K Cache

Conv. Yield ≈ 33.4%

σ_{Vt} ≈ 30mv, using BPTM 45nm technology

\[ N_{\text{Fault-Cells}} = P_{\text{Fault}} \times N_{\text{Cells}} \] (total number of cells in a cache)

- Conventional 64K cache results in only 33.4% yield

Need a process/fault-tolerant mechanisms to improve the yield in memory
BIST detects the faulty blocks

Config Storage stores the fault information

Idea is to resize the cache to avoid faulty blocks during regular operation
Resizing the Cache

- Conventionally multiple blocks are stored in a row
- Column MUX selects one block based on column address

Force the column MUX to select a non-faulty block in the same row if the accessed block is faulty

Config Storage is accessed in parallel with cache

Controller alters the column address

Feeds the fault information to controller
Resizing: Mapping Issue

More than one INDEX are mapped to same block

Include column address bits into TAG bits

Resizing is transparent to processor → same memory address
Effective Yield of 64K Cache

- Maximum yield achieved by ECC + Redundancy ~ 77%
- Proposed architecture + Redundancy results in ~ 94% yield
Fault Tolerant Capability

- Proposed architecture can handle more number of faulty cells than ECC, as high as 890 faulty cells with marginal perf loss.
CPU Performance Loss

- Increase in miss rate due to downsizing of cache
- Average CPU performance loss over all SPEC 2000 benchmarks for a cache with 890 faulty cells is ~ 2%
Summary

- Large number of faulty cells are expected in nano-scale SRAM under process variation
- The proposed scheme removes the faults by adaptively resizing the cache
- Transparent to processor (same memory address)
- Negligible area and energy overhead (excluding BIST)
- Does not affect the cache access time
- Minimal affect on processor performance ~ 2%
- High fault-tolerant capability compared to ECC and/or row/column redundancy
- Improves the yield to 94% from its original 33% for a 64K L1 cache
Conclusions & future work

• A simulation framework for evaluating CNFET based circuits and systems has been developed. More work is required to develop mixed mode device/circuit simulators for different types of devices
• Novel circuit ideas for low power are being investigated
• Research will be conducted in matching the models with experimental data
• Fault tolerant architecture and circuit design under process variation need to be considered
Major Technological Challenges

1. Control of chirality (yield ~90% with PECVD).
2. Direction of growth has to be controlled and gate material deposited on the CNT only.
3. Arrange CNTs in parallel in arrays to make effective transistors.
4. Nano-contacts with low parasitics need to be made.
5. Air stable chemical doping of CNTs necessary for making MOS CNFETs.
6. Make better metal-nanotube contacts free from tunneling barriers.