The Key Challenge

There needs to be pull from up here

And there need to be models and tools that connect them

There is much investment and bottom-up work here
Conclusions (from December meeting)

- Nanotech requires bridges between design and technology communities
  - **Circuits folks:** live or die based on their ability to tame unruly characteristics of physical devices into useful functions
  - **CAD folks:** live or die based on their ability to deliver tools that improve productivity given a hierarchy of models
  - **Architecture folks:** live or die based on their ability to deliver a complex function with highly constrained cost/reliability/power

- Many of the issues of concern to this committee are crosscuts, requiring joint work with research in the other areas:
  - Modeling, simulation, tools
  - Thermal management
  - Hybrid integration technology

- Models are important, but some work at this level can begin now

- *Applications* should drive architectural directions
Charge (from December meeting)

- Identify and characterize applications that will be enhanced by and made possible by emerging nanotechnology.

- Exploit revolutionary computational models and nonstandard architectures (memory, brain, parallel, VLIW, systolic, ...)
What are the research challenges for:

- nanoarchitectures
- bridging between circuits/systems and devices
- building reliable systems with noisy nanodevices
- identifying applications which will drive the use of nanotechnology
- producing tools and models which will enable circuits and systems with nanodevices (even though we may not know what those devices are now)
Three groups:

(1) Revolutionary architectures for reliable systems built with noisy nanodevices (Willamette Falls Ballroom)
Jeff Welser, Iris Bahar          Cliff Lau, Justin Harlow
Including but not limited to parallelism, fault tolerance, neuromorphic and polymorphic computing, adaptive computing, and mathematical foundations

(2) Application-driven architectures using nanodevices (Astoria Room)
Bob Colwell, Diana Marculescu    Dan Hammerstrom, Peter Varman
Including but not limited to CMOS-nano-hybrids, image and speech processors, graphic systems, memory-intensive systems

(3) Design tools, modeling, and simulation for nanoarchitectures (Coos Bay Room)
Chagaan Baatar, Massoud Pedram    Bill Joyner, Sankar Basu
Including but not limited to design methodologies and design tools for nanoarchitectures, hardware-software co-design, circuit and system models, multi-level simulations
Schedule:

1:00  Assemble in groups

3:30  Break in Willamette Falls Ballroom

4:00  Groups present conclusions

5:00  Adjourn
Charge:

Develop a presentation outlining the key challenges and areas of emphasis in your area which should be the subject of research, including enough text to explain what you mean.