Self assembled cellular neural networks for nanoelectronics

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Nanoscale CMOS based devices and architectures - Problems

- Small gate area leads to small capacitance
  - small transconductance
  - larger root mean square noise voltage.
  - Thin insulator…Gate leakage
  - High $\kappa$ dielectrics… degradation of channel mobility by POP scattering
Production Transistors Smaller Than Virus

Si transistor in the 90nm logic technology node: currently in production

Influenza virus
Source: CDC

Courtesy: Suman Datta, Intel Corp.
Experimental 10nm Si MOS Transistor

- 10nm transistor still behaves like a transistor!

Courtesy: Suman Datta, Intel Corp.
Silicon Transistor Scaling and Moore's Law will Continue through 2015 ......

New electronic materials, nano-technologies and nano-architecture introduced along the way

R.Chau, S. Datta, Intel, Nov20 2003
Prognosis

- Silicon CMOS – perhaps augmented by CNT devices, perhaps some molecular electronics – will probably continue till 2015, and possibly beyond
- ...But cost will likely balloon
Our aim

- Develop nano-architectures which will be
  - Inexpensive, perhaps taking advantage of self assembly techniques which are parallel fabrication routes with rapid throughput
  - Dense
  - Fault tolerant
  - Fast
  - Low power

First proposed in 1996:
A Self Assembled Nano-electronic Architecture
Essential ingredients

- A 2-D array of nanoparticles on a non-ohmic substrate whose I-V characteristic has a non-monotonic non-linearity, e.g. an NDR.
- Each nanoparticle is resistively and capacitively linked to its nearest neighbor nanoparticles.
What can this “bottom up” architecture do?

- This architecture generates
  - The STM model of neural networks (associative memory)
  - Can do image processing with an unprecedented density of $10^{10}$ pixels/cm$^2$
  - Can solve combinatorial optimization problems (exploiting single electron charging effects), e.g. the traveling salesman problem
  - Boolean logic circuits (NAND and NOR gates)
Associative memory

\[ G_{ij} \]

\[ C_{ij} \]

\[ C_{si} \]

\[ C_{sj} \]

\[ v_i \]

\[ v_j \]

\[ V_1 \]

\[ V_2 \]
What about logic?

- Uses 2-terminal devices (nanowires) instead of 3-terminal devices. These are *reciprocal* devices with no “isolation” between input and output of the logic device. Therefore, clearly unsuitable for logic circuits (combinational or sequential). Isolation is required for unidirectional propagation of logic signal from input to output.

- Preferred applications are “non-logic” computation and signal processing.
Issue of unidirectionality

- **Unidirectionality**, meaning isolation between input and output terminals of a logic device, is a “must” for logic circuits (see, for example, David A. Hodges and Horace G. Jackson, *Analysis and Design of Digital Integrated Circuits*, 2nd ed., Chap. 1, pg. 2). That is why 3-terminal devices are usually mandatory for logic applications since they are **non-reciprocal**.

- There exists diode-resistor logic (see Sedra and Smith, *Microelectronic Circuits*, 3rd ed. Oxford), …diodes are non-reciprocal devices… but DRL are less versatile and less fault tolerant

Can you make logic circuits with reciprocal 2-terminal devices?

- This is what is done in charge coupled devices (CCDs)
- In CCDs, you ensure unidirectional signal propagation by using a 3-phase clock ("push clock" and "drop clock"). ... But nobody uses CCDs for logic
- Boolean logic based on 2-terminal nanostructures are most likely to be nothing but glorified CCDs!
Self assembling the network…
Filling up the pores

Aluminum

Al$_2$O$_3$
Multi-layered nanowires

Cobalt
Nickel
Alq₃
Cobalt

200 nm
Vertical conduction characteristic (after removing the barrier layer) showing NDR

Peak-to-valley ratio at 300 K = 1.5:1

High resolution TEM
Computational Paradigms in Nanoelectronics: Quantum Coupled 
Single Electron Logic and Neuromorphic Networks

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We describe a new class of nanoelectronic circuits where circuit functions are derived from cooperative, quantum mechanical interactions between single electrons confined in arrays of quantum dots. Two specific architectures are examined: (i) quantum coupled logic in which Boolean logic functions are implemented by quantum mechanical spin-spin interactions between single electrons in arrays of quantum dots, and (ii) quantum neuromorphic networks that exploit the complex spatial and temporal evolution of discrete charge in an ensemble of non-linearly interacting quantum dots to elicit collective computational behavior. The first class of circuits includes combinational and sequential digital systems. Both logically irreversible elements such as half-adders, S-R flip-flops, shift registers, ring counters, etc., and reversible Feynman gates for quantum computation have been designed in this paradigm. These circuits can be endowed with the required “unidirectional” (non-reciprocal) character that previous (flawed) designs of similar circuits lacked. The second class of circuits comprises discrete Hopfield networks which utilize single electron tunneling events in arrays of metallic islands to perform neuromorphic computation. They can solve NP-complete optimization problems (such as the traveling salesman problem), produce associative memory effects and also exhibit rudimentary image-processing capability.

KEYWORDS: nanoelectronics, quantum dots, Boolean logic, neural networks, single electronics, spin polarization
S-type NDR

Peak to valley ratio = 19:1 at 300 K
Origin of S-type non-linearity

Al Ag
Accumulation layer
Alumina
Tunneling
qV
E_F
E_F1
E_F2
Ag
Al
Quantum Dot Network Circuit Model

Network Connectivity (Top view):

- $G_{ij}$
- $C_{ij}$
- $C_{si}$
- $C_{sj}$
- $J_{si}$
- $J_{sj}$

Dot pair circuit model

NDR piecewise model

- $I_P$
- $I_V$
- $v_P$
- $v_V$

Dots (or dot clusters)
C-V characteristics with silver paint contacts

Contact area is 1 mm$^2$

Wire density is $10^{11}$cm$^{-2}$, so that $10^9$ wires are contacted

Capacitance per wire is 0.5 aF

N. Kouklin and S. Bandyopadhyay
Technical Digest of ISCS, IEEE Press, pp. 303-308 (2000);
See also, N. Kouklin, L. Menon and S. Bandyopadhyay, APL, 80, 1649 (2002)
Current voltage characteristics of few dots

N. Kouklin, L. Menon and S. Bandyopadhyay
APL, 80, 1649 (2002).

Room temperature Coulomb blockade

T = 300 K
Measured resistivity of alumina = 160 kΩ-cm


In collaboration with Kurchatov Institute, Moscow, Russia
Quantum Dot Network Circuit Model

Network Connectivity (Top view):

\[ G_{ij} = 640 \, \text{M} \Omega \]

Dot pair circuit model

Network Connectivity (Top view):

- Dots
- (or dot clusters)

NDR piecewise model

\[ I_P, I_V, v_P, v_V \]

\[ G_D, G_{PR} \]
Circuit parameters based on measured values

- Single dot: $R_{\text{inter-dot}} = 640 \text{ M}\Omega$
- Single dot: $C_{\text{inter-dot}} = 5 \text{ aF}$
- Single dot: $C_{\text{substrate}} = 0.5 \text{ aF}$
- Single dot: Peak current = 1.5 nA

- Superdot (1 pixel = 6400 dots):
  - $R_{\text{inter-superdot}} = 8 \text{ M}\Omega$
  - $C_{\text{inter-superdot}} = 4 \text{ fF}$
  - $C_{\text{substrate}} = 3.2 \text{ fF}$
  - Superdot: Peak current = 0.1 $\mu$A

Since a pixel edge should be 10 times the wavelength of light, a typical pixel will contain about 6400 dots. A cluster of 6400 dots is called a “superdot”
A Quantum Dot Image Processor: Edge detection enhancement

Very fast response time of < 1 nsec

A Quantum Dot Image Processor: Horizontal/vertical line detection

Very fast response time of 1 nsec

Propagation of trigger waves

Auto waves (1-Layer CNN)

Trigger Wave Formation

Biologically inspired networks

\textsuperscript{3}FitzHugh Nagumo Neuroelectric Model: 2-Layer 2D array (with a coupled resistive layer)

Circuit level simulation at boundary of chaotic regime: System response with guided front waves
Modifying NDR characteristics with infrared illumination

Programming with light

Conclusion

- Locally interconnected.. Only nearest neighbor connection
- Massively fault tolerant (simulation shows that architecture can work even if 30% of the devices fail)
- Drivability is not an issue …architecture is primarily neuromorphic
- Reproducibility is not necessary. Architecture is based on collective computational models, where the cooperative interactions of many devices, acting in unison, matters. No single device is critical. We do not have to strive against stochasticity
- Switching speed is 0.1 psec
- Power dissipation is 0.01 nW/device
- Integration density achievable with self assembly techniques approaches 1 trillion devices per sq-cm
- THESE SPECIAL PURPOSE SELF ASSEMBLED ARCHITECTURES, WHICH ARE COMPATIBLE WITH SILICON CMOS TECHNOLOGY, CAN SERIOUSLY AUGMENT TRADITIONAL ARCHITECTURES AND IMMENSELY REDUCE COST WHILE INCREASING PERFORMANCE.
One other characteristic feature of publications on nanoarchitecture is the emphasis on defect tolerance and to a lesser extent tolerance to transient faults. The goal of fault and defect-tolerant implementations is to enable reliable circuits and computing using unreliable devices. Defects can occur as permanent defects from hardware manufacturing.

ERD WG meeting Munich April 08 2005

1996: Rolf Landauer…. Nanodevices must be more forgiving and fault tolerant than microdevices
For future considerations: “NEW” SPINTRONICS

- “Different” spintronics
  
  (1) Can we make spin devices that operate without moving electrons?
  (2) Non-equilibrium operation of binary switch?

- Orbitronics (in the future)

Interplay between charge, orbital, and spin degrees of freedom. Materials with both ferroelectricity and ferromagnetism (electrically controlled)

ERD Logic Group: Courtesy Jim Hutchby
Munich, 2005
Computing without moving electrons!

Toffoli-Fredkin gate

www.arxiv.org/cond-mat/0412519