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A Fast Congestion Estimator for Routing with Bounded Detours<br>Lerong Cheng, Guowu Yang, Xiaoyu Song and Zhiwei Tang<br>Dept. Electrical \& Computer Engineering, Portland State University, Oregon, USA.


#### Abstract

Congestion estimation is an important issue for the success of the VLSI layout. Fast congestion estimation provides an efficient means to adjust the placement and wire planning. A probabilistic model of interconnections enables designers to quickly predict routing congestion. We propose a powerful and fast estimation approach which allows wires to have bounded-length detours to bypass congestions. The method is more realistic and precise than the previous work. The experimental results demonstrate the effectiveness of the method on routing benchmarks.


Index Terms: VLSI Routing, Probabilistic Methods, Estimation.

## 1. Introduction

As deep-submicron fabrication technology advances, billion-transistor chips will be feasible in future. Estimation of the routing area becomes a crucial issue for a hierarchical design process and a necessity for top-down design styles [2]. With varieties of intellectual property (IP) from multiple sources, the estimation of the wire area becomes a more difficult issue in the development of the giga-transistor chip [1, 2, 4]. Fast congestion estimation provides an efficient means to adjust the placement and wire planning $[1,2,4,5,7,8]$.

With sizes on the order of hundreds of cells and thousands of connections, a probabilistic model of interconnections will enable designers to quickly compute estimates of the routing congestion. There has been some work on probabilistic models. Lou et al. [7] presented a fast probabilistic estimation for congestion. They assumed each net uses the shortest route and each possible route has the same usage probability. Base on such assumption, they estimate the congestion for the routing area.

In practice, the placement and routing problems are hardly solved optimally due to their computational complexity. The previous probabilistic approaches are not sufficient accurate as the shortest routes are merely considered in their restricted models. A more precise prediction should incorporate congestion-related detouring in the model to reflect the actual practice. In this paper, we propose a novel model where wires are allowed to have bounded-length detours to
bypass congestions. We present a probabilistic method to estimate the congestion of interconnect wires. The method is more realistic and precise than the previous work. The experimental results demonstrate the effectiveness of the method on routing benchmarks.

## 2. Problem Formulation

Given a set of nets, the routing area can be decomposed into grids. An edge is a border between two grids. The capacity of an edge is the number of available tracks crossing the edge and the density of an edge is the number of routes crossing the edge. Given a set of nets, we estimate the density of each edge of the routing area. We restrict our discussion on two-terminal nets. The model can be extended to handle the case for multi-terminal nets by using rectilinear Steiner tree or minimum spanning tree.

Without loss of generality, we assume that the terminals are located at the lower left and upper right grids. The lower left terminal is the start terminal and the upper right terminal is the end terminal of the net. The direction of the route is from the start terminal to the end terminal. A forward segment is a route segment which goes continuously up or right. A reverse segment is a route segment which goes continuously down or left.

Since we do not restrict the net route with the shortest length, the routes may not be monotonic. We use the coordinate on the grid. The coordinate of the grid containing the start terminal is assigned as $(0,0)$ and the coordinate of the grid containing the end terminal is assigned as $(m, n), m \geq 0$ and $n \geq 0$, as shown in Fig 1. If a route contains reverse segments, it will increase the total wire length, thus increasing delay. To limit the wire length, we make the following assumptions for each route.


Fig 1. A non-monotonic path from $(0,0)$ to $(m, n)$.

## Assumptions:

(i) The route contains only one reverse segment.
(ii) The reverse segment is a straight line.
(iii) The length of the reverse segment is bounded by no more than $d+1$ grids, $d \geq 0$ is an integer.


Fig 2. The expanded routing area for non-monotonic route.

By allowing the route to go down or left, the legal usage area is actually extended. As shown in Fig 2, $(m, n)$ is the end terminal coordinate and $d+1$ is the bound of the reverse segment. This models the actual layout where the shortest route is not always achievable.

Consider the dual graph of the grid model [7] as the routing mesh model in Fig 3. Each grid is represented by a node and the line segment connecting two adjacent nodes represents the line between two adjacent grids. The coordinate of each grid in the grid model is that of the corresponding point in the routing model. In the routing mesh model, a unit line is the line connecting two adjacent nodes. The length of the route is the number of unit lines covered by the route. Node $(0,0)$ is the start point of the route and node $(m, n)$ is the end point of the route. Both the start and end points are extreme points of the route.


Fig 3. The grid model and its dual mesh model.
Since the reverse segment of the route can go through no more than $d+1$ grids, the length of the reverse segment is no more than $d$ in the routing mesh model. The capacity and density of each edge in the grid model becomes the capacity and density of the corresponding unit line in the routing mesh model, respectively.

## Problem Statement:

Given a set of nets in the routing mesh model, estimate the density of all the edges for all routes satisfying the following constraints:
i) The route contains only one reverse segment.
ii) The reverse segment is a straight line.
iii) The length of the reverse segment is bounded by no more than $d+1$ grids, $d \geq 0$ is an integer.

## 3. Experimental Results

Our estimator is implemented in C and the experiments are run on a machine Pentium III 1G Hz with 256 M memory. The benchmarks are obtained from Prof. M. Sarrafzadeh's group at UCLA [3]. We compare our estimated results to those produced by the global router developed by the research group of Prof. M. Sarrafzadeh at UCLA [3].

In Table 1, we summarized the results for five benchmarks. For each benchmark, we tested it on our estimator, the estimator without detour and the global router. The density is divided into four ranges according to the unit line capacity. We count the number of unit lines whose density are in each range. For instance, in benchmark 2, the capacity for each vertical unit line is 20, we divide the density of vertical unit line into four ranges: $0-5,6-10,11-15$, and 15-20. The global router outputs 736 unit lines whose density is between 6 and 10 , the estimation without detour predicts 561 such unit lines while our method predicts that there are 704 such unit lines. Our prediction is very close to the outcome of a real global router while the time used by the estimator is dramatically smaller.

Table 1

| Benchmarks |  | Vertical Unit lines |  |  |  | Horizontal Unit lines |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Benchmark 1 <br> \# of nets: 9874 <br> routing area: $80 \times 64$ <br> vertical capacity: 22 <br> horizontal capacity: 32 | Density range | 0-5 | 6-10 | 11-15 | 16-22 | 0-7 | 8-14 | 15-21 | 22-34 | Run time (s) |
|  | Global router | 4870 | 237 | 13 | 0 | 4777 | 274 | 57 | 12 | 64 |
|  | Analysis without detour | 4974 | 142 | 4 | 0 | 4480 | 452 | 111 | 77 | 1 |
|  | Analysis with detour | 4787 | 312 | 21 | 0 | 4798 | 264 | 49 | 9 | 2 |
| Benchmark 2 <br> \# of nets: 15583 <br> routing area: $96 \times 64$ <br> vertical capacity: 20 <br> horizontal capacity: 33 | Density range | 0-5 | 6-10 | 11-15 | 16-20 | 0-5 | 6-10 | 11-15 | 16-23 | Run time (s) |
|  | Global router | 5273 | 736 | 125 | 10 | 4732 | 1217 | 168 | 27 | 144 |
|  | Analysis without detour | 5517 | 561 | 62 | 4 | 5036 | 978 | 121 | 9 | 1 |
|  | Analysis with detour | 5288 | 704 | 144 | 8 | 4841 | 1143 | 149 | 11 | 2 |
| Benchmark 3 <br> \# of nets: 19386 <br> routing area: $128 \times 64$ <br> vertical capacity: 20 <br> horizontal capacity: 23 | Density range | 0-5 | 6-10 | 11-15 | 16-20 | 0-8 | 9-16 | 17-24 | 25-33 | Run time (s) |
|  | Global router | 7931 | 257 | 4 | 0 | 7508 | 663 | 21 | 0 | 238 |
|  | Analysis without detour | 8061 | 131 | 0 | 0 | 7661 | 524 | 7 | 0 | 1 |
|  | Analysis with detour | 7901 | 291 | 0 | 0 | 7716 | 476 | 0 | 0 | 2 |
| Benchmark 4 <br> \# of nets: 26735 <br> routing area: $192 \times 64$ <br> vertical capacity: 21 <br> horizontal capacity: 32 | Density range | 0-5 | 6-10 | 11-15 | 16-21 | 0-7 | 8-14 | 15-21 | 22-32 | Run time (s) |
|  | Global router | 11724 | 558 | 6 | 0 | 11886 | 402 | 0 | 0 | 466 |
|  | Analysis without detour | 12041 | 247 | 0 | 0 | 12061 | 227 | 0 | 0 | 1 |
|  | Analysis with detour | 11881 | 407 | 0 | 0 | 12014 | 184 | 0 | 0 | 2 |
| Benchmark 5 <br> \# of nets: 28796 <br> routing area: $256 \times 64$ <br> vertical capacity: 14 <br> horizontal capacity: 28 | Density range | 0-3 | 4-6 | 7-9 | 10-14 | 0-6 | 7-12 | 13-18 | 19-28 | Run time (s) |
|  | Global router | 14052 | 2167 | 156 | 9 | 14769 | 1519 | 96 | 0 | 866 |
|  | Analysis without detour | 15215 | 1105 | 61 | 3 | 15164 | 1166 | 54 | 0 | 2 |
|  | Analysis with detour | 13988 | 2281 | 112 | 3 | 15167 | 1189 | 28 | 0 | 4 |

Fig. 12 and Fig. 13 illustrate the density map for Benchmarks 1 and 2, respectively. The brighter color represents a higher density. The density predicted by our method is very close to that predicted by the global router.

(a) Vertical density predicted by our method. (b) Vertical density predicted by global router. (c) Horizontal density predicted by our method. (d) Horizontal density predicted by global router.

Fig 12. Congestion maps for Benchmark 1.


Fig 13. Congestion maps for Benchmark 2.

## 4. Current Work

Our current work is to extend our approach by incorporating other design constraints:

1) Bounded number of bends
2) Relaxed detour constraints.

## 5. References

[1] C.-C. Chang, J. Cong, D. Pan, and X. Yuan, "Multilevel global placement with congestion control," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 22, no. 4, pp. 395-409, July 2002.
[2] J. Cong and Z. Pan, "Interconnect performance estimation models for synthesis and design planning," ACM/IEEE Int'l Workshop on Logic Synthesis, pp. 427-433, June, 1998.
[3] UCLA, http://www.ece.ucsb.edu/~kastner/labyrinth/.
[4] X. Yang, R. Kastner and Majid Sarrafzadeh, "Congestion estimation during top-down placement," IEEE Transactions on Computer-Aided Design (TCAD), vol 21, no. 1, pp. 7280, January 2002.
[5] M. Wang and M. Sarrafzadeh, "On the behavior of congestion minimization during placement," Proc. Int. Symp. Physical Design, pp. 145-150, Apr. 1999.
[6] H. Chen, H. Zhou, F. Y. Young, D. F. Wong, H. Yang, N. A. Sherwani, "Integrated floorplanning and interconnect planning," ICCAD 1999: 354-357.
[7] J. Lou, S. Thakur, S. Krishnamoorthy, and H. S. Sheng, "Estimating routing congestion using probabilistic analysis," IEEE Trans. Computer-Aided Design, 21(1), pp. 32-41, 2002.
[8] S. D. Brown, J. Rose, and Z. G. Vrabesic, "A stochastic model to predict the routability of field programmable gate arrays," IEEE Trans. Computer-Aided Design, 12(12), pp. 18271838, 1993.
[9] A. A. El Gamal, "Two-dimensional stochastic model for interconnections in master slice integrated circuits," IEEE Trans. Circuit \& Systems, 28(2), pp. 127-138, 1981.
[10] A. A. El Gamal and Z.A. Syed, "A stochastic model for interconnections in custom integrated circuits," IEEE Trans. Circuit \& Systems, 28(9), pp. 888-894, 1981.
[11] F. J. Kurdahi and A.C. Parker, "Techniques for area estimation of VLSI layouts," IEEE Trans. Computer-Aided Design, 8(1), pp. 81-92, 1986.
[12] N. Sherwani. Algorithms for VLSI Physical Design Automation. Kluwer Academic Publishers, 1995.
[13] M. Hall. Combinatorial Theory, $2^{\text {nd }}$ ed. New York: John Wiley \& Sons, 1986.
[14] M. Percy and A. Macmahon. Combinatory Analysis. New York: Chelsea, 1960.

