Project 1

Objective: To design a 64-bit parallel descrambler for the physical coding sublayer (PCS) receiver block.

Description: The serial form of the descrambler (i.e., LFSR) is shown in the diagram.

As shown in the figure, the descrambler implements the polynomial: \( G(x)=1+x^{39}+x^{58} \). The serial descrambler has one-bit input, 58-bit shift register, 2 XOR gates and one-bit output. This means the descrambler will output one-bit in one clock cycle. Thus, we need 64 clock cycles for 64-bits.

Task:
1) Design a parallel descrambler which has 64-bit inputs and gives the 64-bit output in one clock cycle. The block diagram is as follows:

2) Create test benches to verify your design.

To Turn in:
You need to turn in all of your VHDL files. All of your VHDL files should be in a directory called `sim1`. On any UNIX Operation System-based workstation, make a directory named `sim1`, put all of your VHLD files under `sim1`. From the directory right above `sim1`, copy the script `submit_sim1.pl` . Then execute the script via "perl submit_sim1.pl". This will create a com-
pressed tar file of your 'sim1' directory and will mail it to slip@ee.pdx.edu. In addition, a hard copy of report is required. In your report, clearly illustrate the steps about how to run the simulation of your design. Well verify your design with ModelSim on Sun Solaris workstation which is running with UNIX at ECE Dept. of PSU.