ECE 595
Emulation and Functional Specification Verification
Spring 2018
WCC, Mon, Wed,7-8:50pm

Introduction to theory and techniques to verify digital circuit designs with emphasis on non-simulation methods. Topics include hardware emulation, formal verification, and abstract system specification. Familiarity with computer architecture and System Verilog is required. A design verification project is an integral part of this course.

Students will gain experience using different techniques used to validate modern digital designs. The course will cover theory and methodology followed by hands on experience with emulation and formal methods. The course material complements other ECE pre-silicon and post-silicon functional validation courses.

Prerequisites: An upper-division undergraduate computer architecture (such as ECE 371) and System Verilog (ECE 571) or permission of instructor.

Course Coordinator/Instructor: Tom Schubert
FAB 20-10, 503.725.5395
tom.schubert@pdx.edu

Office Hours: Tues 11am-12pm, Fri 3pm-4pm**.** Or by appointment

TA: Nancy Mathan, Office Hours TBD

D2L website active: Lecture notes, papers, assignments and dropbox, announcements, etc

Required Texts and/or Required Reading List (all materials online)

- Specifying Systems, Leslie Lamport
- PSU ECE Veloce Documentation Website (access restricted to students in the class)
- Mentor Graphics Tools Documentation
- Multiple Papers

Course Objectives: Students will gain experience using several techniques used to validate modern digital designs. The course will cover theory and methodology followed by hands on experience with emulation and two different formal verification methods (protocol specification/verification and RTL design exercise). The course material complements the current ECE pre-silicon and post silicon functional validation courses.

Course Outcomes

1. Knowledge of role of validation in modern digital design projects
2. Knowledge of formal verification theory and application to digital design
3. Knowledge of emulation techniques as a complement to simulation
4. Ability to test digital designs using emulation technology
5. Ability to use formal verification tools to model and validate evolving architecture ideas prior to RTL development
6. Ability to use formal verification tools during early RTL development.
7. Understanding of the central nature of validation and the need for a structured, measured validation approach.

Outline of Course Content

Week	Topics
1	Design validation principles, strategies, product lifecycle, risk management Introduction to emulation, Simulation extensions for emulation
2	Emulation hardware and software, concurrency, SVA assertions
3	Emulation checking using SVA assertions, SCEMI and TBX emulation mode
4	XRTL language extensions for emulation, emulation debugging
5	Emulation testbench examples, review
6	Midterm, System specification, TLA+ language
7	TLA+ language, writing specifications, checking correctness using TLC
8	System specification checking of safety and liveness properties
9	Formal verification theory, representation of information, BDDs, BMC, SAT
10	Formal verification continued, project presentations, course review

Course requirements

- Midterm (20%), Final (25%), Project (30%), homework (25%)

There will be approximately 5 homework assignments. To pass the course, each assignment must be turned in on or before its due date. Some assignments may be done in groups. If you choose to work in a group, please turn in only one solution, indicating the names of all group members. Of course, individually, you will be expected to understand the material and demonstrate so on exams.

Some of the solutions might be obtained from previous classes. Using such solutions is **very** counterproductive! To pass exams, you'll need to develop analysis skills by working through problems. More importantly, working through the problems yourself or discussing in groups or with me is the best way to learn the material. I strongly encourage you to come to my office hours after working on a problem and we'll work out the correct answer together.

Project: The project is an important educational complement to the material presented in lectures. A good project will encounter problems that will require some research to find a solution. We'll discuss the project in more detail in a few weeks, but you should soon start thinking about possible projects. While I am receptive to projects either exploring formal methods or emulation, previous classes have opted for emulation based projects. To complete the project, the first step is to identify a design to verify. The design needs to be sufficiently complicated to require significant testing such that you can insert a subtle error in the design that might be difficult to catch. You are welcome to create a new design from scratch, though I recommend students start with a pre-existing Verilog design, possibly one you've created from another class (e.g. ECE585). I also encourage students to work in groups of 2-3 people. Students are expected to orally present their projects as well as turn in a written report.

Professionalism: In our worldwide discipline, we must work with many men and women from different cultures, races, sexual preferences, religions, political affiliations, etc. To pass this course, each student must demonstrate they are a good team player. Students are expected to work/learn in a harassment free environment with the highest professional standards.

As an instructor, one of my responsibilities is to help create a safe learning environment for my students and for the campus as a whole. We expect a culture of professionalism and mutual respect in our department and class. You may report any incident of discrimination or discriminatory harassment, including sexual harassment, to either the Office of Equity and Compliance or the Office of the Dean of

Student Life. Please be aware that as a faculty member, I have the responsibility to report any instances of sexual harassment, sexual violence and/or other forms of prohibited discrimination. If you would rather share information about sexual harassment or sexual violence to a confidential employee who does not have this reporting responsibility, you can find a list of those individuals (http://www.pdx.edu/sexual-assault/get-help). For more information about Title IX, please complete the required student module "Creating a Safe Campus" in your D2L.

Academic Honesty: I enjoy teaching very much and consider students to be future colleagues. Thus plagiarism is an extremely depressing thing for me to encounter and will be taken very seriously. Plagiarism is definitely not just a harmless prank. It can have very serious effects, harmful to your standing at the university, and possibly very harmful to your job prospects when you seek employment after graduation. The penalty for plagiarism is an F in the course and a letter describing the incident sent to the Vice Provost for Student Affairs. Please avoid any actions during an exam (e.g. talking, looking around, etc.) which might make the exam proctors doubt your honesty. Please also view PSU's Student Code of Conduct at **http://www.pdx.edu/dos/codeofconduct**

Doing Well: Lectures cannot cover all aspects of the material. Much of the detail will be learned through exercises or supplied by consulting the book and other online material. Ask me about anything that you don't understand, no matter how minor it seems. I recommend actively attending lectures. Many good discussions result from questions asked during class.

Finally, note that grading is non-competitive, so it is possible for everyone to do well.