# ECE 171: Digital Circuits – Winter 2018

This is a foundational course in design and analysis of digital circuits using number systems, Boolean algebra, and basic logic gates. Students will learn building digital circuits from Boolean functions using Karnaugh maps, timing diagrams, programmable logic devices. The simple digital circuits covered in class include multiplexers, demultiplexers, adders, and multipliers. The structure of the core of a microprocessor, Arithmetic Logic Unit (ALU) will be covered. The distinction between synchronous and asynchronous circuits will be discussed. Students will be introduced to a digital circuit design tool, Verilog.

### Prerequisite: MTH 112

Instructor: Tom Schubert FAB 20-10, 503.725.5395 tom.schubert (at) pdx.edu (email is the best way to contact me)

ECE 171 Office Hours: Tuesday 4pm, Friday 1pm, or by appointment.

# TA:Sri YamparalaOffice Hours: TBD (In FAB Circuit Lounge)

**Textbook**: *Digital Design: Principles & Practices*, John Wakerly, Prentice Hall, 4<sup>th</sup> Edition.

**D2L website active:** Lecture notes, homework assignments and dropbox, announcements, etc.

## **Course Concepts/Student Learning Outcomes**

- 1. Apply basic knowledge of number systems, Boolean algebra and logic circuits to reason about and analyze digital circuits.
- 2. Apply Karnaugh maps and Systematic Algebraic Reduction Technique to minimize Boolean functions.
- 3. Apply appropriate engineering techniques and methodology to design basic combinational logic circuits.
- 4. Apply basic timing and gate delay knowledge to reason about glitches and identify their causes.
- 5. Apply basic knowledge of programmable logic devices to analyze and design simple combinational logic circuits that use programmable devices.
- 6. Learn to analyze and design basic useful circuits including open-drain and tri-state gates, muxes and dmuxes, decoders, adders, multipliers and ALUs.
- 7. Apply appropriate engineering techniques to analyze basic synchronous and asynchronous circuits.
- 8. Introduce Verilog design tool and apply basic knowledge to specify simple combinational logic in Verilog.

| Week | Topics                                  | Reading (Wakerly)                                |
|------|---|--|
| 1    | Number Systems                          | 1.1, 1.2, 2.1, 2.2, 2.3                          |
|      | Binary Arithmetic                       | 2.4, 2.5, 2.6                                    |
| 2    | Floating Point and Binary Codes         | 2.10, 2.11, 2.12, 2.15.7, 2.16                   |
|      | Boolean Algebra                         | 4.1  |
| 3    | Boolean Equations and Karnaugh Maps     | 4.3  |
|      | Combinational Logic Circuits            | 3.1, 3.2, 3.3.2, 3.3.3, 3.3.4, 4.2, 6.1.2        |
| 4    | Integrated Circuits                     | 1.6, 1.7, 1.8, 1.9, 3.4, 4.3.1, 4.3.2            |
|      | Verilog                                 | 5.1, 5.4.1, 5.4.6, 5.4.8, 5.4.11, 5.4.12, 5.4.13 |
| 5    | Midterm (through Integrated Circuits)   |  |
|      | Verilog                                 | 5.4.7, 5.4.9                                     |
| 6    | Hazards, Decoders, and Multiplexers     | 4.4, 6.4.1, 6.7.1                                |
|      | Programmable Logic Devices              | 6.3.1, 6.3.2, 6.3.3, 6.3.4                       |
| 7    | Modular Design, Demultiplexers          | 3.7.3 - 3.7.7, 6.6.1, 6.7.3, 6.8.1, 6.8.2, 6.8.4 |
|      | Adders and Subtractors                  | 6.10.1   |
| 8    | Ripple Carry and Carry Lookahead Adders | 6.10.2, 6.10.4, 6.10.6                           |
|      | Multipliers                             |  |
|      | Arithmetic Logic Unit                   |  |
| 9    | Introduction to Sequential Logic        | 7.2.1 – 7.2.6, 7.2.10, 7.2.11, 7.3, 7.5          |
|      | State Machines                          |  |
| 10   | Review for the Final                    |  |

### **Outline of Course Content** (approximate)

Course Requirements: midterms/quizzes (30%), final (40%), homework (30%)

There will be approximately 7 homework assignments. To pass the course, each assignment must be turned in on or before its due date. Assignments may be done in groups. If you choose to work in a group, please turn in only one solution, indicating the names of all group members. Of course, individually, you will be expected to understand the material and demonstrate so on exams.

Solutions can sometimes be found through web surfing or from previous classes. **Doing so is very counterproductive!** To pass exams, you'll need to develop analysis and mathematical skills by working through problems. Even when working in a team, be sure you can work out solutions from scratch. I strongly encourage you to come to my office hours after struggling and we'll work out the correct answer together.

**Grading:** Grades are not curved. The course covers material that you need to know to be a successful engineer. Percentage grades can be converted to letter grades as follows:

| А  | >93%  | A-  | >90% |    |      |
|----|-------|-----|------|----|------|
| B+ | >87%  | В   | >83% | в- | >80% |
| C+ | >77%  | С   | >73% | С- | >70% |
| D+ | >67%  | D   | >63% | D- | >60% |
| FΕ | Below | 60% |      |    |      |

**Attendance:** As a student in this class, you are expected to attend each class meeting. Attendance is essential for success. Unfortunately, absences are sometimes unavoidable. If you are absent, it is your responsibility to find out what work was covered.

**Professionalism:** In our worldwide discipline, we work with many people with different genders, cultures, races, sexual preferences, religions, political affiliations, etc. We expect a culture of professionalism and mutual respect in our department. To pass this course, each student must demonstrate they are a good team player. Students are expected to work/learn in a harassment free environment with the highest professional standards.

**Safe Campus:** As an instructor, one of my responsibilities is to help create a safe learning environment for my students and for the campus as a whole. Please be aware that as a faculty member, I have the responsibility to report any instances of sexual harassment, sexual violence and/or other forms of prohibited discrimination. If you would rather share information about sexual harassment, sexual violence or discrimination to a confidential employee who does not have this reporting responsibility, you can find a list of those individuals. For more information about Title IX please complete the required student module *Creating a Safe Campus* in D2L.

**Academic Honesty:** I enjoy teaching very much, and consider students to be professionals. Thus cheating is an extremely depressing thing for me to encounter and will be taken very seriously. Cheating is definitely not just a harmless prank. It can have very serious effects, harmful to your standing at the university, and also possibly very harmful to your job prospects when you seek employment after graduation. The penalty for cheating is an F, making it difficult to subsequently pass the course. A letter describing the incident is also sent to the Vice Provost for Student Affairs. Also, please avoid any actions during an exam (e.g. talking, looking around, etc.) which might make the exam proctors doubt your honesty.

**Doing Well**: Lectures cannot cover all aspects of the material. Much of the detail will be learned through exercises or supplied. Make sure that you set aside enough time to do the exercises and complete the reading carefully, thoroughly and thoughtfully. Several copies of the text are also on reserve at the library. Finally, note that grading is non-competitive, so it is possible for everyone to do well.