Maseeh College of Engineering and Computer Science

PORTLAND STATE UNIVERSITY

Friday, October 13th, 2017 - 9:30 a.m. to 1:30 p.m.

8005 SW Boeckman Road - Wilsonville, OR 97070

Deschutes Conference Room (D1320)

Sponsored by Mentor Graphics

Message from the Dean

The Fariborz Maseeh College of Engineering and Computer Science at Portland State University is a research-integrated engineering school that evolved in parallel with the growth of the high-tech industry in Oregon. More than 3,000 students are currently enrolled in programs that lead to Bachelors, Masters, and PhD degrees in civil engineering, computer engineering, computer science, electrical engineering, environmental engineering, mechanical and materials engineering, and engineering and technology management and systems engineering.

Maseeh College has close industrial ties, which offer students opportunities for internships and to study cutting-edge, problems. Many participate in research, industrial projects, prestigious competitions, and the college's student-driven Innovation Programs.

The Electrical and Computer Engineering Department is the second largest department in the Maseeh College. Its teaching and research laboratories are equipped with modern industry-grade equipment for measurement, test, and prototyping.

Maseeh College faculty members have outstanding strengths in a number of fields including Tera-Hz devices, Acoustics Electromagnetics, IC Design and Test, Power Engineering, Embedded Systems, and Communications.

A multi-year process is currently underway at Maseeh College to establish a nationally-recognized program in Design Verification. The program is founded on two important premises. The first is that design verification is increasingly becoming a central and demanding process in modern digital designs due to drastically increasing complexity and the need for speed. The second is that there is a huge and rising demand for verification engineers who are well versed in modern verification technologies.

A focused Design Verification curriculum has been developed, which is supported by faculty from Electrical and Computer Engineering and from Computer Science who are actively engaged in developing new design verification technologies.

Renjeng Su, D.Sc.
H. Chik M. Erzurumlu Dean

Maseeh College of Engineering
and Computer Science
PORTLAND STATE UNIVERSITY

Competition Agenda

TIME	TOPIC	PRESENTERS
9:30 a.m. – 9:50 a.m.	**Check-in & Refreshments**	***Students & Guests***
9:50 a.m.	**Welcome & Introduction**	***Renjeng Su & Kenneth Larsen***
Competition Finalists' Presentations		
10:00 a.m.	Emulator Based Verification of PDP8 ISA Hardware Simulation	***Aanchal Chobisa***
10:30 a.m.	Accelerated Verification of a 64 point FFT Core	***Nancy Mathen***
11:00 a.m.	Emulation Testbench for Accuracy Testing of a Stochastic Computer of Linear Dynamical Systems	***John Parker***
11:30 a.m.	Emulation Ready UVM Framework for an Ethernet IP Core	***Ashwin Harathi Durga Kundan Vanama Manavsi Prasad Randon Stasney***
12:00 p.m. – 12:15 p.m.	**Break for Judging**	***All (except judges)***
12:15 p.m. – 12:30 p.m.	**Announcement of Winners & Photos - Wrap-up**	***Tom Schubert & Mark Faust***
12:30 p.m. – 1:30 p.m.	**Lunch**	***All***

Need for Speed Emmulation Competition Background

The Need for Speed Veloce Emulation Competition was conceived of as a joint effort by Mentor Graphics and the Portland State Electrical and Computer Engineering Department to encourage more students to explore hardware emulation by tackling industry-level engineering challenges.

The competition's theme underscores growing demand for sophisticated testing hardware and design verification talent. Complex designs can take hours or even weeks to adequately test. Emulation tools, such as the Mentor Graphics Veloce, are capable of dramatically accelerating this process allowing for more thorough verification before production. This results in higher quality products and faster time to market.

A total of $9,000 in prize money was funded by an anonymous donor. Five thousand dollars in prize money will be awarded to the first-place team, $3,000 for second place, and $1,000 for third place.

Executives from industry leaders Intel and Imagination Technologies, along with representatives from Mentor Graphics form this year's judging panel.

PSU professors Tom Schubert and Mark Faust served as team mentors and helped to make the event possible.

Competition Judges from Industry

Tom Berg

Principal Engineer, MIPS Technologies

Tom Berg is a Principal Engineer at Imagination Technologies where he leads the hardware development of multi-core, L2 cache and IO-coherence technologies. Tom has 25+ years of pushing the state-of-the art in coherent multi-processing computer systems with companies such as Sequent Computers, IBM, PMC-Sierra, and MIPS Technologies. He received his BS in Electrical and Computer Engineering from The University of Michigan and his MS in Electrical Engineering from Purdue University. Tom has been named on 16 patents in many aspects of computer systems.

Andrew Iverson

Silicon Components Design Manager, Compound Photonics

Andrew is an experienced ASIC design and verification engineering manager with 18+ years of experience in all areas of an ASIC design cycle including project management, IP sourcing, system/chip-architecture, block-level micro-architecture, Verilog design, SystemVerilog verification, production testing, lab bring-up and validation, and embedded software.

Rick Leatherman

Director of Tools, Imagination Technologies

Prior to joining Imagination Technologies, Rick was VP of Tools for MIPS Technologies. He also founded First Silicon Solutions (FS2), a provider of system-level debug technologies, acquired by MIPS in 2005. He has 20+ years of experience in development tools at companies including Intel, Microtek and Microcosm. He championed the concept of On-Chip Instrumentation (OCI®) in 1999; a concept that has become widely adopted in the embedded tools industry. Rick has an EE degree from Virginia Tech and MBA from the Tuck Business School at Dartmouth College. He is listed as “co-inventor” on issued and pending patents.

Leon Lim

Engineering Manager, Intel Corporation

Lim is an Engineering Manager at Intel Corp. He manages engineering teams who are responsible for hardware emulation of multiple Xeon Servers, HPC and data center products. Lim has a MSEE from OHSU and BSEE from the University of Washington. He has 18 years of industry experience ranging from board design, FPGA & ASIC design to hardware emulation and FPGA prototyping.

Satish Munirathnam

Engineering Manager, Intel Corporation

Satish is an Engineering Manager at Intel Corp, responsible for emulation effort for the Xeon Phi (MIC) segment. Satish brings with him many years of industry validation and emulation experience. Satish holds MSEE from Oklahoma State University.

Competition Judges from Mentor Graphics and PSU

Dr. Lauro Rizzatti

Verification Consultant with Mentor Graphics

Dr. Rizzatti is an industry expert on hardware emulation (www.rizzatti.com). Previously, Dr. Rizzatti held positions in management, product marketing, technical marketing, and engineering. He can be reached at lauro@rizzatti.com.

Tom Schubert, Ph.D.

Design Verification and Validation Instructor – Electrical and Computer Engineering

Maseeh College of Engineering and Computer Science, Portland State University

Schubert directs a graduate track in Design Verification and Validation. Previously, he was at Intel Corporation for 17 years, where he was a senior pre-silicon validation manager for many generations of microprocessor/SOC designs. He also led Intel's largest formal verification team developing techniques that were applied across the company. Tom received a Ph.D. in Computer Science from the University of California, Davis.

Mark Faust

Assistant Professor – Computer Architecture

Maseeh College of Engineering and Computer Science, Portland State University

Faust is an assistant professor in the Electrical and Computer Engineering Department at Portland State University where he teaches a variety of courses in digital design and computer architecture, as well as SystemVerilog. Prior to coming to PSU in 2004, Mark was General Manager for Asian Operations for Credence Systems Corporation. Before joining Credence, he held a variety of engineering and engineering management positions at several startups. He earned BS and MS degrees from Carnegie Mellon University.

Roy Kravitz,

Instructor and Westside Program Director

Maseeh College of Engineering and Computer Science, Portland State University

Professor Kravitz is a full-time instructor and the Director of the ECE Westside program. He has created and co-taught courses in FPGA design, digital systems design, embedded systems, and computer architecture for more than 15 years.

Kravitz's professional career spans more than 35 years in multiple companies and roles. He started as a micro-processor designer at Intel and completed 5 years as VP of Engineering for BPL Global before switching to Academia. Roy earned his BS Computer Engineering and MS Electrical Engineering from the University of Illinois, Urbana. His interests include embedded system hardware and software, digital system design using programmable logic, Android programming, and computer architecture.

Project finalist 1

Aanchal Chobisa

I graduated with a Masters in Electrical and Computer Engineering from Portland State University in IC Design, Test and Validation track in June 2017. I have completed courses including Digital IC Design, System Verilog, Emulation Specification, SOC and Computer Architecture among others.

I was introduced to the emulation platform as a part of the final project for the course 'Introduction to System Verilog' offered by Prof. Mark Faust and further enhanced my knowledge for emulator during course 'Emulation and System Specific Verification' taught by Prof. Tom Schubert which helped me enter the finals for the Need For Speed competition by Mentor Graphics.

I have experience with scripting languages python and tcl, programming languages like C.

I am currently looking for an opportunity in the field of Design or Verification in semiconductor industry and can be reached at 'aanchal.chobisa@gmail.com' or 'aanchal@pdx.edu'.

Emulator Based Verification of PDP8 ISA Hardware Simulator

(Aanchal Chobisa)

ABSTRACT:

The task was to design, verify, simulate and test the PDP8 ISA Simulator. The goal is debugging and functional verification of the system being designed. One of the biggest advantages that the emulator presents apart from used as a hardware system is the speedup it provides in the working environment for the Design Under Test (DUT). The design was emulated using the Standalone and Transactor based modeling for the Veloce based solo Emulator Hardware and calculate the speedup achieved in the verification process.

DESIGN:

The PDP8 ISA Simulator consists of three units, The Instruction fetch and Decode (IFD) Unit, the Execution (EXEC) Unit and the Memory (MEM) Unit. All the three unit work in coherence to provide the result of the instruction fetched by the IFD from the MEM. The design has 13 basic functions input to the design as a text file written to incorporate the memory unit.

VERIFICATION:

The verification strategy was based on the bottom up and the re-use strategy. The design was first simulated on Questasim verifying the unit level and the chip level. The verification environment included the scoreboard and a monitor. The design was emulated using STANDALONE and Veloce TBX mode. The design and the testbench were written in synthesizable System Verilog. The top level testbench uses these pseudo-randomly generated test vectors along with pre-computed expected values in order to efficiently test the DUT(s) using System Verilog assertions. The System Verilog based HVL testbench communicating with the XRTL HDL Transactor running on the Veloce emulator, communicating through SCEMI pipes is used.

RESULT:

The run-times on the emulator and simulator were compared to calculate the speed-up achieved by the emulator over the simulator. A speed-up of 45x was achieved using emulation over pure simulation and a functional coverage of 96%. This reduces a multi-hour simulation run to few minutes on the emulator.

Project finalist 2

Nancy Mathen

Nancy Mathen is a graduate student at Portland State University focusing on the digital design, test and validation track. She also has a special interest in verification and validation. She will graduate in Spring 2018. She is currently a teaching assistant for Dr. Schubert's Digital Circuits class.

She has previously completed courses in Microprocessor System Design, Introduction to SystemVerilog, ASIC Design and Synthesis, Computer Architecture and Pre- Silicon functional verification. Through various projects, she has gained experience in SystemVerilog and Mentor Graphics verification tools such as Questa and Veloce emulator. She has previously worked on Veloce emulator for accelerating the verification of an 8 bit CPU core. She has also completed multiple design projects including design of an L2 cache simulator, ISA simulator for PDP 11/20, and an asynchronous FIFO design.

Accelerated Verification of a 64 point FFT Core

(Nancy Mathen)

ABSTRACT:
The aim of this project is to the study the advantages of emulation based verification over simulation for heavily computational designs. For this, I have chosen an existing 64 point FFT core in Verilog. The design is verified on Mentor Graphics Veloce in standalone and TBX modes.

DESIGN:
The FFT core computes the fourier transform for a 64 point complex data set. It uses a Winograd FFT computation algorithm. The inputs to the FFT are 16 bit wide and the outputs (real, imaginary) are 18 bit bit wide. The outputs are produced serially. The 64 point FFT is implemented using 4 8-point FFTs making the design pipelined. The design completes one set of computation in 136 cycles out of which 64 cycles are required to produce the 64 point FFT. However, as soon as the first output set is available, the next set of 64 point data can be applied. The design can be configured for Forward and Inverse FFTs.

VERIFICATION:
A black box approach towards verification is adopted. The huge state space of the design provides a large number of testcases. In standalone mode, the output of the FFT core for a 64 point complex dataset is compared against a reference data set. In standalone mode the data set is configured as a ROM which feeds the input data to the DUT. The reference set is based on the output of another FFT model for the same input which is configured in a second ROM. In the TBX mode, a C model of FFT is used as a reference model for generating the FFT. The input stream of 64 point data is also generated on the HVL side through a C function. The inputs are floating point data which are normalised to preserve accuracy while truncating to a 16 bit value. DPI function calls are used to communicate between HVL and HDL sides.

Project finalist 3

John Parker

John Parker is a graduate student in the Electrical and Computer Engineering department at a Portland State University. He is writing a Master's Thesis on the subject of Stochastic Computing under Marek Perkowski and studies in the Computer Architecture track, but has also made concerted effort in the study of Formal Verification, Machine Learning, Complex Systems, and Quantum and Memristor Computing. His primary interest is High-Performance Computing for research in the Natural Sciences, and he teaches Computational Thinking for grade-school students in an after-school program. He holds a Bachelor of Arts degree with emphasis in Mathematical Physics and Microbiology from The Evergreen State College in Olympia, Washington.

He developed a software system employing Naive-Bayes text classification as part of a voice command and chatbot platform in Marek Perkowski's Intelligent Robotics courses, and began work on a stochastic computer of linear dynamical systems in Marek Perkowski's Digital System Design using Hardware Description Language course. He has investigated techniques for determining properties of state transition graphs of Cellular Automata so as to relate those properties to Wolfram's CA classes as in Langton's Paper entitled "Computation at the Edge of Chaos: Phase Transitions and Emergent Computation", and this work was done in Tom Schubert's Emerging Functional Verification Methods course and Joe Fusion's Artificial Life course in the Systems Science department. He has also developed a foundation of study for Quantum Computing and Memristor Computing in Marek Perkowski's seminars, and is considering employing Stochastic Computing to build a Quantum Computing Simulator.

Emulation Testbench for Accuracy Testing of a Stochastic Computer of Linear Dynamical Systems

(John Parker)

ABSTRACT:

The goal is to perform accuracy testing on design variants of a stochastic computer of linear dynamical systems. The computer is implemented as a logical unit for approximate numerical computation of dynamical system trajectories implemented in the stochastic computing hardware paradigm, and the design is parameterized in terms of the number of dynamic variables and the precision of stochastic signals employed in the computation. In addition, the system is also parametrized in terms of a proposed design variant to speed up computation by increasing the number of stochastic signals representing each variable.

Testing requires evaluating approximation accuracy statistically by performing many trial runs of the system to obtain sample output for each system of equations to be solved and for each setting of design parameters. Hardware Emulation is necessary to test the design because emulation promises a near-constant time of calculation for a dynamical system as design parameters are increased, where simulation time becomes prohibitive beyond even modest parameter settings on dynamical systems of 2-4 variables.

SUMMARY:

The primary motivation for undertaking this project is to test an experimental design for a parallel computer of linear dynamical systems (differential equations that change with respect to time). The plans for the project include several design variants, and several parameters that effect the precision of the design's computation. Since the computing paradigm of the design is stochastic in nature, plans also include testing using various sources and amounts of pseudo-random numbers, and rigorous testing requires establishing a framework for statistically evaluating the validity of the design. The project is large in scope, and includes goals scientific, engineering, and validation in nature.

So, for the purposes of this competition, the focus must remain primarily on the goals of validation, the challenges that were overcome in establishing the current state of the test bench, and how knowledge gained may be applied in further work on the test bench. The most essential goals have been accomplished, and include compiling the design on the emulator, parameterizing design description to scale to any number of variables and any range of design parameters, establishing a co-modeling test bench that is suitable for designs with a small number of variables, and establishing a method for including HVL-generated pseudorandom numbers in the sources of pseudorandom numbers used to validate the design. After achieving these goals, future work now includes expanding the test bench to accommodate a design

modeling a large number of variables, searching for other methods to increase efficiency of moving HVL-generated pseudorandom numbers to the HDL, properly adding pipelined stages to achieve better performance from both an emulation and engineering perspective, and moving methods of generating test cases and evaluating design output from OS-level scripts into the HVL.

Specifically, the experiments that are included in the materials of this report are threefold. The first two are are test benches implementing variants of the stochastic computer of linear dynamical equations. The third is preliminary work for constructing a test bench to provide pseudorandom numbers to the HDL from the HVL.

- Dynamic system as set of differential equations

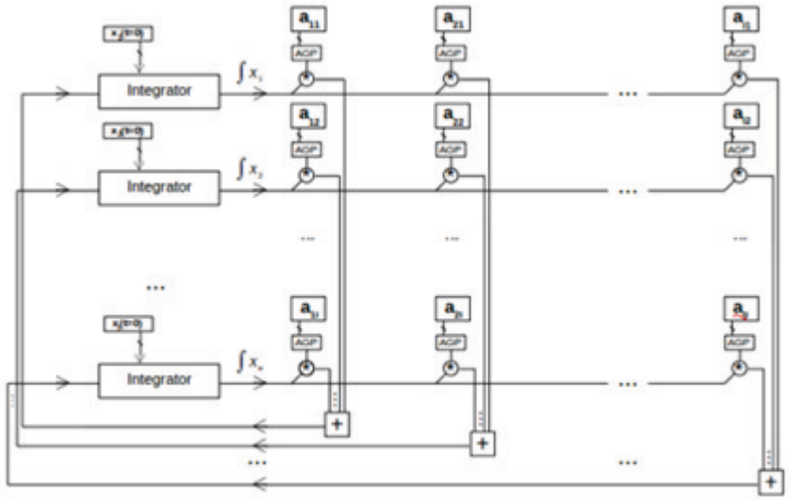
$$\frac{dx_1}{dt} = a_{11}x_1 + a_{12}x_2 + \ldots + a_{1i}x_i$$
$$\frac{dx_2}{dt} = a_{21}x_1 + a_{22}x_2 + \ldots + a_{2i}x_i$$
$$\ldots \quad \ldots \quad \ldots$$
$$\frac{dx_i}{dt} = a_{i1}x_1 + a_{i2}x_2 + \ldots + a_{ii}x_i$$

- Matrix form

$$\begin{bmatrix} a_{11} & a_{12} & \ldots & a_{1i} \\ a_{21} & a_{22} & \ldots & a_{2i} \\ \vdots & & \ddots & \\ a_{i1} & a_{i2} & \ldots & a_{ii} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_i \end{bmatrix} = \begin{bmatrix} dx_1/dt \\ dx_2/dt \\ \vdots \\ dx_i/dt \end{bmatrix}$$

- Transformed into a set of integral equations

$$x_1 = a_{11}\int x_1 dt + a_{12}\int x_2 dt + \ldots + a_{1i}\int x_i dt$$
$$x_2 = a_{21}\int x_1 dt + a_{22}\int x_2 dt + \ldots + a_{2i}\int x_i dt$$
$$\ldots$$
$$x_i = a_{i1}\int x_1 dt + a_{i2}\int x_2 dt + \ldots + a_{ii}\int x_i dt$$



Team finalists 4

Ashwin Harathi is a graduate student at Portland state University pursuing his MS in ECE with specialization in Computer Architecture and Design. He has completed courses including Formal Property Verification using System Verilog Assertions, SoC using FPGA, Computer Architecture, and Post-Silicon Functional Validation. His interests include Computer Architecture, Operating Systems and loves scripting. He is actively looking for opportunities in the field of verification and can be reached at ashwin.harathi@gmail.com. Prior to his Masters, Ashwin worked as a Verification Engineer in Applied Micro Circuits Corporation on Block Level Verification of RDMA over Converged Ethernet(RoCE) based on InfiniBand, AMBA AXI and Security Subsystem which were part of APM's server chip X-GENE. Ashwin is a Student Leader of Indian Student Association and Hindu -Yuva Student groups at Portland State University.

Kundan Vanama is an Electrical and Computer Engineering graduate student at PSU. He will complete his Masters in Computer Architecture track by June 2018. He is interested in Verification and Embedded Systems as well. With more than a year of experience with Robert Bosch as an embedded engineer, he has worked on EEPROM and diagnostics domain in automotive systems. He is currently a Teaching Assistant for Prof. Roy Kravitz. Kundan is interested in applying concepts he's learned, which motivated him to publish a technical paper on "Low Power Stable Design of SRAM cell" during his undergraduate studies. His passion for technology led him to learn various languages such as PERL, python, Ruby, JAVA (Oracle Certified Java Programmer), and TCL. His projects include vehicle collision detection, PDP-11 ISA simulator, Formal verification of TLB of MIPS FPGA and Physical and Logical Flow Synthesis of Asynchronous FIFO where he had used SystemVerilog and taken support of Mentor tools. He is actively looking for opportunities in Computer Architecture and Verification fields and can be reached at kundan.vanama@gmail.com.

Manasvi Prasad is a second year grad student in the Electrical and Computer Engineering Master's Program at PSU. Her interests lay in the Design and Verification of Digital Systems. Manasvi's primary area of focus is in the Pre-Silicon Verification. Her work on the Design, Pre-Silicon Functional Verification and Emulation of AMBA 2.0 Bus Protocol using Synthesizable SystemVerilog has made her confident of the Bus Architecture, Hardware Modeling using SystemVerilog and configuring the Emulator. She has performed the complete Verification cycle in the Pre-Silicon Functional Verification on PDP-8 Processor Architecture. Her interest further extends to the Timing Analysis of the Digital Circuits. She is currently working as a Front End Verification Engineering Intern with Xilinx. She is looking for Full-Time Opportunities in the Pre-Silicon Verification Domain from April 2018 and can be reached at manasvi@pdx.edu or www.linkedin.com/in/manasvi09.

Randon Stasney is a recent graduate from Portland State University. In March of 2017 he completed his masters in the embedded systems track. While he was at PSU he had the opportunity to be a Teaching Assistant for Dr. Hall's Microprocessors class and for Dr. Schubert's Emerging Functional Verification Methods class. He was also able to work with his academic advisor, Prof. Kravitz, creating a timing project for SOC Design with FPGAs. Through several successful school projects, Randon has gained proficiency and confidence using System Verilog and Mentor Graphics tools. Some examples include: creating a pipelined HW design with forwarding and an original ISA for the IDEA algorithm; verifying a UART design with BIST and BFM interface; designing a satellite hub controller FSM. He also created a dungeon scroller game for NEXYS 4 FPGA using PicoBlaze soft core processors. Additionally, his projects have involved interfacing with Beagle Bone Black, Arduino, and Raspberry Pi through UART, I2C, and SPI.

Emulation Ready UVM Framework for an Ethernet IP Core

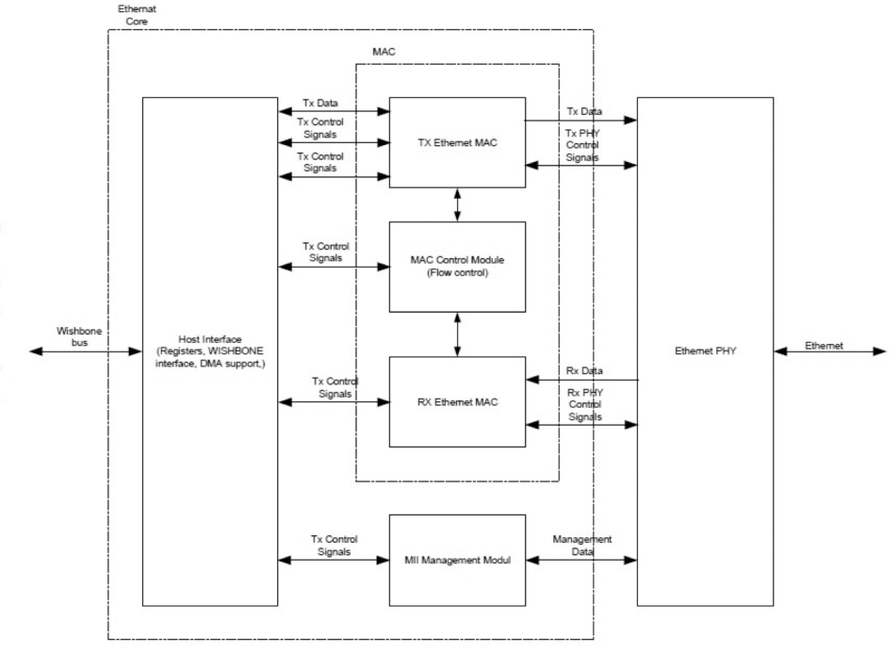
(Ashwin Harathi, Durga Kundan Vanama, Manavsi Prasad, and Randon Stasney)

ABSTRACT:
Our goal was to leverage UVM testbench into emulation and create unified a dual-top testbench. We were able to construct a fully reusable UVM framework for ethernet IP core.

ABSTRACT:
The ethernet IP core is a MAC (Media Access Controller). It connects to the Ethernet PHY chip on one side and to the WISHBONE SoC bus on the other. Ethernet IP Core features are

- Performing MAC layer functions of IEEE 802.3 and Ethernet.
- Automatic 32-bit CRC generation and checking
- Preamble generation and removal
- Automatically pad short frames on transmit
- Full duplex mode
- Complete status for TX RX packets
- IEEE 802.3 Media Independent Interface (MII)
- WISHBONE SoC Interconnect
- Internal RAM for holding 128 TX/RX buffer descriptors.
- Interrupt generation on all events

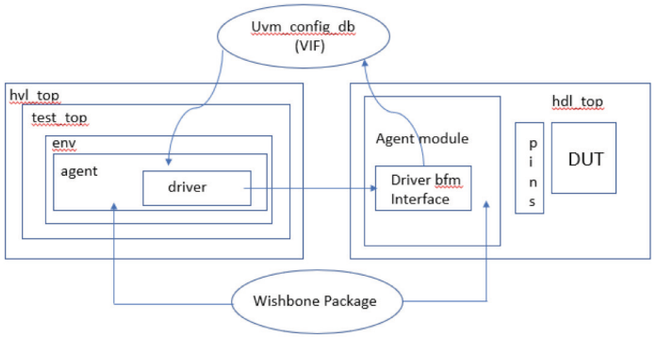
ARCHITECTURE OVERVIEW:



VERIFICATION:

- We designed our testbench in TBX mode to get best of both worlds
- We followed all the key concepts of co-emulation like dual domain testbench, transaction based communication and untimed testbench model
- We used UVM register model to configure registers in the DUT and wishbone bus adapter that translates register based transactions to wishbone based transactions.
- We implemented virtual interface (VIF) based HVL-HDL communication, used a hierarchical verification approach and UVM configuration database to pass VIFs
- Implemented BFMs using VIFs to drive DUT signals
- Implemented memory on emulator to have infrequent information rich transactions between domains and let emulator run at full speed

TESTBENCH OVERVIEW:



Emulator Used for this Competition

Veloce® 'Solo' emulator

In August of 2011, Mentor Graphics Corporation donated a Veloce® Solo emulator to Portland State University (PSU), and has worked with the Electrical and Computer Engineering (ECE) department at PSU to integrate hardware assisted (emulation) technology information into both the upper division undergraduate and graduate curriculum.

In integrated circuit design, hardware emulation is the process of imitating the behavior of one or more pieces of hardware with another piece of hardware, typically a special purpose emulation system. The goal is normally debugging of the system being designed. Often an emulator is fast enough to be plugged into a working target system in place of a yet-to-be-built chip, so the whole system can be debugged with live data.

"As electronic systems move aggressively toward increased complexity, there becomes a greater demand for design verification and validation engineers," said Renjeng Su, Dean of the Maseeh College of Engineering and Computer Science, Portland State University. "With Mentor's help, we've developed much more sophisticated design examples and labs that allow our students to learn cutting-edge verification methods and tools. This means they enter the workforce with real-world experience."

At PSU some undergraduates, and many graduate students, take an ASIC design course and the graduate students follow that with an ASIC verification course. These two courses were chosen to introduce hardware emulation into the curriculum because of the natural fit with the current content and because of the relatively large enrollment in those classes. In the Fall of 2010, PSU added coverage of hardware emulation in a graduate course in high-level synthesis and design automation.

"The faculty in the Electrical and Computer Engineering department teaches advanced methods, but until recently their design examples were limited to the component level or descriptions of systems at a low level of complexity," said Greg Hinckley, president and COO at Mentor Graphics. "With the joint efforts of PSU and Mentor, we have been able to bring the necessary tools and expertise together to raise the level of complexity of classroom examples and challenge the students to achieve a higher-level of learning."

Mentor Higher Education Program

Mentor Graphics, a technology leader in electronic design automation (EDA) with the broadest industry portfolio of best-in-class products, founded the Higher Education Program (HEP) in 1985 to further the development of skilled engineers within the electronics industry. HEP provides schools around the globe with leading-edge design tools for classroom instruction and academic research to help ensure that engineering graduates enter industry proficient in state-of-the-art tools and techniques. To date, Mentor Graphics is proud to have partnered with more than 1200 academic institutions worldwide.