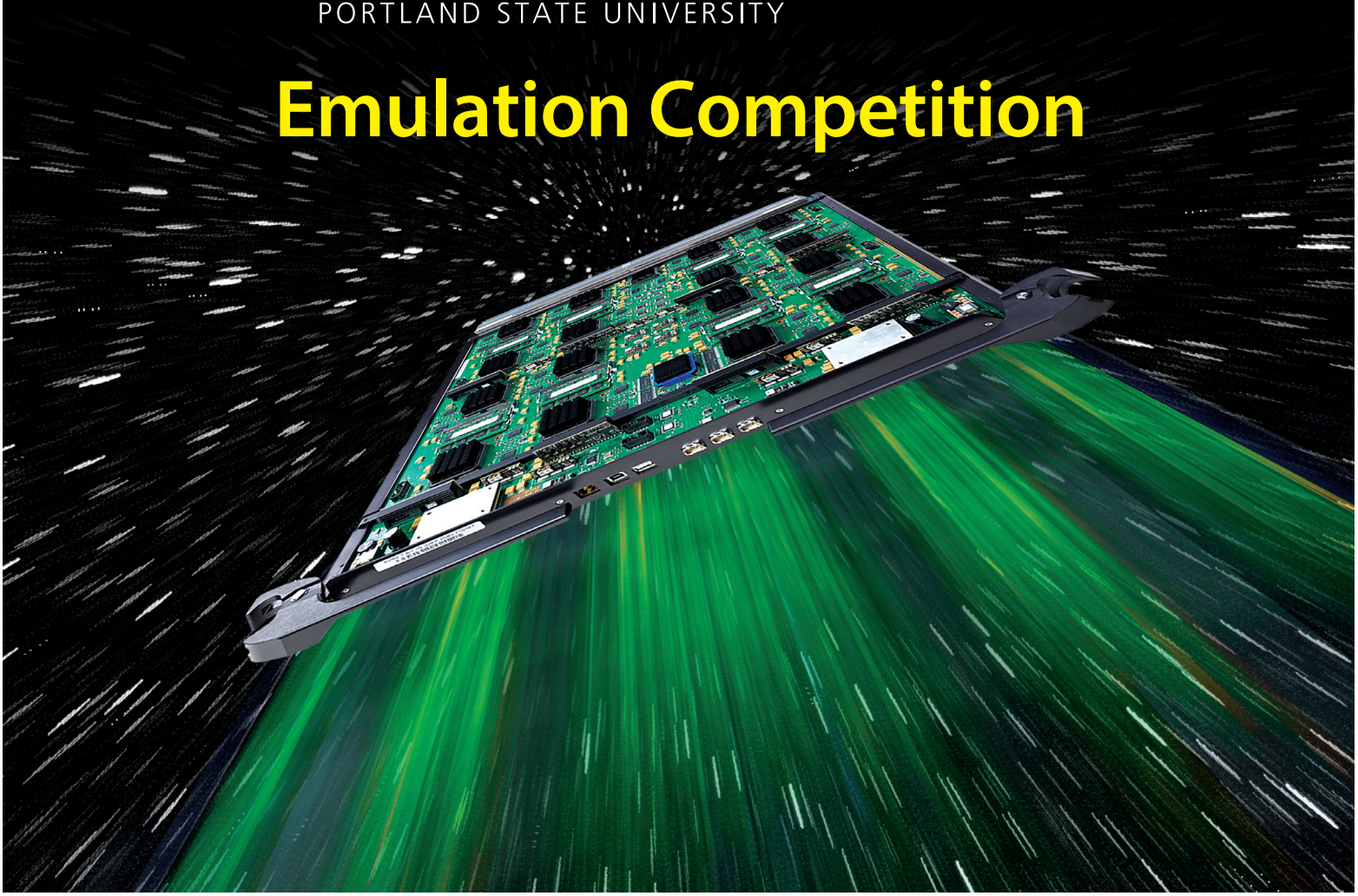
3rd Annual

NEED FOR SPEED

Maseeh College of Engineering and Computer Science

PORTLAND STATE UNIVERSITY

Emulation Competition



Friday, November 18th, 2016 - 9:30 a.m. to 1:30 p.m.

8005 SW Boeckman Road - Wilsonville, OR 97070

Deschutes Conference Room (D1320)

Sponsored by Mentor Graphics

Message from the Dean

The Fariborz Maseeh College of Engineering and Computer Science at Portland State University is a research-integrated engineering school that evolved in parallel with the growth of the high-tech industry in Oregon. More than 3,000 students are currently enrolled in programs that lead to Bachelors, Masters, and PhD degrees in civil engineering, computer engineering, computer science, electrical engineering, environmental engineering, mechanical and materials engineering, and engineering and technology management and systems engineering.

Maseeh College has close industrial ties, which offer students opportunities for internships and to study cutting-edge, problems. Many participate in research, industrial projects, prestigious competitions, and the college's student-driven Innovation Programs.

The Electrical and Computer Engineering Department is the second largest department in the Maseeh College. Its teaching and research laboratories are equipped with modern industry-grade equipment for measurement, test, and prototyping.

Maseeh College faculty members have outstanding strengths in a number of fields including Tera-Hz devices, Acoustics Electromagnetics, IC Design and Test, Power Engineering, Embedded Systems, and Communications.

A multi-year process is currently underway at Maseeh College to establish a nationally-recognized program in Design Verification. The program is founded on two important premises. The first is that design verification is increasingly becoming a central and demanding process in modern digital designs due to drastically increasing complexity and the need for speed. The second is that there is a huge and rising demand for verification engineers who are well versed in modern verification technologies.

A focused Design Verification curriculum has been developed, which is supported by faculty from Electrical and Computer Engineering and from Computer Science who are actively engaged in developing new design verification technologies.

Renjeng Su, D.Sc.
H. Chik M. Erzurumlu Dean
Maseeh College of Engineering and Computer Science

Maseeh College of Engineering and Computer Science
PORTLAND STATE UNIVERSITY

"Need for Speed" competition background

The Need for Speed Veloce Emulation Competition was conceived of as a joint effort by Mentor Graphics and the Portland State Electrical and Computer Engineering Department to encourage more students to explore hardware emulation by tackling industry-level engineering challenges.

The competition's theme underscores growing demand for sophisticated testing hardware and design verification talent. Complex designs can take hours or even weeks to adequately test. Emulation tools, such as the Mentor Graphics Veloce, are capable of dramatically accelerating this process allowing for more thorough verification before production. This results in higher quality products and faster time to market.

A total of $9,000 in prize money was funded by an anonymous donor. Five thousand dollars in prize money will be awarded to the first-place team, $3,000 for second place, and $1,000 for third place.

Local industry leaders Intel, Imagination Technologies, and Compound Photonics, along with PSU staff members form this year's judging panel.

PSU professors Tom Schubert and Mark Faust served as team mentors and helped to make the event possible.

Agenda - Friday, November 18, 2016

TIME	TOPIC	PRESENTER
9:30 a.m. – 9:50 a.m.	**Check-in**	**Students & Guests**
9:50 a.m.	**Welcome & Introduction** *(Intel, Imagination Technologies, and Compound Photonics)*	Renjeng Su & Kenneth Larsen
10:00 a.m. – 12:00 p.m.	**Contest Presentations**	
10:00 a.m.	IDEA Algorithm Pipeline *(Randon Stasney)*	**Team 1**
10:30 a.m.	Emulator Based Verification of Synthesizable and Configurable Multicore Cache Controller *(Sai Krishna Ravuri & Aditya Pawar)*	**Team 2**
11:00 a.m.	Self-Organizing Incremental Neural Network Based on General Associative Memory Structure *(Vishwas Pulugu & Vasudev Rupanaguntla)*	**Team 3**
11:30 a.m.	Efficient Verification of an Elaboration-time, Key Size Configurable Pipelined AES Encoder and Decoder using a Mentor Veloce Emulator *(Daniel Collins & Alex Pearson)*	**Team 4**
12:00 p.m. – 12:15 p.m.	**Break for Judging**	**All** (except judges)
12:15 p.m. – 12:30 p.m.	**Announcement of Winners & Photos - Wrap-up**	Tom Schubert
12:30 p.m. – 1:30 p.m.	**Lunch**	**All**

2016 Competition Finalists

IDEA Algorithm Pipeline
Randon Stasney

Efficient Verification of an Elaboration-Time, Key Size Configurable Pipelined AES Encoder and Decoder using a Mentor Veloce Emulator
Daniel Collins, Alex Pearson

Emulator Based Verification of Synthesizable and Configurable Multicore Cache Controller
Sai Krishna Ravuri, Aditya Pawar

Self-Organizing Incremental Neural Network Based On General Associative Memory Structure
Vishwas Pulugu, Vasudev Rupanaguntla

Additional Entries

DDR4 functional model Memory Controller with UVM
Hussein AlAmeer

Design and Verification of a Floating Point Unit
Sai Cherupally, Rudraraju Kiran, Varma Karthik

Calculator
Manasa Gurrala, Venkata Yalla, Bharath Godi

Speed and Accuracy Analysis of a Stochastic Computer for Linear Dynamic Equations
John Parker

Competition Judges from Industry

Tom Berg

Principal Engineer, Imagination Technologies

Tom Berg is a Principal Engineer at Imagination Technologies where he leads the hardware development of multi-core, L2 cache and IO-coherence technologies. Tom has 25+ years of pushing the state-of-the art in coherent multi-processing computer systems with companies such as Sequent Computers, IBM, PMC-Sierra, and MIPS Technologies. He received his BS in Electrical and Computer Engineering from The University of Michigan and his MS in Electrical Engineering from Purdue University. Tom has been named on 16 patents in many aspects of computer systems.

Bruce Ableidinger

Technical Marketing Manager, Development Tools, Imagination Technologies

Bruce has had a varied career in hardware instrumentation and tools, having worked at Tektronix, Intel, several startups, and now the MIPS division of Imagination Technologies. For over 30 years he has pursued tool solutions to enable SoC hardware and software developers to get products to market. With the growth of transistor budgets, more features continue to be added on-chip to processors and systems in the form of debug hooks and performance monitoring IP. Bruce was instrumental in defining numerous debug IP blocks that are now widely deployed in architectures ranging from the 8051, x86 and now MIPS cores.

Bruce has a BSEE degree from Washington State University and an MSCS from Oregon State University. He has several patents in the area of logic analyzers, hardware trace, and performance analys

Leon Lim

Engineering Manager, Intel Corporation

Lim is an Engineering Manager at Intel Corp. He manages engineering teams who are responsible for hardware emulation of multiple Xeon Servers, HPC and data center products. Lim has a MSEE from OHSU and BSEE from the University of Washington. He has 18 years of industry experience ranging from board design, FPGA & ASIC design to hardware emulation and FPGA prototyping.

Satish Munirathnam

Engineering Manager, Intel Corporation

Satish is an Engineering Manager at Intel Corp, responsible for emulation effort for the Xeon Phi (MIC) segment. Satish brings with him many years of industry validation and emulation experience. Satish holds MSEE from Oklahoma State University.

Andrew Iverson

Engineering Manager, Compound Photonics

Experienced ASIC design and verification engineer with 16+ years of experience in all areas of an ASIC design cycle including system/chip-architecture, block-level micro-architecture, Verilog design, SystemVerilog verification, production testing, lab bring-up and validation, and embedded software. Specialties: ASIC design, ASIC verification, SystemVerilog, OVM, Embedded Software. Andrew holds a MSEE from OHSU and a BSEE from Montana State University-Bozeman.

Competition Judges from PSU

Tom Schubert, Ph.D.

Design Verification and Validation Instructor – Electrical and Computer Engineering

Maseeh College of Engineering and Computer Science, Portland State University

Schubert recently joined the Electrical and Computer Engineering faculty at Portland State University and directs a graduate track in Design Verification and Validation. Previously, he was at Intel Corporation for 17 years, where he was a senior pre-silicon validation manager for many generations of microprocessor/SOC designs. He also led Intel's largest formal verification team developing techniques that were applied across the company. Tom received a Ph.D. in Computer Science from the University of California, Davis.

Mark Faust

Assistant Professor – Computer Architecture

Maseeh College of Engineering and Computer Science, Portland State University

Faust is an assistant professor in the Electrical and Computer Engineering Department at Portland State University where he teaches a variety of courses in digital design and computer architecture, as well as SystemVerilog. Prior to coming to PSU in 2004, Mark was General Manager for Asian Operations for Credence Systems Corporation. Before joining Credence, he held a variety of engineering and engineering management positions at several startups. He earned BS and MS degrees from Carnegie Mellon University.

Roy Kravitz,

Instructor and Westside Program Director

Maseeh College of Engineering and Computer Science, Portland State University

Professor Kravitz is a full-time instructor and the Director of the ECE Westside program. He has created and co-taught courses in FPGA design, digital systems design, embedded systems, and computer architecture for more than 15 years.

Kravitz's professional career spans more than 35 years in multiple companies and roles. He started as a micro-processor designer at Intel and completed 5 years as VP of Engineering for BPL Global before switching to Academia. Roy earned his BS Computer Engineering and MS Electrical Engineering from the University of Illinois, Urbana. His interests include embedded system hardware and software, digital system design using programmable logic, Android programming, and computer architecture.

Judges, winning teams, and representatives of Mentor Graphics at the competition in 2015.

Emulator used for this competition

Veloce® Solo emulator

August 22, 2011 - Mentor Graphics Corporation announced it has donated a Veloce® Solo emulator to Portland State University (PSU), and has worked with the Electrical and Computer Engineering (ECE) department at PSU to integrate hardware assisted (emulation) technology information into both the upper division undergraduate and graduate curriculum.

In integrated circuit design, hardware emulation is the process of imitating the behavior of one or more pieces of hardware with another piece of hardware, typically a special purpose emulation system. The goal is normally debugging of the system being designed. Often an emulator is fast enough to be plugged into a working target system in place of a yet-to-be-built chip, so the whole system can be debugged with live data.

"As electronic systems move aggressively toward increased complexity, there becomes a greater demand for design verification and validation engineers," said Renjeng Su, Dean of the Maseeh College of Engineering and Computer Science, Portland State University. "With Mentor's help, we've developed much more sophisticated design examples and labs that allow our students to learn cutting-edge verification methods and tools. This means they enter the workforce with real-world experience."

At PSU some undergraduates, and many graduate students, take an ASIC design course and the graduate students follow that with an ASIC verification course. These two courses were chosen to introduce hardware emulation into the curriculum because of the natural fit with the current content and because of the relatively large enrollment in those classes. In the Fall of 2010, PSU added coverage of hardware emulation in a graduate course in high-level synthesis and design automation.

"The faculty in the Electrical and Computer Engineering department teaches advanced methods, but until recently their design examples were limited to the component level or descriptions of systems at a low level of complexity," said Greg Hinckley, president and COO at Mentor Graphics. "With the joint efforts of PSU and Mentor, we have been able to bring the necessary tools and expertise together to raise the level of complexity of classroom examples and challenge the students to achieve a higher-level of learning."

Mentor Higher Education Program

Mentor Graphics, a technology leader in electronic design automation (EDA) with the broadest industry portfolio of best-in-class products, founded the Higher Education Program (HEP) in 1985 to further the development of skilled engineers within the electronics industry. HEP provides schools around the globe with leading-edge design tools for classroom instruction and academic research to help ensure that engineering graduates enter industry proficient in state-of-the-art tools and techniques. To date, Mentor Graphics is proud to have partnered with more than 1200 academic institutions worldwide.

Project finalist 1

Randon Stasney

Randon Stasney is an Electrical and Computer Engineering graduate student at Portland State University. In March of 2017 he will complete his masters in the embedded systems track. He is currently a Teaching Assistant at PSU for Dr. Hall's Microprocessors class and last spring had the opportunity to be a TA for Dr. Schubert's Emerging Functional Verification Methods class. He recently completed development of a timing project for Prof. Kravitz's SOC Design with FPGAs class.

Through several successful school projects, Randon has gained proficiency and confidence using SystemVerilog and Mentor Graphics tools. Some examples include: creating a pipelined HW design with forwarding and an original ISA for the IDEA algorithm; verifying a UART design with BIST and BFM interface; designing a satellite hub controller FSM. He also created a dungeon scroller game for NEXYS 4 FPGA using PicoBlaze soft core processors. Additionally, his projects have involved interfacing with Beagle Bone Black, Arduino, and Raspberry pi through UART, I2C, and SPI.

IDEA Algorithm Pipeline

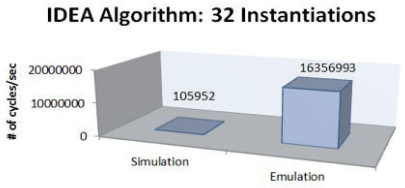
(Randon Stasney)

Abstract

The task was to design, model, simulate and test an application specific processor using the International Data Encryption Algorithm. As this was an exercise in latency and bandwidth I chose a pipeline processor with forwarding to maximize the throughput. The design was parallelizable, making it a good candidate for verification on the Veloce Emulator rather than traditional simulation. By emulating the design in Standalone Mode, I was able to achieve a speed-up factor of over 150 times in my verification.

Design

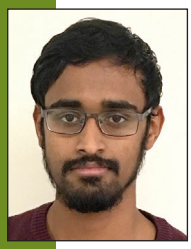
I created a SystemVerilog model of the 5-stage pipeline with forwarding based on "Computer Architecture – A Quantitative Approach" by Hennessy and Patterson. The problem constraints given were to design our own ISA with only the following ALU instructions: Add, Subtract, And, Or, Xor, and Multiplication. In addition, I was allowed to use Load, Store, and Jump, as well as limited Branches: Equal, Zero, Less Than Zero, and Greater Than Zero. The instructions were to be written in a text file representing a memory image that is 32-bits wide. The encryption results of 1024 bits of data were to be written back to this memory image.



Verification

1. Encoding data with the IDEA algorithm requires eight and a half rounds of operations using modulo addition, Xor, and modulo multiplication. I first verified the modulus multiplication functionality. Exhaustively testing both 16 bit operands gave me 4.2 billion tests.
2. This was accomplished by writing a simple assembly code loop in my constructed ISA. This also served to test my branch and jump functionality.
3. I constructed the test to return a result every eight cycles, which allowed my golden testbench in the Top module to calculate and then compare the results.
4. The Top module, being synthesizable, was also emulated, thereby maximizing speed-up. This allowed a simulator test taking 3.75 days to be emulated in less than 36 minutes.
5. Through minimal modification I was able to exhaustively test both the Xor and modulo addition.

Team finalist 2



Sai Krishna Ravuri

Sai Krishna Ravuri is a Graduate student at Portland State University in the Department of Electrical and Computer engineering. He is specializing in the field of VLSI Design and Verification . He will be graduating in June 2017.

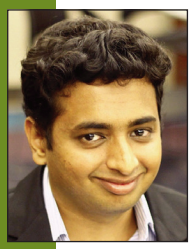
He completed his Bachelors in the department of Electronics and Communication Engineering from Jawarharalal Nehru Technological University, Anantapur, India. He has secured 97%le in GATE (Graduate Aptitude Test for Engineers) which was taken by 219,000 electronics engineers all over India.

VLSI has been his field of interest right from Bachelors which prompted him to specialize in this field . Sai has not confined to any particular track in this field . He has always tried to perform better in logic design as well as verification, which made him to work on the emulator stuff to explore its advantages (for the purpose of verification).

He got a chance to work on emulator as a part the final project during the course 'Introduction to System Verilog' offered by Prof. Mark Faust . He further enhanced that project , which helped him entering the finals of the Emulation Competition being conducted by Mentor Graphics. He is working as Teaching Assistant at present, for the same course under Prof . Mark Faust .

He has experience with the scripting languages like Perl and Python, programming languages like C and C++.

Sai is currently looking for an opportunity in the field of Design or Verification in semiconductor industry.
He can be reached reached at 'sairavuri93@gmail.com' or 's23@pdx.edu'.



Aditya Pawar

Aditya Pawar is a graduate student in Electrical and Computer Engineering at Portland State University, Oregon. Aditya's specialization is Design Verification and Validation. He obtained his Bachelors of Engineering in Electronics and Telecommunications at the University of Mumbai. So far he has completed Microprocessor System Design, SystemVerilog, ASIC Verification, Post Silicon Functional Validation, and Digital IC Design courses and is currently working on System on Chip using FPGAs and ASIC Design courses.

Aditya's interests include verification of systems in the pre-silicon and post silicon phase. He is fascinated by the ingenuity required to create scenarios which will result in finding bugs. As part of the ASIC Verification course he has created a verification environment for a single cycle MIPS processor which consists of a golden model, generator driver, scoreboard and coverage monitor. Another project was the verification of a dual port FIFO in which he verified the working of the FIFO and emulated the design on a Veloce Solo emulator. For post silicon validation he has done work on JTAG and validation of the IA 32 architecture in which he utilized randomization of encoded instructions and implemented multi-threading execution of instruction sets.

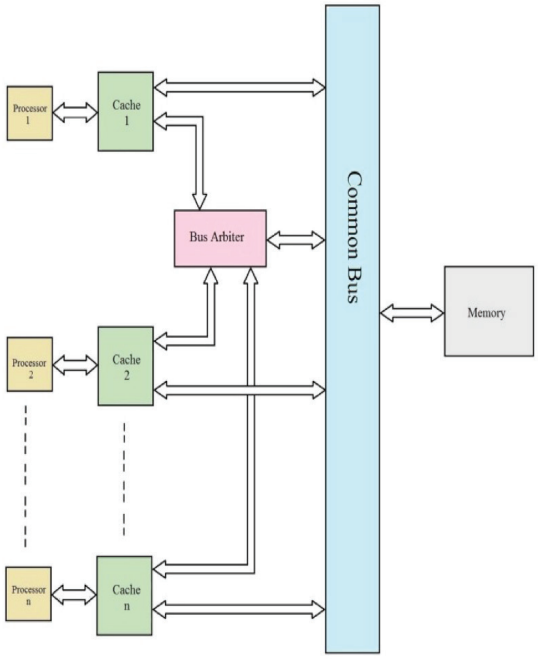
Next to his studies, Aditya likes to participate in academic competitions like the PSU Need For Speed Veloce Emulation Competition and ROBOCON. His hobbies include reading Japanese manga, fiction novels, watching anime, travelling to new places and trying new food.

Project finalist 2

Emulator Based Verification of Synthesizable and Configurable Multicore Cache Controller

(Sai Krishna Ravuri, Aditya Pawar)

The goal of the project is to explore the advantages of emulation over simulation. For this purpose, we have designed a Multicore Cache Controller in SystemVerilog. The Dragon protocol was adopted for maintaining coherence between the caches and memory.
The Cache Controller and Bus Arbiter were modeled as state machines and the Processor Module generates READ/WRITE requests following Spatial and Temporal locality. The entire design was implemented in SystemVerilog.



QuestaSim was used for the purpose of simulation and Mentor's Veloce Solo Emulator was used for the purpose of emulation.

Our verification was based on a bottom-up + re-use strategy.

The goal of our verification is to get 100% coverage of our functional coverpoints without the checker throwing any error. Coverage was calculated only for random testcases, not the deterministic cases.

Initially all the lower level modules like Memory, BusArbiter and Processor modules were tested . Then the verification was moved to a higher level where all the modules including the Cache Controller were configured using the Common Bus.

The number of cores was configured as 2 at first and then it was made 16.

Checkers used at lower levels were reused at the top level. And the checker was designed to make sure that properties like Protocol State Transitions, BusGrants and other properties are being satisfied all the time.

Regarding stimulus (READ/WRITE requests), a set of deterministic stimuli was maintained for the purpose of initial verification. Then constrained random stimuli were generated through the processor module.

Coverpoints were introduced at points like State Interactions of the controllers, Requests to BusArbiter etc. to calculate the functional coverage.

The run-times on the emulator and simulator were compared to calculate the speed-up achieved by the emulator over the simulator.

We achieved a speed-up of 67x (for 16 cores) using emulation over pure simulation and a functional coverage of 97%.

Using the emulator we were able to run test cases of up to 1,000,000 in a very short time compared to simulation. As a result, the verification process was made faster which helped in saving a significant amount of time.

You can gain even more in time with bigger designs as execution is done in parallel in hardware.

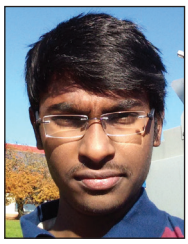
Project finalist 3

Vishwas Pulugu

Vishwas Pulugu graduated with a Masters in Electrical and Computer Engineering from Portland State University in the spring of 2016, with a special interest in Computer Architecture, Logic Design, and Validation. His course work includes Computer Architecture, Digital Design using HDL, SystemVerilog, and Emerging Functional Verification Methods. He has worked on a multicore cache simulator, the emulator-based design and verification of a dual elevator system, and the implementation of a dual segmented LRU to improve IPC of a simple scalar processor simulator, as part of coursework which also includes 3 emulator-based verification projects.

Prior to joining PSU, Vishwas obtained his BE in Electronics and Communication Engineering from Osmania University, India, and was actively involved in robotics organizing a robotic workshop for designing a Gesture Control Robot using an 8051 Micro-Controller.

Vishwas is currently working as Validation Test Engineer at Intel (Contract). He is actively looking for full-time opportunities in the fields of Computer Architecture, Design, and Validation. He can be reached at vishwas.pulugu@gmail.com.



Vasudev Rupanaguntla

Vasudev Rupanaguntla recently joined Intel Corporation, Hillsboro as a Validation Engineer. He earned his MS degree in Electrical and Computer Engineering from Portland State University and has a BE from Osmania University, India. Key projects as part of course work includes, i) Emulator based Design and Verification of configurable L3 cache ii) Improving Simple Scalar Simulator's IPC iii) Design and Characterization of Standard Cells. He is interested in Computer Architecture, Verification, and Validation. He is also passionate about nature and soccer.

Self-Organizing Incremental Neural Network Based On General Associative Memory Structure

(Vishwas Pulugu, Vasudev Rupanaguntla)

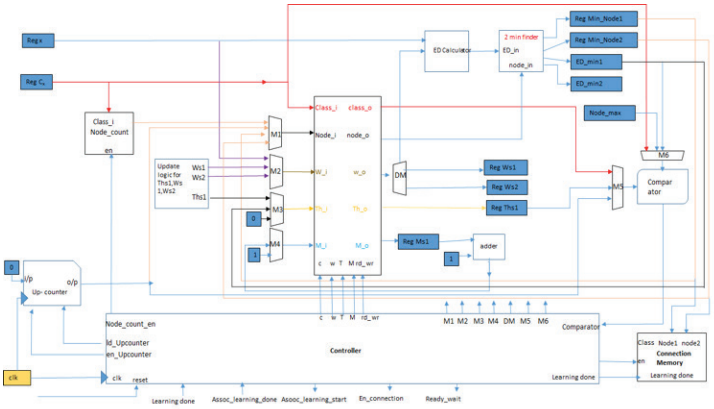
Overview:

The aim of this project is to design and verify a self-organizing memory structure which can be used to detect vectors from incomplete inputs. We verified the design using transaction-based modeling for the Veloce Solo hardware emulator. This can be useful for image recognition, speech recognition, and artificial intelligence.

Design:

We designed FSMD to implement learning and recalling algorithms proposed in " A general associative memory based on self-organizing incremental neural network." This design was developed as synthesizable SystemVerilog RTL. It can be configured to detect any number of unique patterns with the desired level of accuracy. Design modules include

1) Controller with 13 states
2) Memory (Memory Layer and Connection Memory)
3) Euclidian Distance calculator, Learned Vector Calculator
4) Comparator, Multiplexers, and Counters



Verification:

We developed a SystemVerilog testbench for the Veloce TBX mode. SCEMI transaction pipes were used for communication between the HVL testbench and the HDL design. In the learning phase, vectors and their corresponding unique pattern names are sent from the HVL to the HDL side, and in the recalling phase the output is compared against expected results in the HVL testbench to determine the accuracy of the algorithms.

Vectors for the learning phase were obtained from the MNIST image database. We generated multiple sets of images as input vectors in the HVL testbench for the recalling phase by performing vector operations on images from the MNIST database. Assertions and code coverage were used in the verification process. The simulation run-times demonstrated speed-up on the Veloce Solo emulator over the QuestaSim simulator for various design configurations and test cases.

Project finalist 4

Daniel Collins

Daniel Collins is a graduate student at Portland State University pursuing his MS in Computer Architecture and Design. He graduated Magna Cum Laude with a BS in Computer Engineering from Gonzaga University in early 2015, taking a year and a half internship at Intel Corporation in 2013 on a vertically integrated Emulation, Validation Tools, and Validation team. His undergraduate capstone project was building a software defined radio interference source using a Zynq-7000 (dual-core ARM Cortex A9 + Kintex-7 Xilinx FPGA) SoC with an FMC connected transceiver.

For the last two years, Daniel has worked at Intel Corporation as a System Validation engineer on next-gen hardware accelerator IPs used in data center chipsets and communications SoCs. His background in embedded systems has guided his professional interests towards firmware engineering, heterogeneous computing architectures, and accelerators.

Alex Pearson

Alex Pearson is a graduate student at Portland State University working toward his MS in Electrical and Computer Engineering with a focus on Computer Architecture. He has completed courses including Embedded Programming, Computer Architecture, and SystemVerilog.

For the past three years Alex has worked for Mentor Graphics in the Design to Silicon division as a Technical Marketing Engineer. In this role, he supports development and foundry deployment of the Calibre DRC and Multi-Patterning products for advanced IC manufacturing process nodes.

Alex graduated Summa Cum Laude from Oregon State University with a BS degree in Electrical and Computer engineering. As an undergraduate student he interned with Intel Corporation and Mentor Graphics through the MECOP program. At Oregon State University he held positions as teaching assistant, undergraduate research assistant, and graduate research assistant.

Efficient Verification of an Elaboration-Time, Key Size Configurable Pipelined AES Encoder and Decoder using a Mentor Veloce Emulator

(Daniel Collins, Alex Pearson)

Abstract:
Our project represents work done to efficiently verify an Advanced Encryption Standard (AES) encoder and decoder using Mentor Veloce emulation technology. We detail the design, explain the verification strategy, and identify bottlenecks and design limitations. We discuss efforts to overcome or mitigate those hurdles and show the benefit of effectively utilizing co-model emulation. We present our results and demonstrate the speedup achieved by using the Veloce emulator. Finally, we explore challenges encountered and discuss their impact on emulation performance.

Design:
Our starting design was a compile-time, key size configurable, pipelined AES encoder and decoder developed for PSU class ECE 571. The design supports the three different keys sizes specified in the AES standard (FIPS 197). We implemented the design in a hierarchical manner, creating sub-modules for the different stages in each round, a round and key expansion module, buffered round module, and a top level cipher (encoder) and inverse cipher (decoder). As part of the competition, we adapted the design to be elaboration-time configurable so that we can verify multiple DUT instantiations of different key sizes in parallel in the same testbench and simulation/emulation run. An attempt was also made to reduce the critical path in hopes of achieving a higher emulation frequency.

Verification:
As part of our initial design, we created testbenches for each module that use known answer test vectors created by our own test generator written in C. Our top level testbench uses these pseudo-randomly generated test vectors along with pre-computed expected values in order to efficiently test the DUT(s) using on-emulator SystemVerilog assertions. We utilize a SystemVerilog based HVL testbench communicating with the XRTL HDL Transactor running on the Veloce emulator, communicating through SCEMI pipes. We strategically compute and pack our input and output values for transmission to the emulator in order to reduce the expense of communicating with the emulator. Additionally, on the emulator we expand a single communicated message into a series of unique tests, a process which further reduces the communication overhead.

Results:
Comparing our emulation and simulation run-times we are able to achieve a nearly 400x speed-up of emulation over simulation. This reduces a multi-hour simulation run to thirty seconds on the emulator by efficiently utilizing the communication bandwidth between the emulator and co-model host and exploiting the parallel nature of the Veloce hardware.

Past winners – where are they now?

Sanket Borhade

Joined Mentor Graphics as Corporation Application Engineer

"The competition motivated me to learn SystemVerilog and Verification Methodologies. Mentor Graphics donated Veloce Solo to Portland State University, which really helped in learning the new and in-demand technology. This competition gave a platform to showcase our design and test results to people from various companies.

The competition clearly paved the way to understand the differences between emulation and simulation. Following the competition, I received a job at Mentor Graphics on the Design Verification Technology team as Associate Rotation Engineer.

Renjeng Su, Sanket Borhade, Greg Hinckley, Sameer Ghewari, Kenneth Larsen

Sameer Ghewari

Joined Mentor Graphics as Emulation Specialist

Need for Speed Veloce Emulation contest was Launchpad for my career into the new and exciting field of hardware emulation. The contest literally "emulated" a real industry setting for students; right from proposal to the final round.

Steven Bellock

Joined Mentor Graphics as SW Development Engineer

"In the summer of 2014 I took Professor Mark Faust's introduction to SystemVerilog course at the Willow Creek Center in Beaverton. Part way through the term he announced the first PSU / Mentor Graphics Veloce emulation competition which was to be held that fall. . .

My entry to the competition was titled "Computation of Jacobsthal's Function Hardware Accelerator" and it sought to crunch some numbers and expand mathematicians' knowledge of Jacobsthal's function. The project worked well with hardware emulation, as the accelerator could do many of its computations in parallel.

Renjeng Su, Steven Bellock, Greg Hinckley, Kenneth Larsen

Ashok Raju

Joined Intel - Folsom, CA

I participated in the competition last year and got second place. I graduated from PSU last December and I have been working at Intel in Folsom for the past 5-6 months. The competition was a fine learning experience on how to make good use of the emulator and helped me appreciate its utility.

Renjeng Su, Greg Hinckley, Ashok Raju