PSU ECE 510

Topic: PreSilicon Design Verification using FPV

This class will give you an understanding on how Pre-silicon verification is done in industry. We will focus on the use of formal property verification (FPV) and by the end of the class you will have the knowledge and skills to accelerate your development of correct RTL designs (both commercial designs and designs you would create in other classes).

For some time, there has been an upward trend in the amount of effort industrial integrated circuit projects have required to validate designs. Industrial surveys indicate a majority of projects have required more than 50% of the time focused on validation and some projects have spent more than 70% of their time on validation. This "validation crisis" has led to the invention of sophisticated strategies and infrastructure to address increasing complexity. One technique that has emerged to rigorously check a developing design with a minimal amount of overhead, is SAT checking using System Verilog Assertions. In contrast to conventional test bench use, FPV requires much less test bench code development, is much faster to deploy, and for many applications, provides far greater assurance a design is correct.

This class will discuss pre-silicon design verification in general and introduce practical approaches to apply formal verification techniques (SAT checking) to industrial scale RTL designs. Topics include an introduction to pre-silicon verification techniques, formal verification tools, formal verification theory, and system verification problem solving approaches based on solutions to real microprocessor design problems. Students will gain experience using formal verification to validate modern digital designs. The course will cover methodology followed by hands on experience using formal verification techniques. Some formal verification theory is presented throughout the course, but most is deferred until the end of the course.

Familiarity with computer architecture and hardware description languages required. You'll need to be able to read and debug Verilog RTL. In the class you will learn to write System Verilog Assertions and use a very limited subset of System Verilog. A design project is an integral part of this course. The course material complements other ECE pre-silicon and post-silicon functional validation courses.

Prerequisites: Basic knowledge of computer architecture and hardware description languages (Verilog recommended).

Course Coordinator/Instructor: Tom Schubert
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Office Hours: Tuesday, Thursday 2:30-3:30**,** or by appointment

D2L website active: Lecture notes, papers, homework assignments and dropbox, announcements, etc

Textbook

- Formal Verification: An Essential Toolkit for Modern VLSI Design, Seligman, Schubert, Kumar, 2015. The text is also on reserve at the PSU library.

References

- From SVA: The Power of Assertions in System Verilog, Cerny, Dudani, Havlicek, and Korchemny, 2015.
- Logic Design and Verification Using SystemVerilog, Thomas, 2016.
- Mentor Graphics Functional Verification Manuals

Outline of Course Content

- PreSilicon Design Verification Overview
- System Verilog Assertions
- Formal Property Verification

- Effective FPV for Design Exercise
- Effective FPV to Verify RTL Designs
- FPV in Restricted Domains
- False Positives in Formal Verification
- Deployment
- Basic FV Algorithms
- State-Matching Formal Equivalence Verification

Student Learning Outcomes

1. Knowledge of role of validation in modern digital design projects
2. Knowledge of formal verification theory and application to digital design
3. Ability to use formal verification tools to model and validate evolving RTL designs
4. Understanding of the central nature of validation and the need for a structured, measured approach

Course requirements

- Midterm (20%), Final (25%), Project (30%), Homework (25%)

There will be approximately 5 homework assignments. To pass the course, each assignment must be turned in on or before its due date. Some assignments may be done in groups. If you choose to work in a group, please turn in only one solution, indicating the names of all group members. Of course, individually, you will be expected to understand the material and demonstrate so on exams.

Some of the solutions might be obtained from previous classes. Using such solutions is **very** counterproductive! To pass exams, you'll need to develop analysis skills by working through problems. More importantly, working through the problems yourself, discussing in groups, or with the TA or me is the best way to learn the material. I strongly encourage you to come to my office hours after struggling and we'll work out the correct answer together.

Project: The project is an important educational complement to the material presented in lectures. A good project will encounter problems that will require some research to find a solution. We'll discuss the project in more detail in a few weeks, but you should soon start thinking about possible projects. The project will explore using formal verification techniques on an existing complex RTL design. The design needs to be sufficiently complicated to require significant testing such that you can insert a subtle error in the design that might be difficult to catch. While verifying a design written from scratch is possible, I highly recommend students start with a pre-existing Verilog design (e.g. an openCores design). I also encourage students to work in groups of 2 people. Students are expected to orally present their projects as well as turn in a written report.

Professionalism: In our worldwide discipline, we must work with many men and women from different cultures, races, sexual preferences, religions, political affiliations, etc. To pass this course, each student must demonstrate they are a good team player. Students are expected to work/learn in a harassment free environment with the highest professional standards.

As an instructor, one of my responsibilities is to help create a safe learning environment for my students and for the campus as a whole. We expect a culture of professionalism and mutual respect in our department and class. You may report any incident of discrimination or discriminatory harassment, including sexual harassment, to either the Office of Equity and Compliance or the Office of the Dean of Student Life. Please be aware that as a faculty member, I have the responsibility to report any instances of sexual harassment, sexual violence and/or other forms of prohibited discrimination. If you would rather share information about sexual harassment or sexual violence to a confidential employee who does not have this reporting responsibility, you can find a list of those individuals (http://www.pdx.edu/sexual-assault/get-help). For more information about Title IX, please complete the required student module “Creating a Safe Campus” in your D2L.

Academic Honesty: I enjoy teaching very much and consider students to be future colleagues. Thus plagiarism

is an extremely depressing thing for me to encounter and will be taken very seriously. Plagiarism is definitely not just a harmless prank. It can have very serious effects, harmful to your standing at the university, and possibly very harmful to your job prospects when you seek employment after graduation. The penalty for plagiarism is an F in the course and a letter describing the incident sent to the Vice Provost for Student Affairs. Please avoid any actions during an exam (e.g. talking, looking around, etc.) which might make the exam proctors doubt your honesty. Please also view PSU's Student Code of Conduct at **http://www.pdx.edu/dos/codeofconduct**

Doing Well: Lectures cannot cover all aspects of the material. Much of the detail will be learned through exercises or supplied by consulting the book and other online material. Ask me about anything that you don't understand, no matter how minor it seems. I recommend actively attending lectures. Many good discussions result from questions asked during class.

Finally, note that grading is non-competitive, so it is possible for everyone to do well.