Library Characterization and Static Timing Analysis of Single-Track Circuits in GasP
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Thesis Committee
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Introduction: GasP
Fast Asynchronous Symmetric Pulse Protocol
• Uses Single-Track Handshake signaling
• Lightweight in area and in power
• Flexible elastic communication

Flexibility + High Speed + Low Power + Low Area
• Makes an excellent circuit family for on-chip communication

More details on:
• http://arc.cecs.pdx.edu

Important for Multi-core and Parallel systems

Introduction (2): Single-Track Handshaking

Bi-directional 1-wire communication
Request=high, Acknowledge=low
2-phase return-to-zero handshake
Wire is driven briefly
Wire_{end1} starts/stops up-transition
Wire_{end2} starts/stops down-transition

ASSUMPTION-1:
The brief drive is long enough to get the transition to the other end

ASSUMPTION-2:
Voltage observed at the near-end reflects the voltage at the far-end

Introduction (3): Putting Things in Perspective

FAITH versus MEASUREMENT
• In GasP we use FAITH where we CAN
• and MEASUREMENT where we MUST

Thesis Goal:
• Develop a timing validation flow
• that translates FAITH into MEASUREMENT

Scope:
• GasP is the study target
• but the results apply also to other single-track families

Introduction (4): Timing Validation Flow

FAITH GasP Circuits
Generates Timing Constraints
• Analyse (Li Utah)
• Ken Steven
• Yang Xu
• GasP extension (PSU)
• Xiaoyu Song
• Hoon Park
• Jiebing He
• Jea-Woo Park
• ARC

Library Characterization
PSU: Swetha
NEW
Look Up Tables
GasP Black Box Model

Static Timing Analysis
Synopsys PrimeTime (USC)
• Peter Beerel
• Prasad Joshi
• Mallika Prakash

Timing Reports
MEASUREMENT
Outline

- GasP and its Relative Timing Constraints
- Library Characterization
  - Partition Relative Timing Constraints
  - Generate Simulation Environment
  - Generate Look Up Tables
- Static Timing Analysis
  - Run USC flow with my Look Up Tables
  - Inspect Timing Reports
- Conclusion and Future Work

6-4 GasP

Cycle time: 6 gates FORWARD + 4 gates REVERSE = 10

Another Way to Represent Constraint RT2

Outline - Reminder

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Partition RT2 constraint

- Cut red path at SUCC1+
- Cut blue path at SUCC1+
- FIRE1-

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Partition the 6-4 GasP circuit for RT2
Partition the 6-4 GasP circuit for RT2

First Circuit Enhancement for RT2

- What: Minimize the (BLUE) Reset Loop Delay by minimizing the delay of NOR-function A going down

- Formula:
  \[ \text{Input Separation Time} = \frac{(t_{in2} \uparrow - t_{in1} \uparrow)}{2} \]
  - tin2 too late, tin1 too late
  - tin1 first, tin2 first

How: by using a “demon in a box” Voltage Controlled Voltage Source
- That copies V(SUCC1) to V(nPRED1) without extra delay or load
- The VCVS in this picture
  - Minimizes the falling delay of gate A
  - and thus the delay of RT2 sub-path
  - LUTblue: SUCC1 + FIRE1

Second Circuit Enhancement for RT2

- What: Module M1 can only raise SUCC1 because it’s a single-track signal. So: SUCC1 must be re-initialized before the next simulation cycle
- How: another “demon in a box” Voltage Controlled Current Source
  - That uses as completion pulse signal FIRE_CS1 to reset SUCC1
  - by translating the surplus voltage on SUCC1 into a drain current
  - without delaying or loading SUCC1+

Relationship FIRE_CS1 to FIRE1 and SUCC1

- Reset: SUCC1 falls after FIRE1 falls and before FIRE1 rises
- Measurement: SUCC1 rises within the FIRE1 high-pulse window
- Mutual exclusion: VCCS drain current = 0A during the FIRE1 high-pulse window

Demon in action
Final Simulation Setup

- **Sweep**: Trash size widT (driver circuitry) and Load size wid2 (load circuitry)
- **Measure**: Timing and Voltage changes on in[1] and out[1]
- **Result**: (widT x wid2) → slope(in[1]), delay(in[1] to out[1]), slope(out[1])

... and the Look Up Table that it generates

<table>
<thead>
<tr>
<th>Input Slope [ps]</th>
<th>14.2</th>
<th>15.1</th>
<th>16.3</th>
<th>21.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0</td>
<td>35.8</td>
<td>8.6</td>
<td>36.3</td>
<td>8.6</td>
</tr>
<tr>
<td>18.2</td>
<td>37.7</td>
<td>10.0</td>
<td>38.0</td>
<td>10.1</td>
</tr>
<tr>
<td>59.3</td>
<td>41.6</td>
<td>13.8</td>
<td>41.9</td>
<td>14.2</td>
</tr>
<tr>
<td>101.4</td>
<td>45.0</td>
<td>18.0</td>
<td>45.3</td>
<td>18.0</td>
</tr>
<tr>
<td>142.8</td>
<td>49.0</td>
<td>22.8</td>
<td>48.4</td>
<td>22.5</td>
</tr>
<tr>
<td>185.1</td>
<td>53.0</td>
<td>26.9</td>
<td>51.9</td>
<td>27.0</td>
</tr>
</tbody>
</table>

LUTblue:SUCC1+FIRE1-

- Stores: (Input Slope x Output Load) → delay(in[1] to out[1]), slope(out[1])

... is used as follows

- **Delay (12.24ps, 0fF)**:
- **Slope (12.24ps, 0fF)**:

Landscape Graphs for the Look Up Table

**DELAY landscape** (color distinction every 10 ps)

**OUTPUT SLOPE landscape** (color distinction every 5 ps)

- **Both** are very amenable to linear approximation techniques

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Timing Report for RT2

RED path delay = 26.36 ps
BLUE path delay = 80.39 ps
RT2 is satisfied
Slack = 54.03 ps

Conclusion and Future Work

Take-Away:
- We now have a Timing Validation flow for single-track circuits
  - It translates FAITH (design assumptions) into MEASUREMENT
  - by generating Look Up Tables
  - that go into the USC Static Timing Analysis flow
  - which reports how well the FAITH holds up
- The proof of the pudding is in the eating
  - I used this flow to validate relative timing assumptions in 6-4 GasP
  - The results match with the results of my ASYNC 2010 publication

Future Work:
- Wire delay model
  - with near-end capacitive load and far-end delay information
- Flow automation

THANK YOU!