Lecture 19

MEMORY

RAM, ROM and memory systems

Slides of Adam Postula used
Each word in the RAM memory can be read by giving its address and observing the data lines after some time.

Each word can be re-written by giving its address, presenting the new data and keeping it stable for some time.

Addressing can be random (there are no requirements for any sequence in addresses) - hence Random Access Memory.

Storage matrix is usually very large and organised as a square matrix of word cells.
256x4 bit RAM
internal organisation

A square storage matrix (32 x 32) makes an optimal design for the layout and delay minimisation.
256x4 bit RAM

Common I/O data lines
256x4 bit RAM
Separate I/O data lines
Read RAM Timing

**READ CYCLE**

- **WE**
- **CS**
- **Address**
- **Data Out**
Read RAM Timing

◆ READ CYCLE

- WE
- CS
- Address
- Data Out
Read RAM Timing

- READ CYCLE

[Diagram showing timing signals for WE, CS, Address, and Data Out]
Read RAM Timing

**READ CYCLE**

- **WE**
- **CS**
- **Address**
- **Data Out**

- $T_{ACS} = 45\text{ns}$
- $T_{AA} = 45\text{ns}$
Read RAM Timing

 unreadable
Read RAM Timing

READ CYCLE

WE
CS
Address
Data Out

$T_{RC} = 45\text{ns (min)}$

$T_{ACS} = 45\text{ns (max)}$

$T_{AA} = 45\text{ns (max)}$
Read RAM Timing

**READ CYCLE**

- **WE**
- **CS**
- **Address**
- **Data Out**

- $T_{RC} = 45\text{ns (min)}$
- $T_{ACS} = 45\text{ns (max)}$
- $T_{AA} = 45\text{ns (max)}$
RAM Dynamic Parameters

**READ CYCLE**

- **WE**
- **CS**
- **Address**
- **Data Out**

- \( T_{RC} = 45\text{ns (min)} \)
- \( T_{ACS} = 45\text{ns (max)} \)
- \( T_{THZ} = 10\text{ns (max)} \)
- \( T_{OH} = 5\text{ns (min)} \)
- \( T_{AA} = 45\text{ns (max)} \)

\[ THZ = 10\text{ns (max)} \]
Write RAM Timing

◆ WRITE CYCLE

- WE
- CS
- Address
- Data In
- Data Out

DATA VALID
Data Undefined
Write RAM Timing

**WRITE CYCLE**

- **WE**
- **CS**
- **Address**
- **Data In**
- **Data Out**

DATA VALID

DATA Undefined
WRITE CYCLE

- WE
  - TCW = 45ns (min)
- CS
  - TWP = 45ns (min)
- Address
- Data In
  - DATA VALID
- Data Out
  - Data Undefined

DATA VALID

TDW
Write RAM Timing

**WRITE CYCLE**

- **T_{WP} = 45\text{ns (min)}**
- **T_{CW} = 45\text{ns (min)}**
- **T_{WC}**
- **T_{DW} = 15\text{ns}**
- **T_{DH} = 5\text{ns}**

**DATA VALID**

Address

Data In

Data Out

Data Undefined

12/8/2002
Read Only Memory - ROM

Vdd

word 0

word 1

word N

Do0 | Do1 | DoN-1 | DoN

MOS transistor
Read Only Memory - ROM

ADDRESS DECODER

A0
A1
An

No transistor

word 0
word 1
word N

Active high word lines
Active low internal data lines

Vdd

Do0
Do1
DoN-1
DoN
Erasable Programmable Read Only Memory - EPROM
THE BASIC ELEMENT IS A CAPACITOR THAT HOLDS THE STORED VALUE ONLY FOR A SHORT TIME. THE STORED VALUE MUST BE 'REFRESHED' PERIODICALLY TO PREVENT LOSS OF DATA.
DYNAMIC RAM MEMORY

STORE AND REFRESH OPERATION

Vcc

1 written refresh refresh refresh 0 written

0 stored

0 bit line

N bit line

word select
DYNAMIC RAM MEMORY

64 k bits = 256 x 256

Dout
Din

/WE
/RAS
/CAS

row address latch
row decoder

CONTROL

row data latch

column address latch

data multiplexer/demultiplexer

A0-A7
( A8-A15 )

A0-A7

12/8/2002
Dynamic RAM Timing

- **RAS ONLY REFRESH CYCLE**

  - **Address**
  - **Row Address**

  Load row-address
  Read selected row
  and store in a row latch
  to restore the read values

  restore row latch into
  selected row
Dynamic RAM Timing

**READ CYCLE**

Address  
Row Address  
Column Addr  

RAS  

CAS  

Load column-address  
output enable DOUT, drive with selected bit  
output disable DOUT  

DOUT  
valid
Dynamic RAM Timing

**WRITE CYCLE**

- Address
- Row Address
- Column Addr

- RAS
- WE
- DOUT: valid data
- CAS

Load column-address
merge Din into selected column of row latch
MEMORY SYSTEM

- Build a 128k x 8 static RAM memory system of RAM chips 64k x 4bit.

A0 - A15 - address lines
Dio0 - Dio3 - input/output tri-state data lines
RW - read/write active low
CS - chip select active low

<table>
<thead>
<tr>
<th>CS</th>
<th>RW</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Read</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Write</td>
</tr>
<tr>
<td>1</td>
<td>x</td>
<td>Dio0-Dio3 in TriState</td>
</tr>
</tbody>
</table>

A0 - A15 - address lines
Dio0 - Dio3 - input/output tri-state data lines
RW - read/write active low
CS - chip select active low
MEMORY SYSTEM 128k x8

A0 - A15
/CS
/WE

64k x4
D0 - D3

MEMORY SYSTEM 64K x 4
MEMORY SYSTEM 128k x8

A0 - A15
/CS
/WE

64k x4
D0 - D3

64k x4
D4 - D7

MEMORY SYSTEM 64K x 8
MEMORY SYSTEM 128k x8

A0 - A15
/CS
/WE
D0 - D3
64k x4
D0 - D3
D4 - D7
64k x4
D4 - D7
64k x4
64k x4
MEMORY SYSTEM 128k x8

A0 - A15
/CS = A16
/WE

64k x4

D0 - D3
D0 - D3

64k x4

D4 - D7

64k x4

D4 - D7

64k x4

64k x4
MEMORY SYSTEM 128k x8

/CS = A16 = 0

A0 - A15

D0 - D3

/WE

64k x4

D0 - D3

1

D4 - D7

64k x4

D4 - D7

64k x4

64k x4

64k x4

12/8/2002
MEMORY SYSTEM 128k x8

A0 - A15

/CS = A16 = 1

/WE

D0 - D3

D0 - D3

0

D4 - D7

64k x4

64k x4

64k x4

64k x4
What have we learnt?

- RAM - Random Access Memory allow to read/write data at a randomly chosen address to the contrary of a floppy disk where the data is stored and accessed in sequence.
- ROM - Read Only Memory allows to read data stored (during programming) at a randomly chosen address.
- EPROM allows to program the contents of the memory and later read it. Programming is much slower than reading.
- Dynamic RAM achieve the largest density and is the prevalent technology for computer memories.
- Memory chips can be organised in memory systems of various depth and width.