

Parallel Structures for class projects and homeworks

Sources

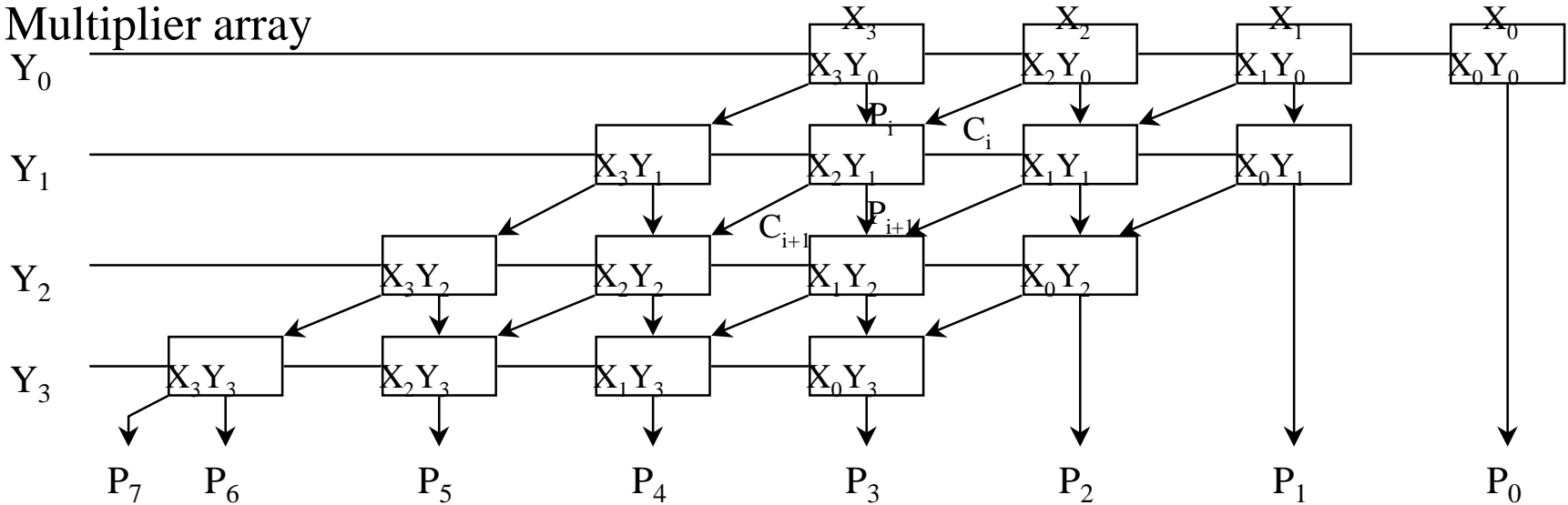
Snyder, Dominic

Parallel Multiplier

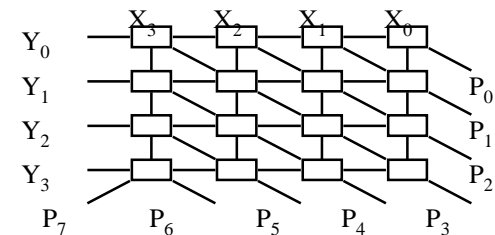
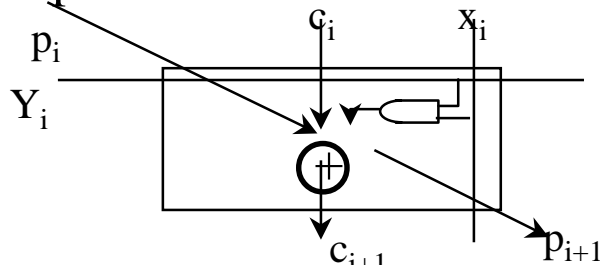
● TABLE 8.2 4-bit multiplier partial products

				X_3	X_2	X_1	X_0	Multiplicand
				Y_3	Y_2	Y_1	Y_0	Multiplier
				X_3Y_0	X_2Y_0	X_1Y_0	X_0Y_0	
			X_3Y_1	X_2Y_1	X_1Y_1	X_0Y_1		
		X_3Y_2	X_2Y_2	X_1Y_2	X_0Y_2			
	X_3Y_3	X_2Y_3	X_1Y_3	X_0Y_3				
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0	Product

● Multiplier array

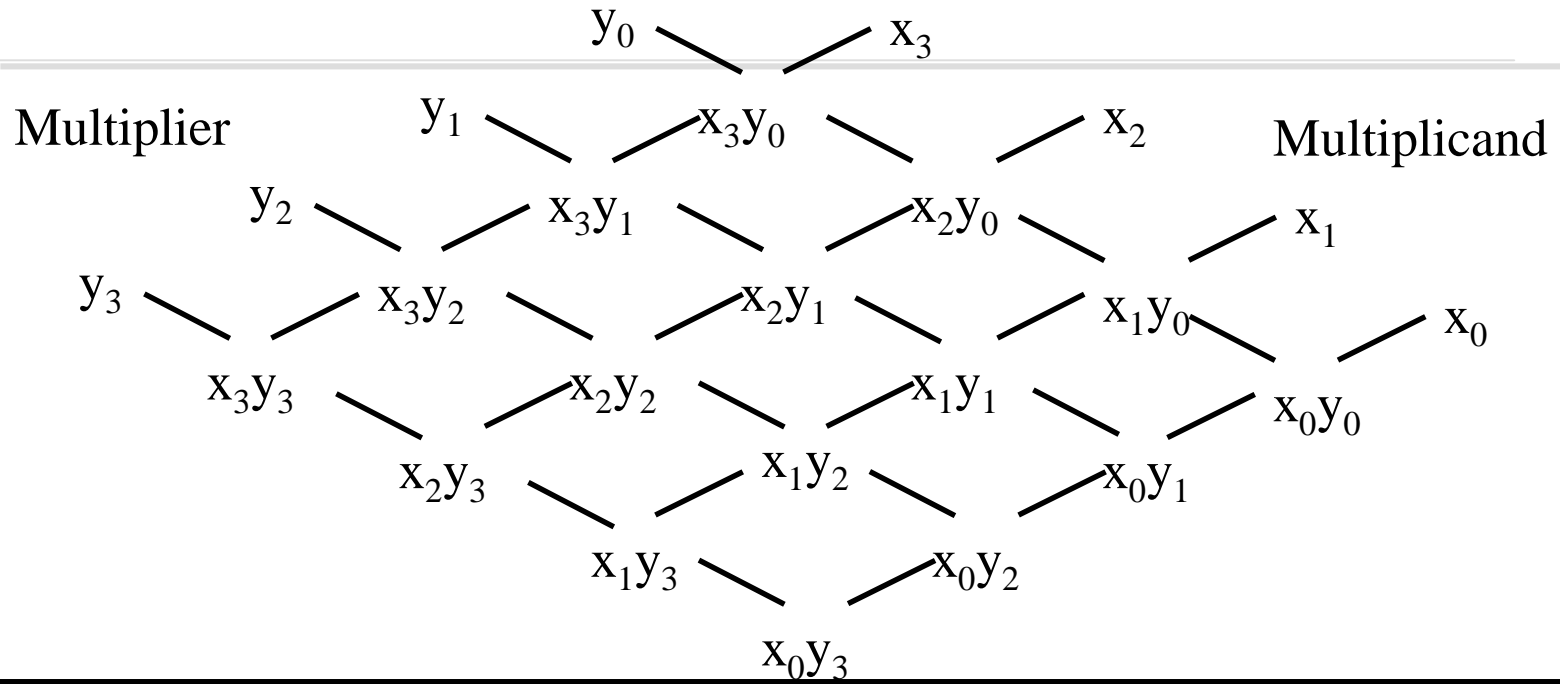


● Parallel multiplier cell



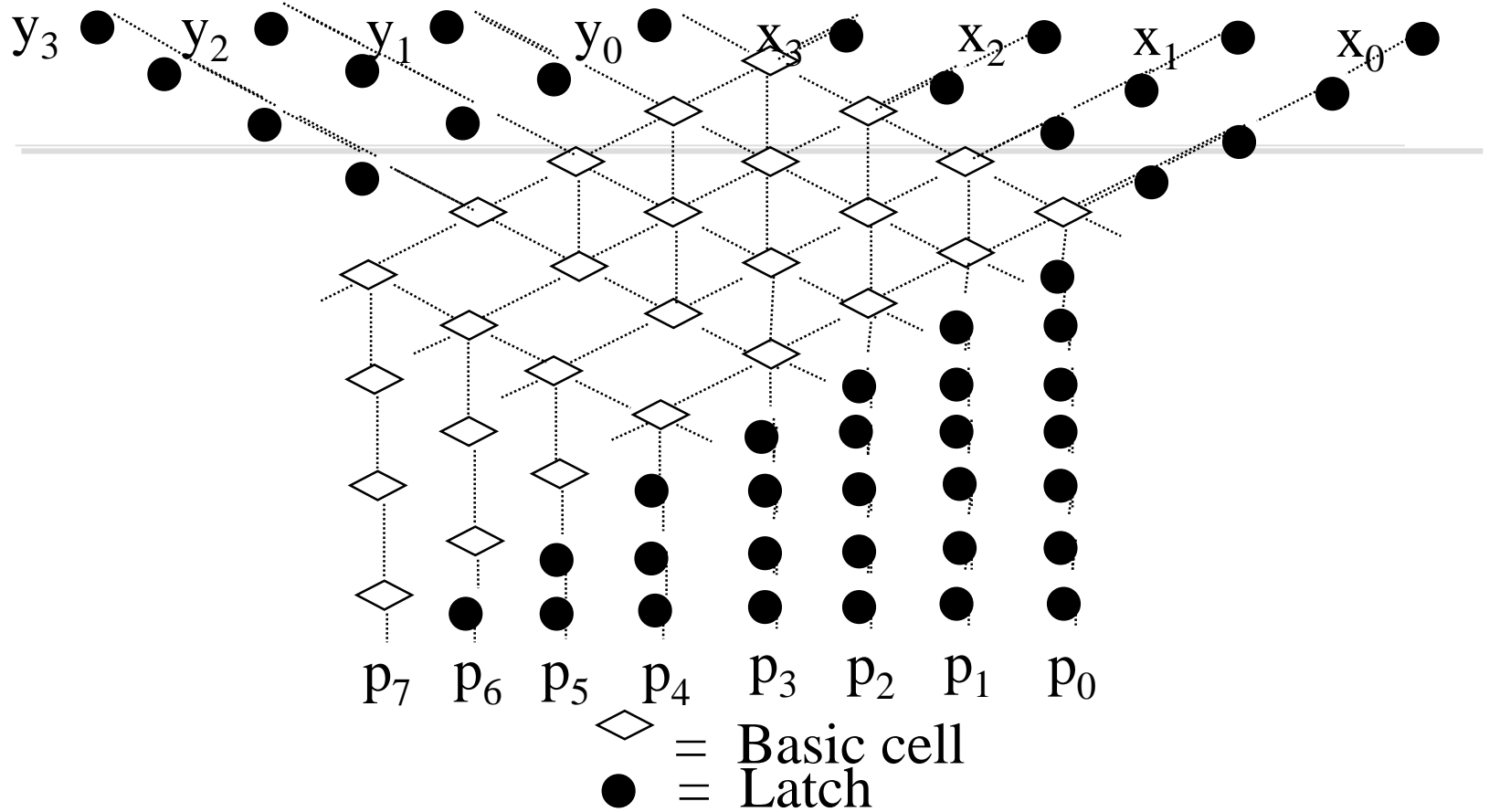
- Speed : parallel > serial/parallel > serial
- Cost : parallel > serial/parallel > serial

Systolic Array Multiplier



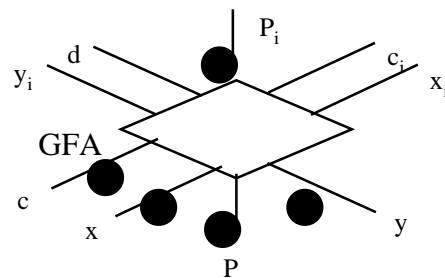
P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0 Product

Multiplier structure



Basic cell

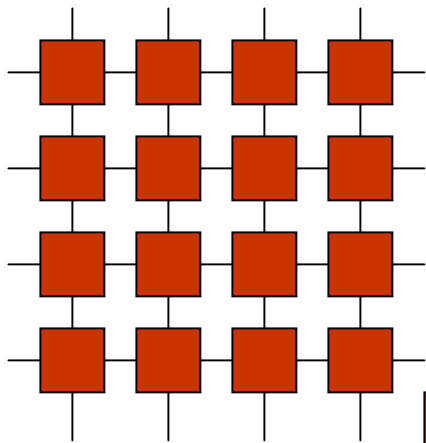
● = Latch
 GFA = Gated full adder



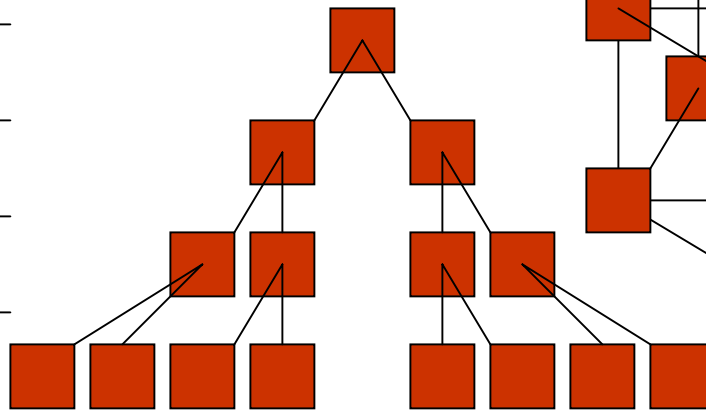
where

- p_i = partial product sum in
- p = partial product sum out
- c_i = carry in
- c = carry out
- d = line required for two's complement operation

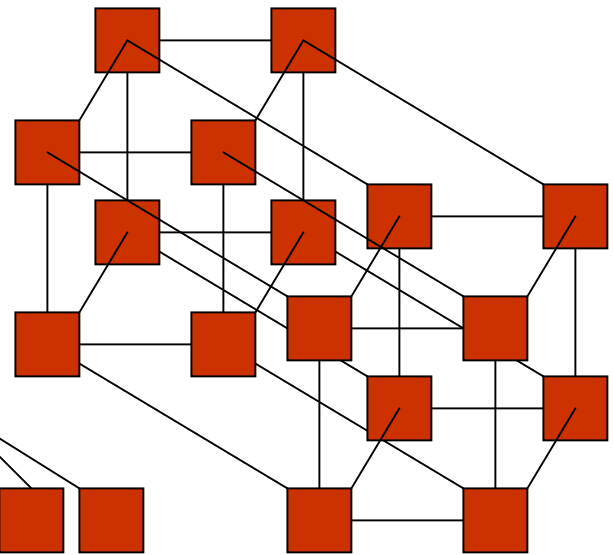
Network and computer structures



OK



Bottlenecks



Not Sparse