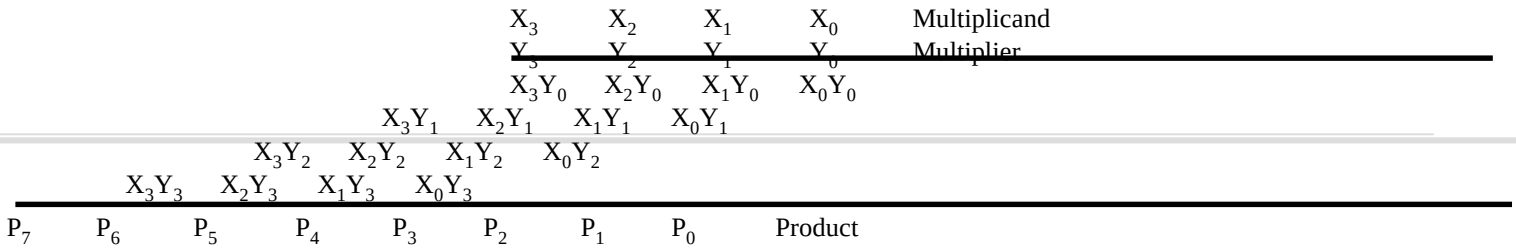
Parallel Structures for class projects and homeworks

Sources

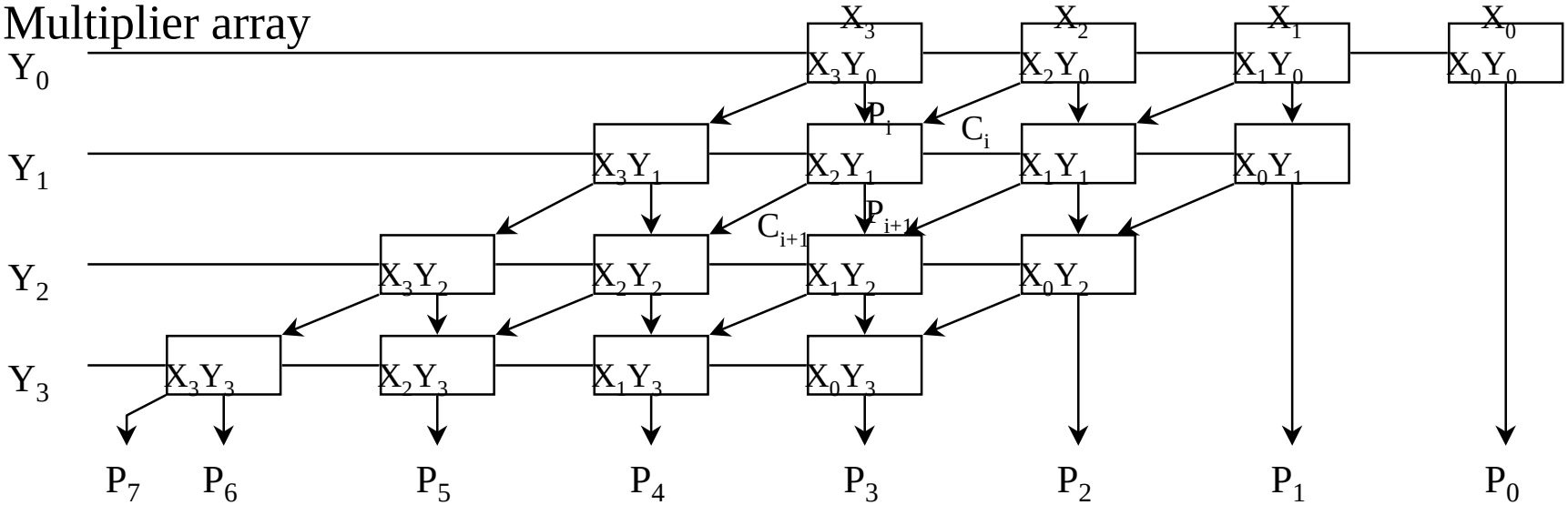
Snyder, Dominic

Parallel Multiplier

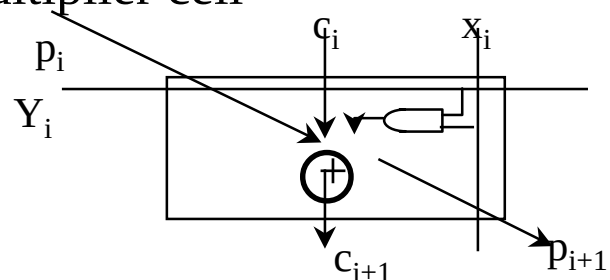
- TABLE 8.2 4-bit multiplier partial products

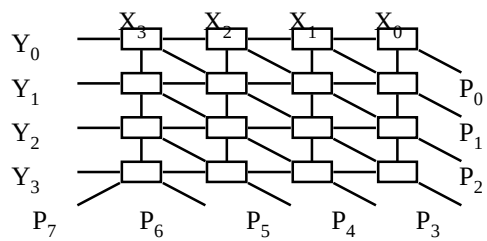


- Multiplier array



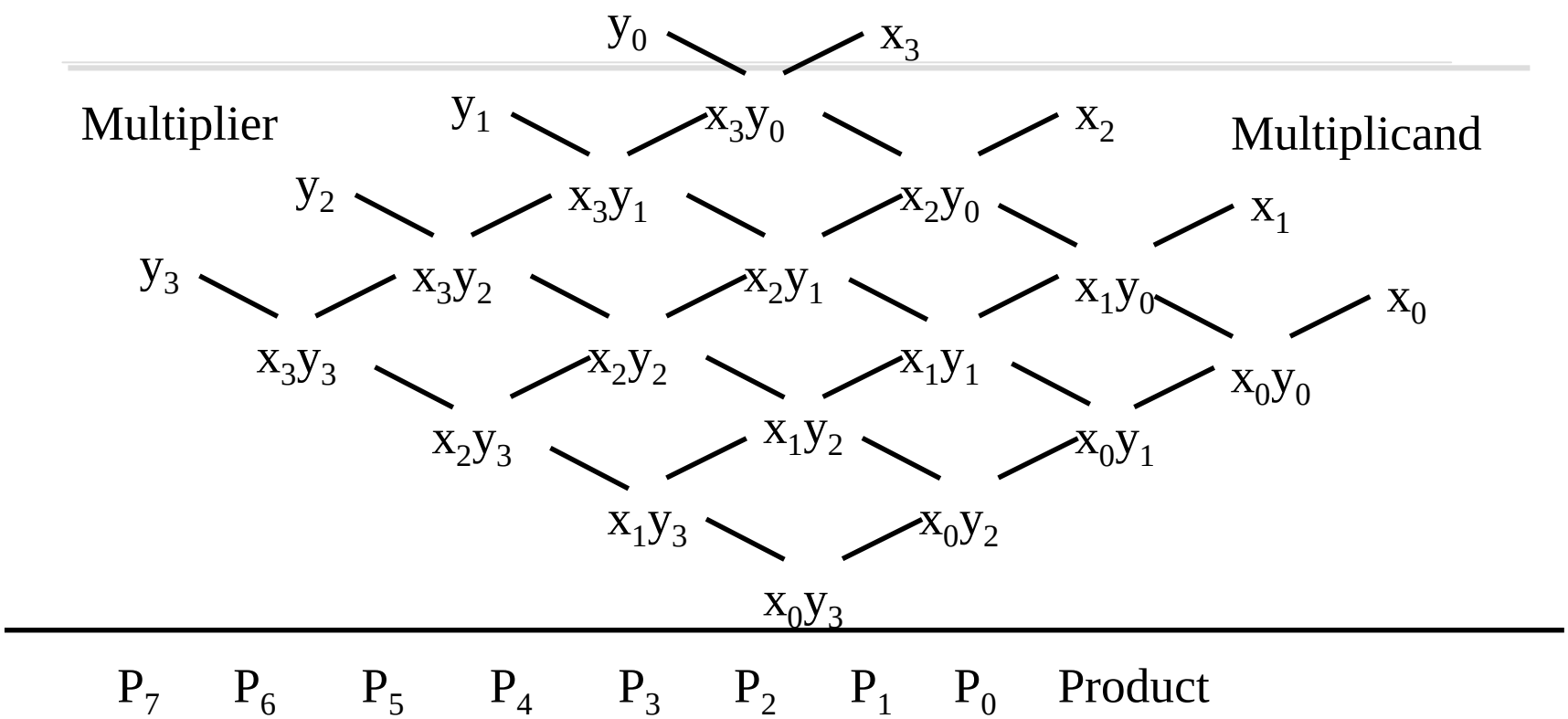
- Parallel multiplier cell



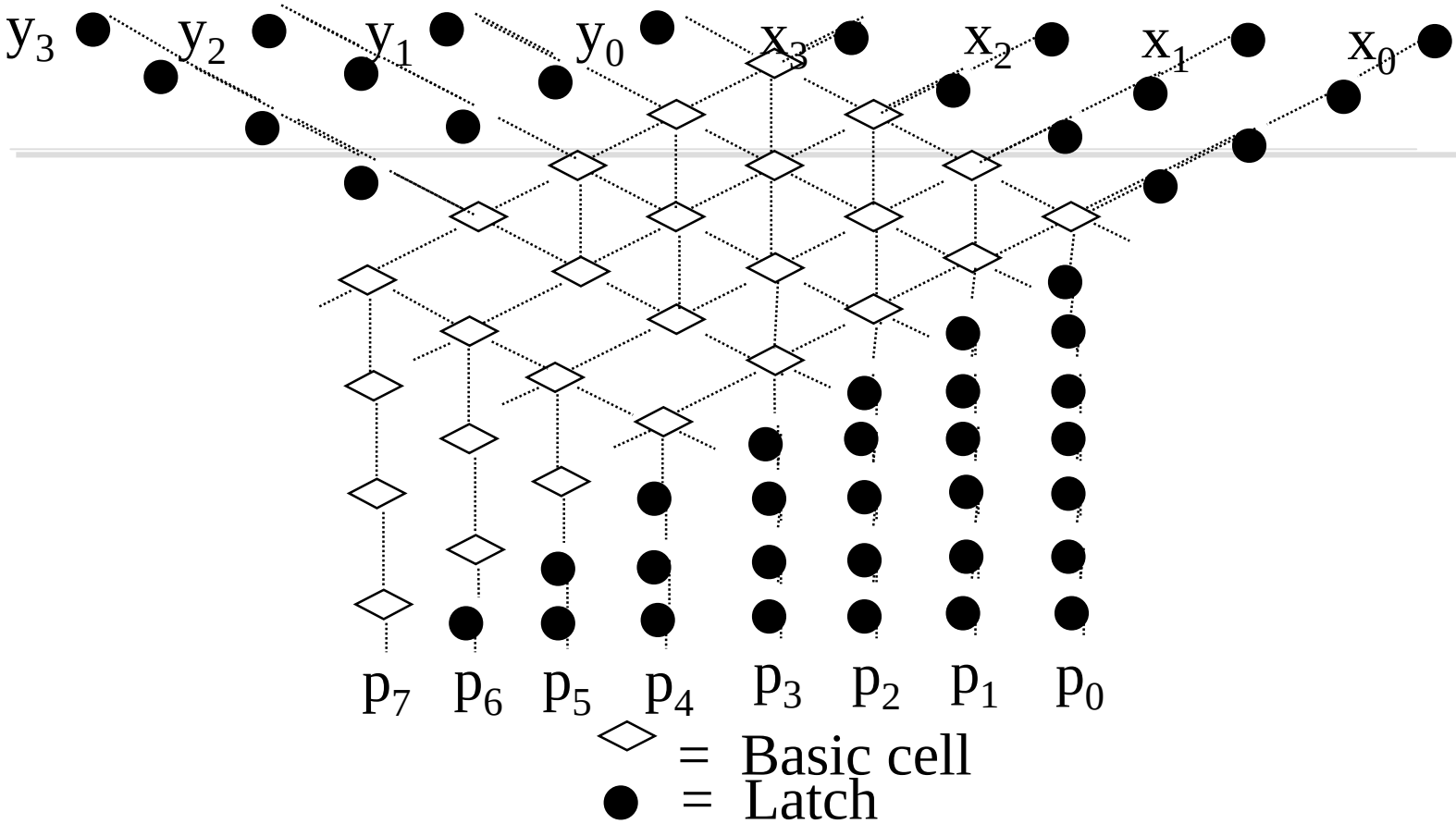


- Speed : parallel > serial/parallel > serial
- Cost : parallel > serial/parallel > serial

Systolic Array Multiplier



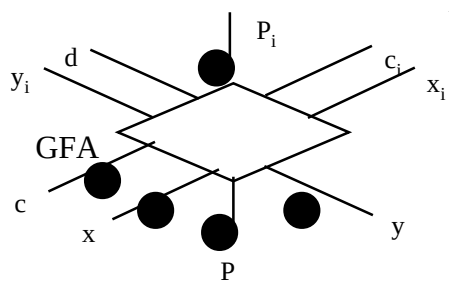
Multiplier structure



Basic cell

● = Latch

GFA = Gated full adder



where

p_i = partial product sum in

p = partial product sum out

c_i = carry in

c = carry out

d = line required for two's complement operation

Network and computer structures