Classification of Parallel Architecture Designs
Level of Parallelism

- **Job level**
  - between jobs
  - between phases of a job

- **Program level**
  - between parts of a program
  - within do-loops
  - between different function invocations

- **Instruct stream level**

- **Instruction level**
  - between phases of instruction execution
  - between instructions

- **Arithmetic and bit level**
  - within ALU units
Job Level

✦ Different job phases
   exp: CPU activities - I/O activities the overlapping may be achieved by programmer visible scheduling of resources

✦ Different jobs

<table>
<thead>
<tr>
<th>OS</th>
<th>T1</th>
<th>T2</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td>job 1</td>
<td>job 2</td>
</tr>
<tr>
<td>I/O</td>
<td>job 2</td>
<td>job 1</td>
</tr>
</tbody>
</table>

✦ Architecture requirement:
   a balanced set of replicated resources in a computer installation.
CPU/I/O Overlapping

Common memory

Computational processor (stage 1)

Input/output processor (stage 2)

Stage

1

Task 1

Task 2

Task 1

Task 3 ...

2

Task 2

Task 1

Task 3

Task1

Time

idle time

CPU/I/O Overlapping
Program Level Parallelism

- Different code sections:
  - diff. procedure/functions
  - diff. code blocks

- Different iterations for the same loop

- Data-dependencies and program partitioning
Instruction Level Parallelism (ILP)

- Between instructions
  - parallel execution of different instructions - spatial
  - key: dependency between instructions
- Between phases of instructions
  - overlapping different suboperations - pipelining
  - pipelining of a suboperations itself, e.g. ALU pipelining
Overlay vs. Pipeline

Pipeline:
- tightly coupled subfunctions
- fixed basic stage time
- independent basic function evaluation

Overlap
- loosely coupled subfunctions
- variable basic stage time
- dependency between function evaluation
Principles of Pipelining

Hardware design method: RT

Time
Pipelining of an Instruction Execution

- Instruction Fetch
- Instruction Decode
- Execute
- Memory Op
- Register Update
number \( i \) corresponds to instruction \( i \)
Hazards

✦ Any conditions within the pipelined system that disrupt, delay or prevent smooth flow of tasks through the pipelines.

✦ The detection and resolution of hazards constitute a major aspect of pipeline design

✦ Types of hazards
Flynn (72)

- Classification of parallel architecture is not based on the structure of the machine, but based on how the machine relates its instructions (streams) to the data (stream) being processed.

A stream:
- a sequence of items
- being executed or operated on by a processor.
SISD + ILP

SIMD + Vector

MISD

MIMD

ILP gains increasing attention!
S I S D

- for practical purpose: only one processor is useful
- pipelining may or may not be used,

often called as serial scalar computer
SIMD

- (single inst stream/multiple data stream)
- single processor
- vector operations
  - one v-op includes many ops on a data stream
- both pipelined processing or array of processors are possible
- Example:
  CRAY -1
  ILLIAC-IV
  ICL DAP
(a) SISD uniprocessor architecture

(b) SIMD architecture (with distributed memory)

(c) MIMD architecture (with shared memory)

Captions:
- \( C \) = Control Unit
- \( P\)U = Processing Unit
- \( M\)U = Memory Unit
- \( I\) = Instruction Stream
- \( D\)S = Data Stream
- \( P\)E = Processing Element
- \( L\)M = Local Memory
Problems of Flynn’s Scheme

✧ too broad

✧ everything in SIMD: vector machines?

✧ MISD?

✧ Relation with Parallel Programming models?
MISD architecture (the systolic array)

Captions:
CU = Control Unit
PU = Processing Unit
MU = Memory Unit
IS = Instruction Stream
DS = Data Stream
PE = Processing Element
LM = Local Memory
The broad subdivisions in computer architecture

Computers

Single I stream
- Single unpipelined E unit
  - Serial unicompurers
- pipelined or multiple E units
  - Parallel unicompurers

Multiple I stream

MIMD
Parallel unicomputers based on functional parallelism and pipelining
ILP Architectures

✦ Multiple inst/op issuing + deep-pipelining
✦ Superscalar
  – Multiple inst/cycle (Power PC, MIPS10000, Intel Pentium)
✦ VLIW
  – Multiple op in one inst/cycle
  – ESL/polycyclic or Cydra5
  – Multiflow
  – Intel iA-64 architecture?
✦ Superpipelined
  – MIPS 4000/8000
  – DEC Alpha (earlier versions)
✦ Decoupled Arch
✦ Multithreaded Arch
  – EARTH/MTA
  – Multiscalar [Sohi]
  – etc.
Sources

Guang R. Gao