A COMPARISON OF LOGICAL EFFICIENCY OF REVERSIBLE AND CONVENTIONAL GATES

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ABSTRACT
In contrast to conventional gates, reversible logic gates have the same number of inputs and ouputs, each of their output function is equal to 1 for exactly half its input assignments and their fanout is always equal to 1. It is interesting to compare compositional properties of reversible and conventional gates. We present such a comparison based on an exhaustive study of logic circuits.

INTRODUCTION
Reversible computing was founded when on the basis of thermodynamics of information processing it was shown that conventional irreversible circuits unavoidably generate heat because of losses of information during the computation (see, e.g. [1]). It was also indicated that different physical phenomena can be exploited to construct reversible circuits avoiding the above mentioned energy losses. One of the most attractive new perspectives opened in this way is the possibility to build almost energy lossless ultra-small and ultra-fast quantum computers.

A circuit is said to be reversible if there is a one-to-one correspondence between the inputs and the outputs (i.e. if there is a distinct output assignment for each distinct input assignment). Thus, the number of outputs in a reversible gate or circuit has to be the same as the number of inputs. Output functions of binary reversible logic gates equal to 1 for exactly half their input assignments (such functions are called balanced. Logic design of reversible circuits is quite different from designing conventional irreversible logic circuits. In reversible circuits we have to use at least one gate to duplicate a signal. Moreover, for realization of nonbalanced Boolean functions by a reversible circuit it is necessary to apply constant signals to some inputs of the circuit (in conventional circuits with complex gates using constant signals is useful but not necessary). Let us call a gate (circuit) with n inputs and m outputs (n,m)-gate (-circuit). It was shown [9] that a universal reversible gate should have at least three inputs and outputs and several such gates were proposed [2-10,13-14]. However, it would be interesting to know which (3,3)-gates are most efficient, as well as to consider relative efficiency of reversible (3,3)-gates in comparison with (3,1)-gates. In the paper the results of an exhaustive study of using reversible gates to design (n,n)-circuits implementing Boolean functions are described. The number of functions realizable in such circuits is used to evaluate approximate efficiency of gates.

BASIC NOTIONS
Definition 1. A Boolean function $f(x_1,x_2,...,x_n)$ is a *subfunction* (also the terms *cofactor, restriction* and *reduced function* are used) of a function $g(x_1,x_2,...,x_n)$ if there exists such a replacement of some variables of g by constants 0 or 1 that $f=g$ after this replacement.

Definition 2. Two Boolean functions $f(x_1,x_2,...,x_n)$ and $g(x_1,x_2,...,x_n)$ are *permutationally-equivalent* (in short: *p-equivalent*) if there exists a permutation p of $x_1,x_2,...,x_n$ such that

$$f(p(x_1), p(x_2),..., p(x_n)) = p(x_1,x_2,...,x_n).$$

The above defined relation is an equivalence relation and we shall call its equivalence classes by *p-classes*. For example, the functions x_1+x_2, x_1+x_3, x_2+x_3 belong to the same p-class.

Below we will use a short notation of Boolean functions and gates. As we are going to present only results concerning 3-variable functions the notation is defined for this case. Let $0\le i\le 7$, $a_i,b_i\in\{0,1\}$, $i=4b_1+2b_2,+b_3$ and $a_i=f(b_1,b_2,b_3)$. Then a function $f(x_1,x_2,x_3)$ is represented uniquely by an 8-bit binary number $a_7\ a_6\ a_5\ a_4\ \ a_3\ \ a_2\ a_1\ a_0$.. To obtain a shorter notation the halves of this sequence,

namely $a_7\ a_6\ a_5\ a_4$ and $a_3\ a_2\ a_1\ a_0$, are treated as hexadecimal digits in the following way: 0000=**0**, 0001=**1**, ... , 1001=**9**, 1010=**A**, 1011=**B**, 1100=**C**, 1101=**D**, 1110=**E**, 1111=**F** (2-variable subfunctions are represented by single hexagonal digits). Thus, the 3-variable function AND will be denoted as **80** and the 3-variable function OR as **FE**. Similarly, (3,3)-gates will be denoted as 6-digit hexagonal numbers, where the first, the second and the third pair of digits will describe respectively the first, the second and the third output function.

Example 1. The truth table below define a reversible (3,3)-gate (note that there are 8!=43200 such gates corresponding to all permutations of 8 assignments). Capital letters *A*, *B* and *C* denote input signals and *P*, *Q* and *R* denote output signals. The short notation of this gate is **4759CA**.

A	*B*	*C*	*P*	*Q*	*R*
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	0
0	1	1	0	1	1
1	0	0	0	1	0
1	0	1	0	0	0
1	1	0	1	1	1
1	1	1	0	0	1

Definition 3. *A subfunction set count* S_G of a reversible (3,3)-gate G is the cardinality of the set of all subfunction p-classes of its three output functions, where only replacements of exactly one variable are considereded and the constant subfunction p-classes **0** and **F** are not taken into account.

The notion of a subfunction set is important from the practical point of view because a gate can implement all functions belonging to its subfunction p-classes. We do not count the constant functions as we assume that to obtain constant signals no gate is needed. On the other hand, implementation of 1-variable functions can be useful because fanout is not possible in reversible circuits without using a gate.

Example 2. For the gate defined in the example 1 the table below gives possible replacements of variables by constants leading to obtaining representatives of all 14 p-classes of nonconstant 2-variable functions.

p-class	Output function	Replacement
1	P=	*C*=1
2	Q	*C*=1
3	P	*B*=0
4	P	*A*=1
5	P	*B*=1
6	Q	*B*=1
7	P	*A*=0
8	R	*C*=0
9	Q	*A*=0
A	R	*A*=0
B	P	*C*=0
C	R	*A*=1
D	Q	*C*=0
E	R	*B*=1

An interesting approach to using complex gates in logic circuits consists in construction of the so-called universal logic modules (although for a long time this field had had no direct impact on practice it was revived recently in the context of constructing area efficient FPGAs). A *(m,1)*-gate is *universal in n arguments* (*is ULM-n*) if every Boolean function $f(x_1,x_2,...,x_n)$ belongs to one of the gate subfunction p-classes. We have established that **there are 408 ULM-2 reversible (3,3)-gates (68 p-classes)**. One of them was given in Example 1.

EFFICIENCY OF LOGIC GATES

In the advent of using integrated circuits, it was established that the (3,1)-building block WOS implementing the function

$$f_{WOS} = 1 \oplus x_1 \oplus x_3 \oplus x_1 x_2$$

where $\oplus$ denote XOR operation (it belongs to the p-class containing **2D, 39, 4B, 59, 63, 65**), can be used to realize any function of 3 variables with no more than three gates [12] and with no more than two levels [11] (in the lattter case sometimes four gates are needed).

Recently two papers [15,16] were published on studies of cascade connections of reversible (3,3)-gates. As the number of arbitrary two-gate circuits is much greater than the number of cascade circuits and cascades implement only balanced functions we think that considering arbitrary two-gate circuits is a better way to measure efficiency of gates. Although magnetic, Josephson junction, optic, optoelectronic and quantum reversible gates was considered in many papers the only practical circuits built so far are electronic ones. This is why we made a different assumption concerning interconnection of gates than the authors of the above mentioned papers: we allow permutation of wires (not allowed in quantum gates) but we do not allow inversions (e.g. permitted when double wires are used).

The following relatively simple reversible (3,3)-gates have been proposed in the literature (they are listed in the chronological order):

G1 – Fredkin gate **F0CAAC** [9,17]
G2 – Feynman gate **F0CC6A** [8]
G3 – Peres gate **66CC78** [13]
G4 – Margolus gate **CAB8E4** [10]
G5, G6, G7, G8, G9 – De Vos gates, respectively **714D2B**, **8EB2D4**, **B4C69A** **D29CA6**, **ACE2D8** [2-6].

EXPERIMENTAL RESULTS

We have ran a program constructing all two-gate circuits made of identical reversible (3,3)-gates:
- (3,3)-circuits,
- (4,4)-circuits with one additional input to which only one specific constant signal was applied,
- (5,5)-circuit with two additional inputs to which two identical constant signals were applied,
- as in the previous case but with different constant signals.

Maximal numbers of realizable 3-variable functions realized in the above described cases are 60, 237, 252 and 256, respectively. As the last case is more interesting than the others (because all 3-variable functions are realizable) the results presented below correspond to this case. After checking all 8! = 40320 (3,3)-gates we have found that most of (3,3)-gates realize all or almost all 3-variable functions in two-gate circuits. In the table below the first column gives an interval of the numbers of the realized functions and the second column gives the number of gates capable to realize these numbers of functions:

Number of functions	Number of gates
1-16	1344
17-32	0
33-48	0
49-64	36
65-80	0
81-96	372
97-112	324
113-128	360
129-144	48
145-160	744
161-176	1128
177-192	1764
193-208	4014
209-224	5418
225-240	9252
241-256	15516
	Total = 40,320

A gate is *two-level universal in n arguments* if using this gate it is possible to implement every function of *n* variables with a two-level circuit. Among reversible (3,3)-gates there are 288 **two-level universal in 3 arguments**. Below we give the list of the representatives of 24 out of 48 p-classes with the single function score equal to 256 and with the best scores for pairs and triples. Note that in all of the below listed gates one output function belongs to the p-class containing f_{WOS}.

Gate	Single functions	Function pairs	Function triples
2E63A9	256	6580	44841
5972E1	256	6561	44499
2D6AA3	256	6527	45513
2D5CC9	256	6523	46035
3A4BA9	256	6517	44370
6378D1	256	6508	44406
3974E1	256	6505	44163
596C8D	256	6458	45807
396A8B	256	6458	44988
6578B1	256	6440	44070
4B6CC5	256	6365	42741
4E65C9	256	6292	41583
1E5972	256	6374	43758
2D365C	256	6341	44397
364E65	256	6311	42981
2E5663	256	6310	43701
3A4B56	256	6271	43278
1E3974	256	6167	42678
2D95A3	256	6135	42819
6387D1	256	6114	43095
4B93C5	256	6114	42384
598D93	256	6084	43710
6587B1	256	6057	42744
398B95	256	5922	42027

For comparison we present below the numbers of functions realized by the gates **G1**-**G9**:

G1	**G2**	**G3**	**G4**	**G5**	**G6**	**G7**	**G8**	**G9**
152	61	88	152	82	93	168	168	152

As we can see using any of the 24 gates listed in the previous table would lead in most cases to smaller circuits.

Now let us compare the average gate count when realizing all 256 3-variable functions with the following building blocks:

(3,1)-**NAND** (or **NOR**)	4.41
(3,1)-**WOS**	2.04
best reversible (3,3)-gate	1.75.

Thus, the efficiency of the most flexible reversible (3,3)-gates is better than the best convential (3,1)-gates despite of the additional constraints imposed on them such as restriction on their output functions to belong to the class of balanced functions and the fanout equal to 1.

Similar calculations for irreversible (3,3)-gates and for broader class of circuits are in progress and will be finished soon (their results can be reported at the IWLS'2000).

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