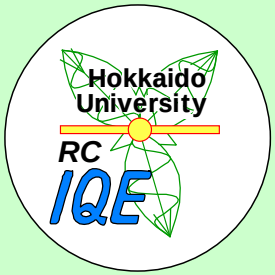
ECS 2001 Joint Intenational Meeting, San Francisco Sept. 2-7, 2001
Sixth International Symposium on Quantum Confinement

Quantum Devices and Integrated Circuits Based on Quantum Confinement in III-V Nanowire Networks Controlled by Nano-Schottky Gates



Hideki Hasegawa

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Graduate School of Electronics and Information Engineering
Hokkaido University, Japan

Outline

1. *Introduction*
2. *Hexagonal BDD Quantum Circuits*
3. *GaAs-Based Quantum BDD Node Devices and Circuits*
   - *Novel nanometer-scale Schottky gates*
   - *GaAs-based quantum BDD node devices*
   - *Integration of BDD node devices on hexagonal nanowire networks*
4. *Toward Room Temperature Operation and High Density Integration*
   - *Formation of InP-based high density hexagonal nanowire networks*
   - *Surface related key issue*
5. *Conclusion*

Collaborators

RCIQE staff

Dr. S. Kasai, Dr. C. Jiang and Dr. T. Sato

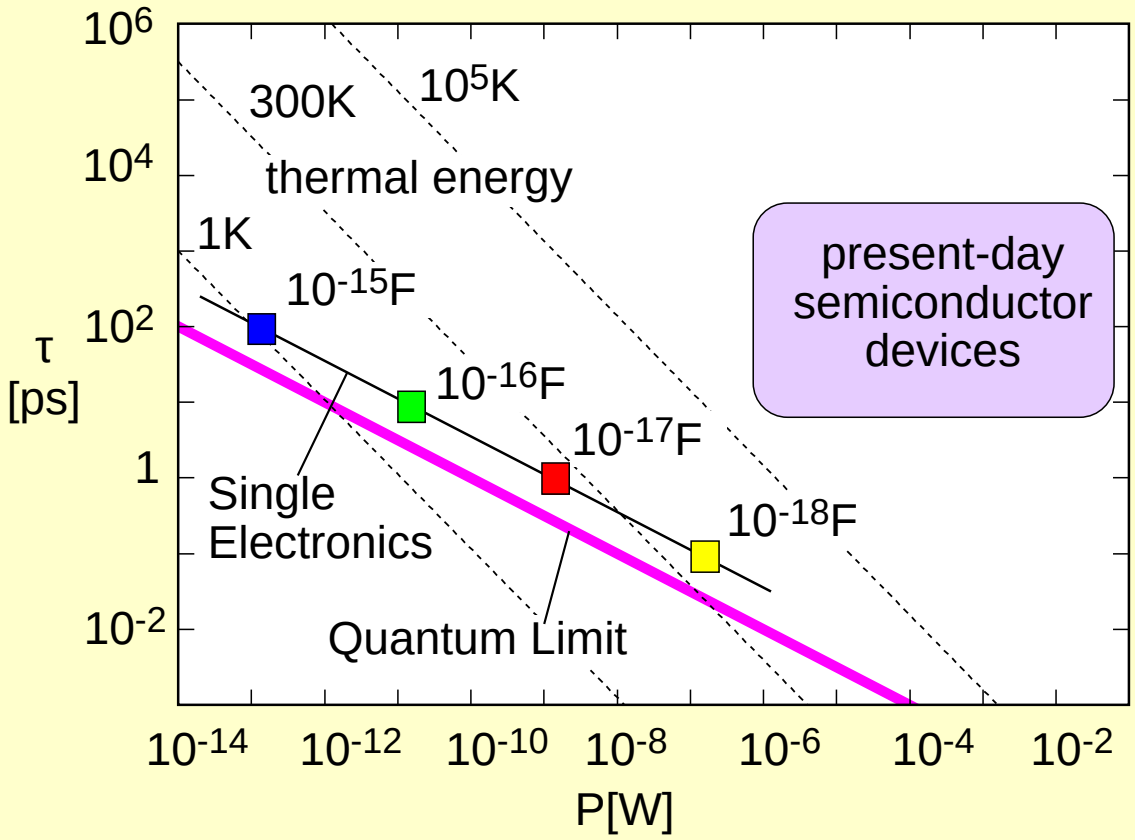
Students

T. Muranaka, A. Ito and M. Yumoto

Speed, Delay-Power Product of Quantum Devices

$$\tau = \frac{C}{G} \qquad G \approx G_0 \equiv \frac{2e^2}{h}$$

J.E.Mooij, 1993 SSDM Ext. Abs. 339



Scale-down limit of
Si CMOS LSIs

Research on
Semiconductor Nanostructure

Growing demands on
Information Technology (IT)

Nanotechnology in wide area
~ chemistry, biology, etc.

Semiconductor Nanoelectronics based on Quantum Device and Circuit

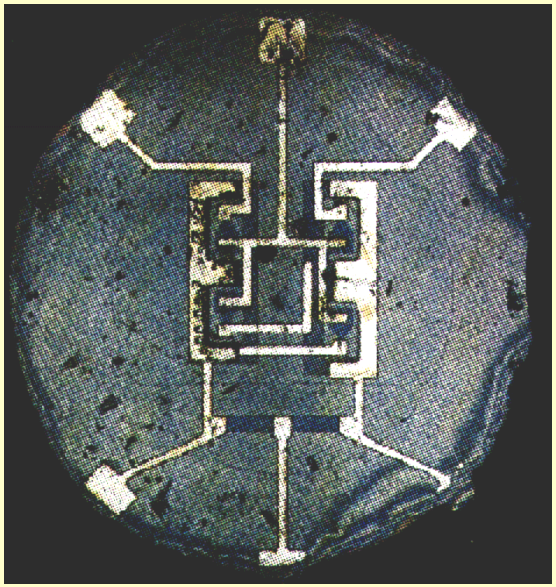
- delay-power product near quantum limit
- small-size and high-density
- nano-sensing, nano-control

But, How to ? So far no realistic approach.

High Density Integration ?

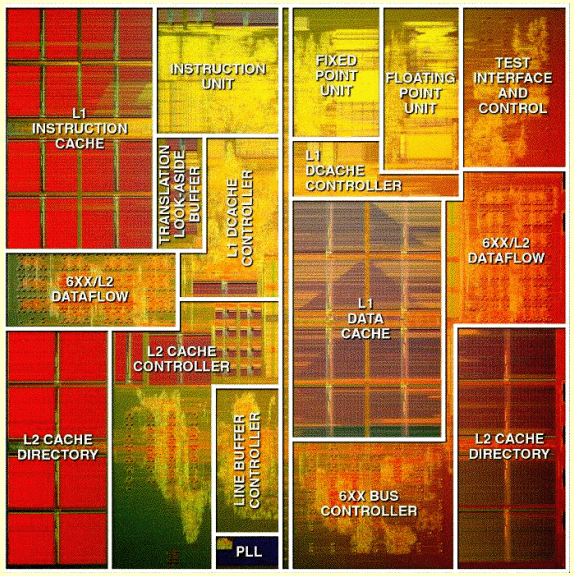
Semi-classical devices

First Monolithic Integrated Circuit in the World (Noyce, 1959)



300μm rule

Current Microprocessor (2001)



IBM PowerPC

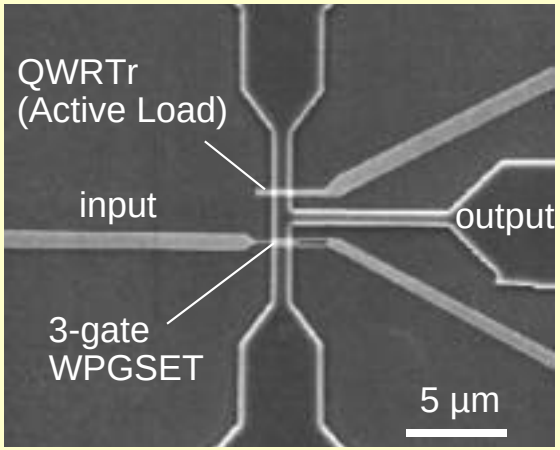
64-bit
0.18μm rule
700MHz
1.4mm x 1.4mm
SOI technology

Discrete quantum devices ➡ **How to make QLSIs ?**

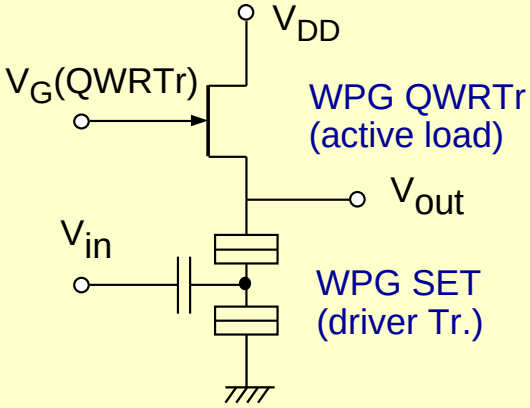
Example of Quantum Logic Circuits

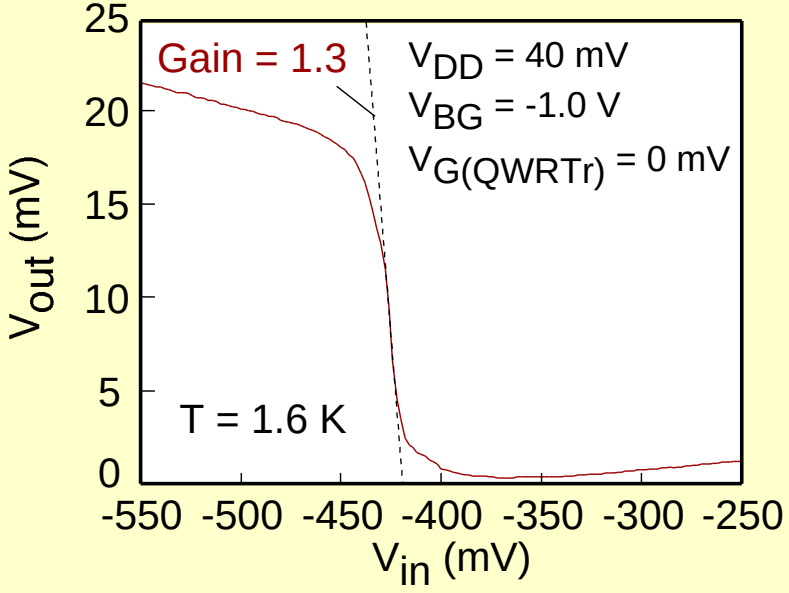
QWRTr-load SET inverter

(S. Kasai and H. Hasegawa presented at DRC 2000)



W = 440 nm
SET: L_G = 50 nm, d_f = 200 nm
QWRTr: L_G = 300 nm





small delay•power product
but
- *low gain*
- *voltage mismatch*
- *poor V_{th} control*
- *poor drivability*
- *low temperature*

Novel Approach for III-V QLSI

Hokkaido University RC IQE

1. Digital Processing Architecture

Binary Decision Diagram (BDD) logic architecture

2. Nanostucture

Hexagonal nanowire networks by
GaAs etched nanowires and
InGaAs nanowires by Selective MBE

3. Nanoscale Gate Technology

Schottky in-plane gate (IPG) and wrap gate (WPG)

4. Surface and Interface Control

Nano-Schottky interface
Interface control layer (ICL)-based passivation

5. Device

BDD node devices using gate-control
quantum wire (QWR) and quantum dot (QD)

Digital Logic Architecture

Digital processing
(operations on digital functions)

Implementation of digital functions

Representation

Boolean Equation | **Truth Table** | **Binary Decision Diagram (BDD)** | etc.

Implementation

Binary Logic Gate → **Transistor Switch**

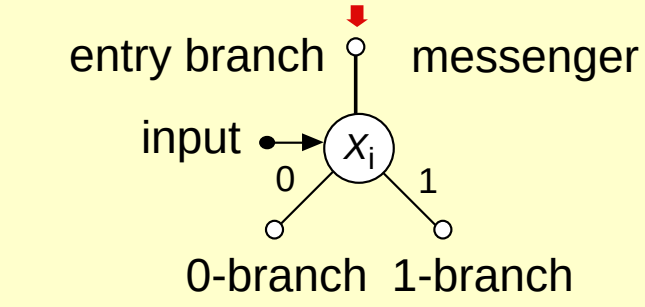
Look-Up Table using Memory → **ROM device**

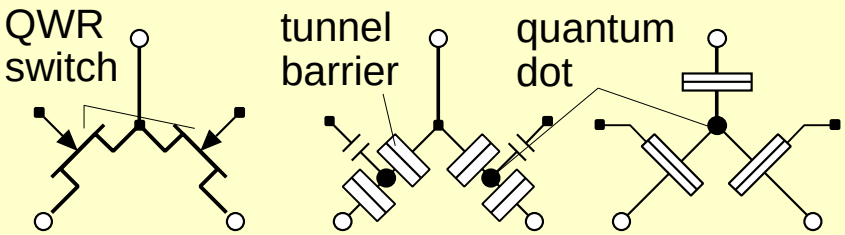
BDD Device

Hexagonal BDD QLSI Approach

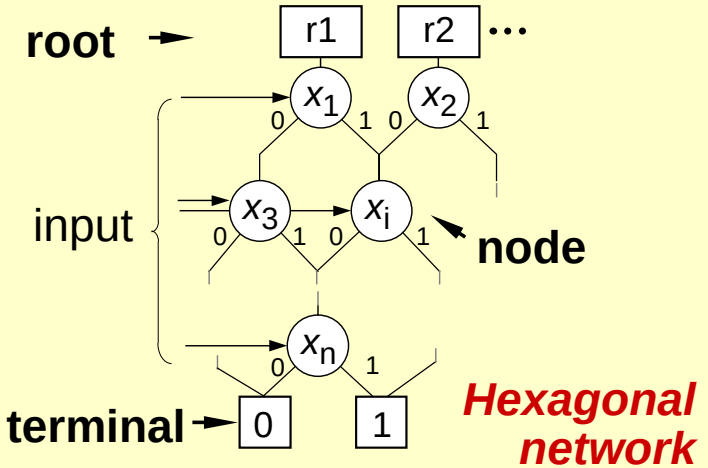
Hokkaido University RC IQE

BDD node device



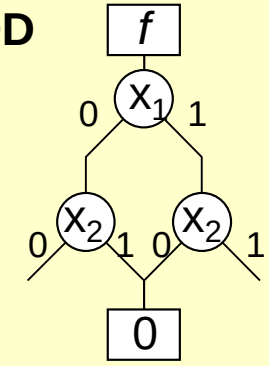


BDD logic architecture



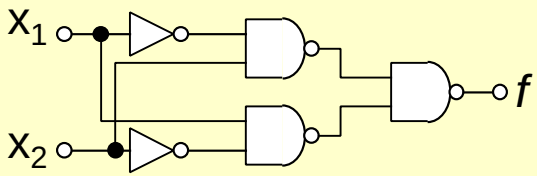
Example: Exclusive OR Logic Function

BDD



3 devices

Boolean Logic Gate



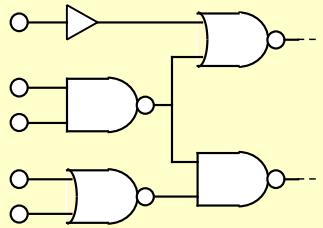
5 gates, 16 Trs

Features of Our Approach

- **BDD is suited to quantum devices**

  No direct input-output connection is required
  - *no precise voltage matching*
  - *no large voltage gain*
  - *no large current drivability*
  - *no large fan-in and fan-out*

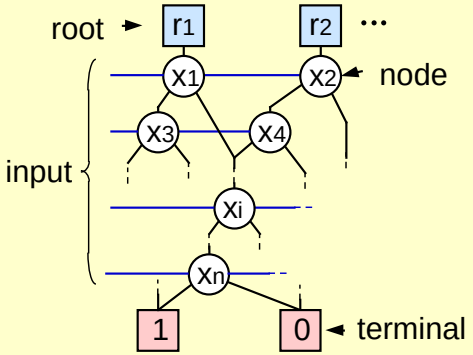
Conventional Logic Gate Architecture



- **Ultra-low delay-power product near the quantum limit**

- **High density integration**
  - *hexagonal closely packed nanowire network*
  - *free from contact problem*
  - *reduced device count*

Hexagonal quantum BDD



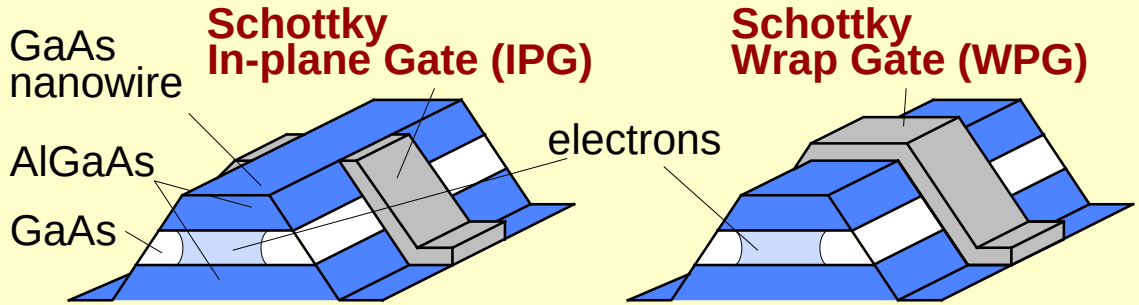
- **The circuit itself works at room temperature at sacrifice of delay-power product**

  IPG/WPG QWRTr-based BDD devices act as classical path switching devices even under non-quantum conditions.

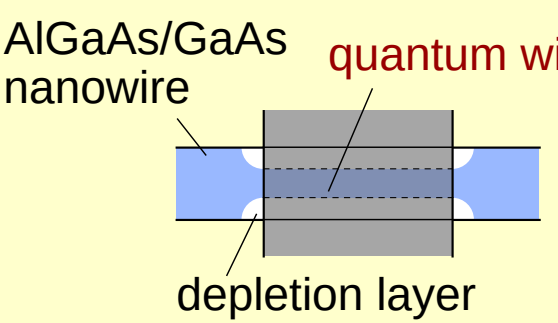
single electron regime → few electron regime → many electron classical regime

Basic Schottky Gate Structure

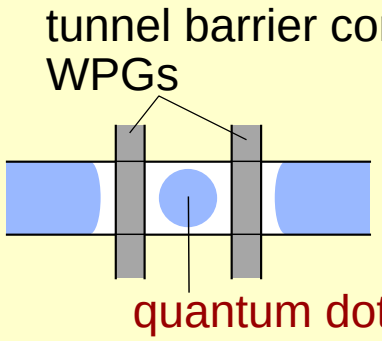
Schottky In-Plane Gate (IPG) and Schottky Wrap Gate (WPG) control of AlGaAs/GaAs etched nanowires



- lateral structure → suitable for planar integration
- stronger confinement, size ~ smaller → high temperature operation



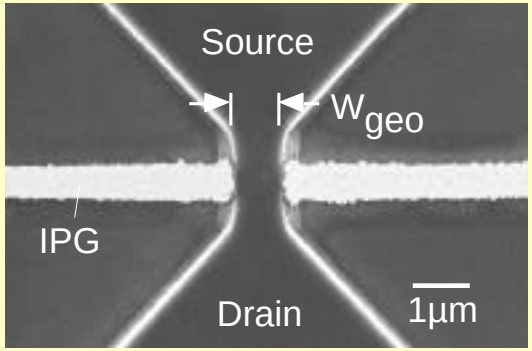
WPG quantum wire transistor (QWRTr)



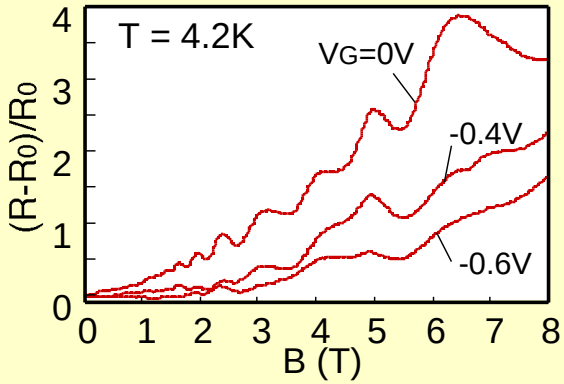
2-gate WPG single electron transistor (SET)

Gate Control Characteristics of IPG/WPG Structures

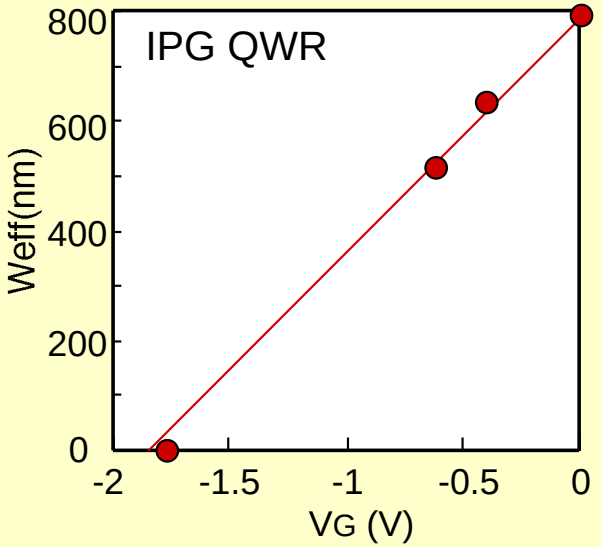
IPG QWRTr



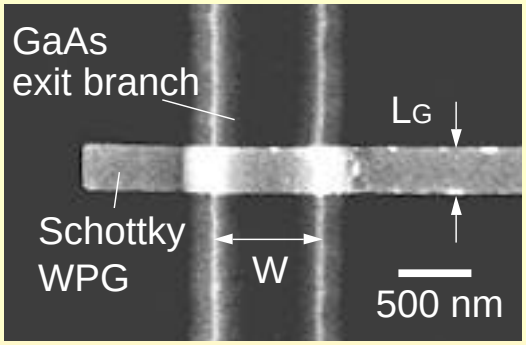
SdH oscillation

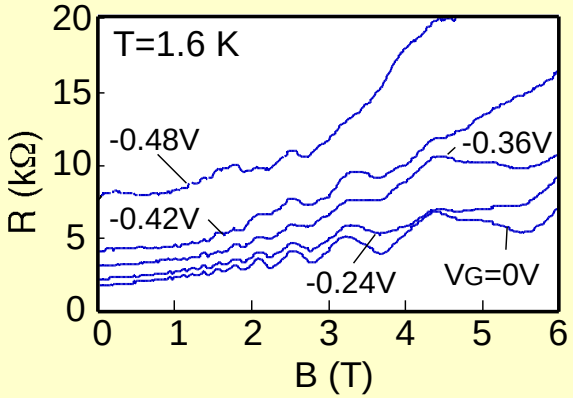


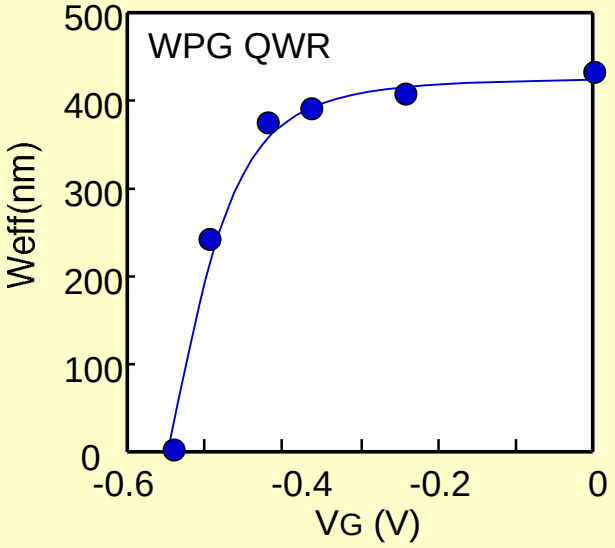
Controlof W_{eff}



WPG QWRTr



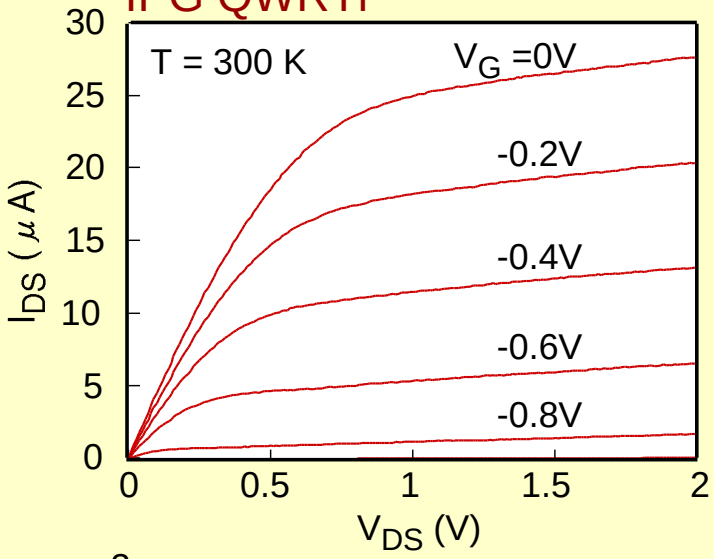


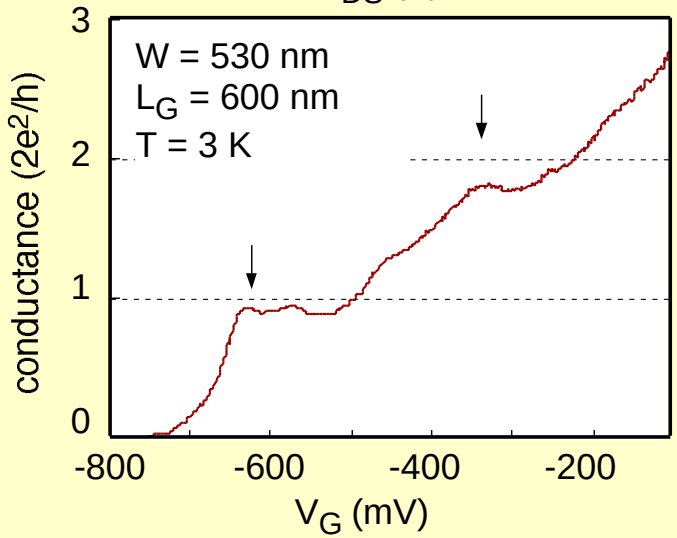


I-V Characteristics of IPG/WPG QWRTrs

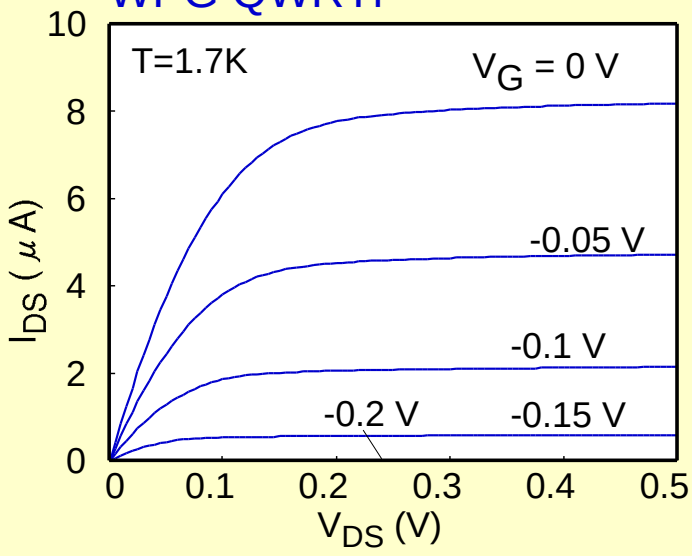
AlGaAs/GaAs etched nanowire

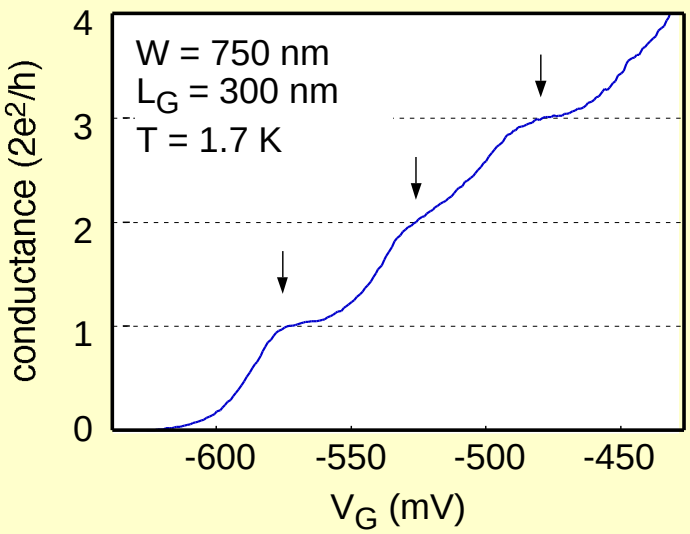
IPG QWRTr





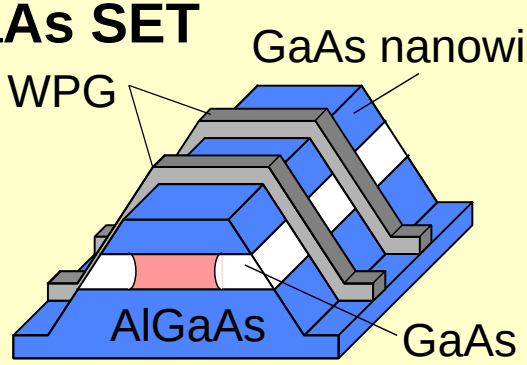
WPG QWRTr





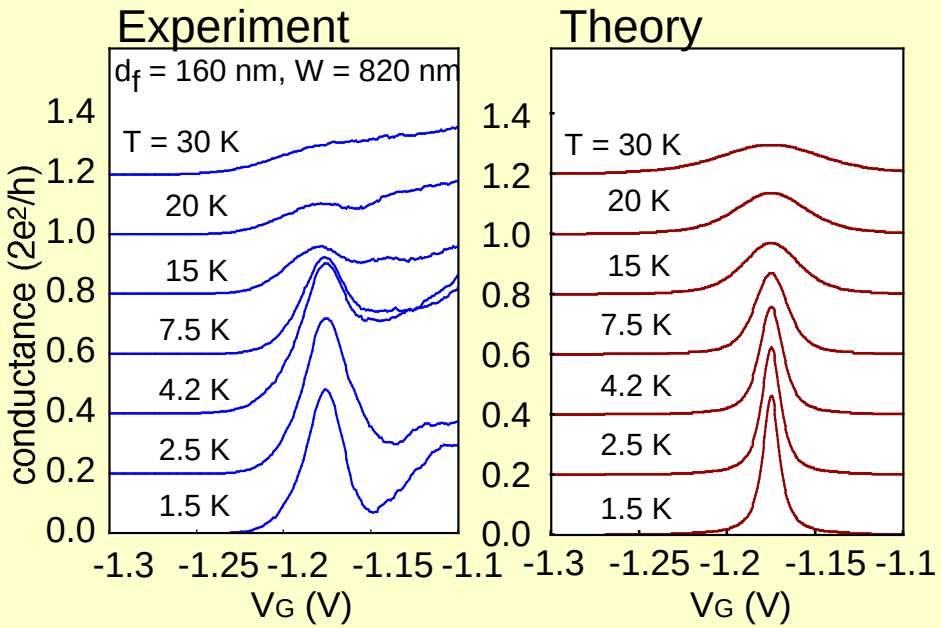
Single Electron Transport in 2-WPG SET

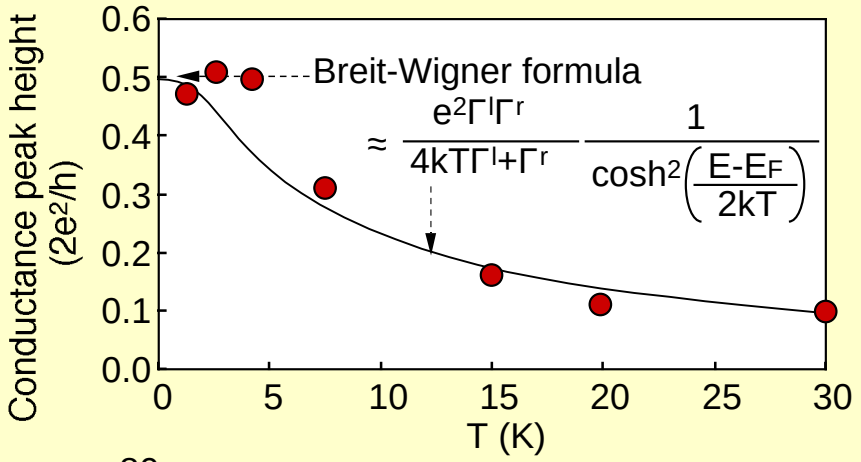
GaAs SET

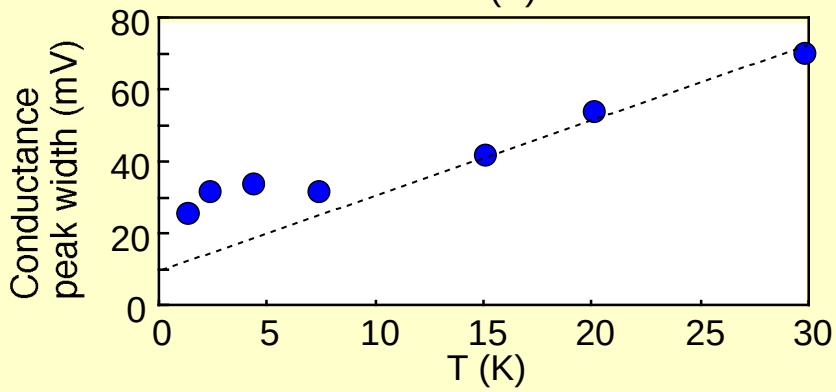


Lateral resonant tunnling of single electron

$$I = \frac{e^2}{h}\int |T(E)|^2 \,[f(E) - f(E+qV_{DS})]\, dE$$

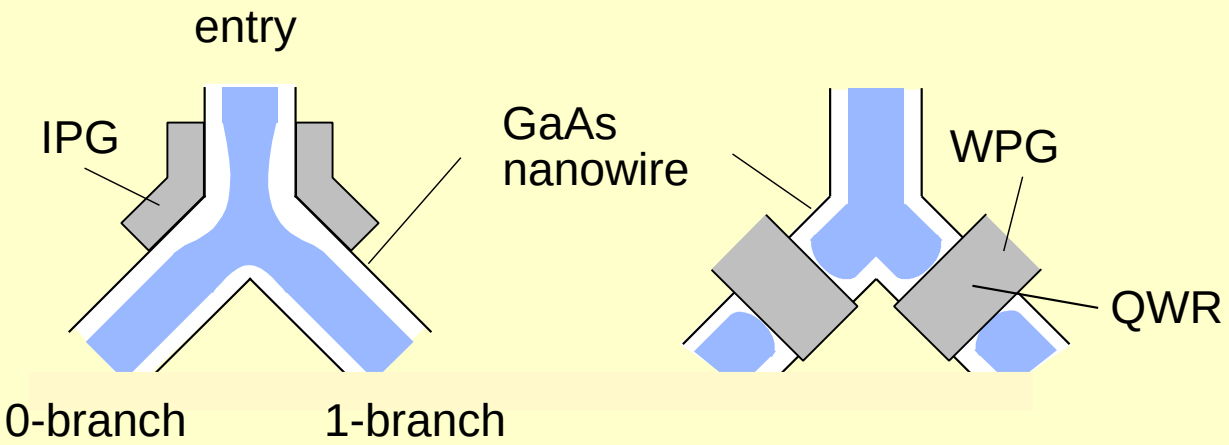




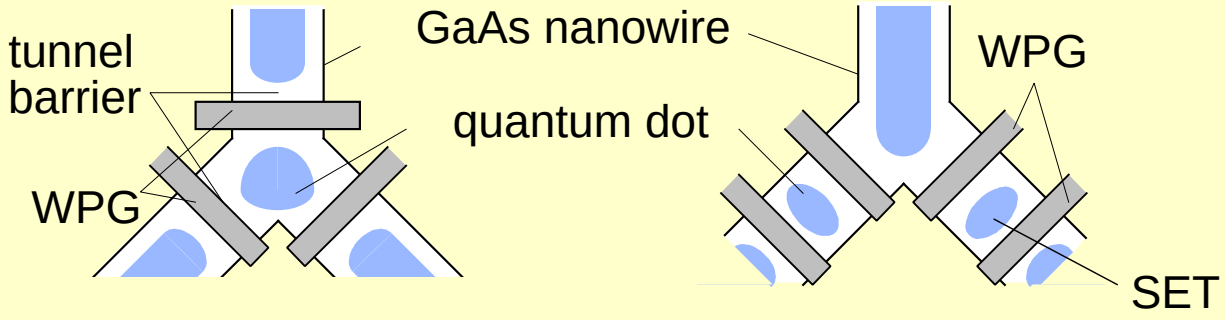


Various Types of BDD Node Devices by IPG/WPG Control of III-V Nanowires

QWR-based BDD node device

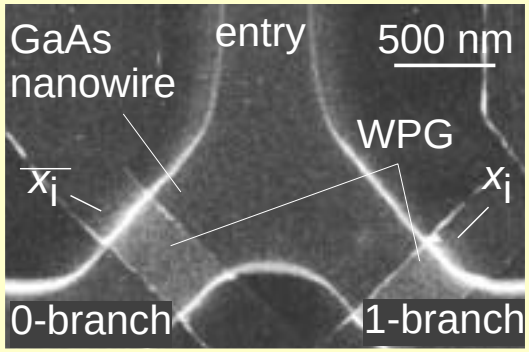


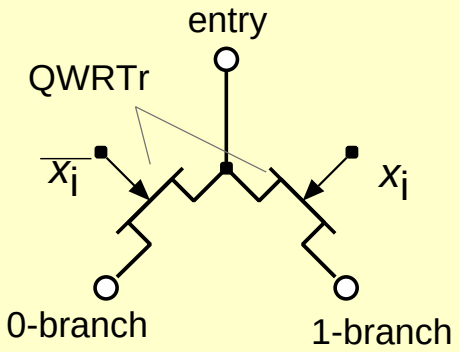
Single electron BDD node device



WPG BDD Quantum Node Device

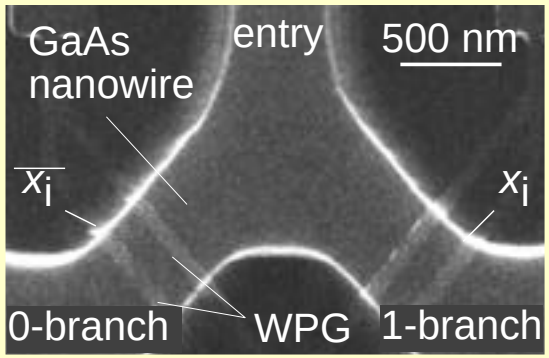
WPG QWR-based BDD device

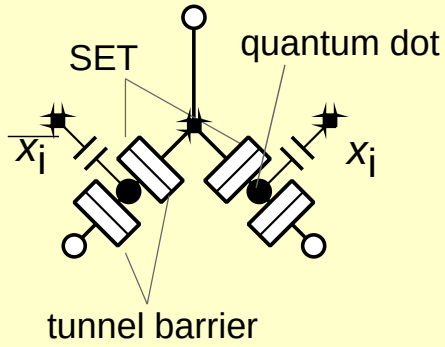




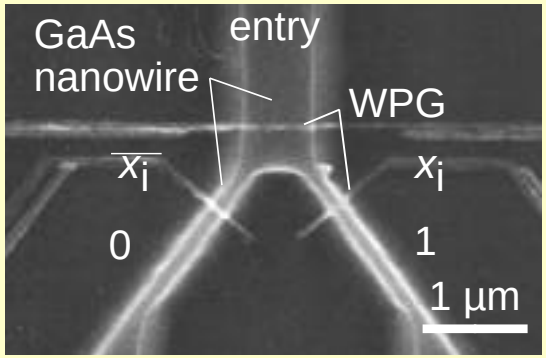
branch switch type

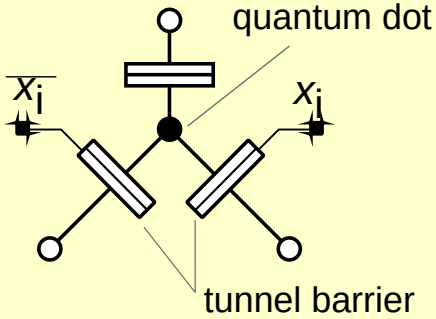
WPG single electron BDD devices





branch switch type

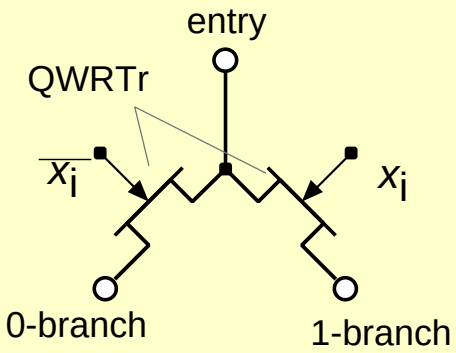




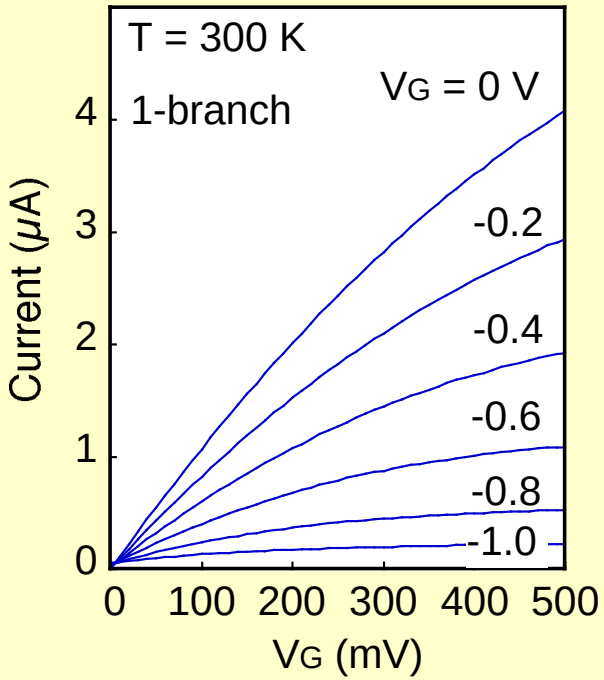
node switch type

Switching Characteristics

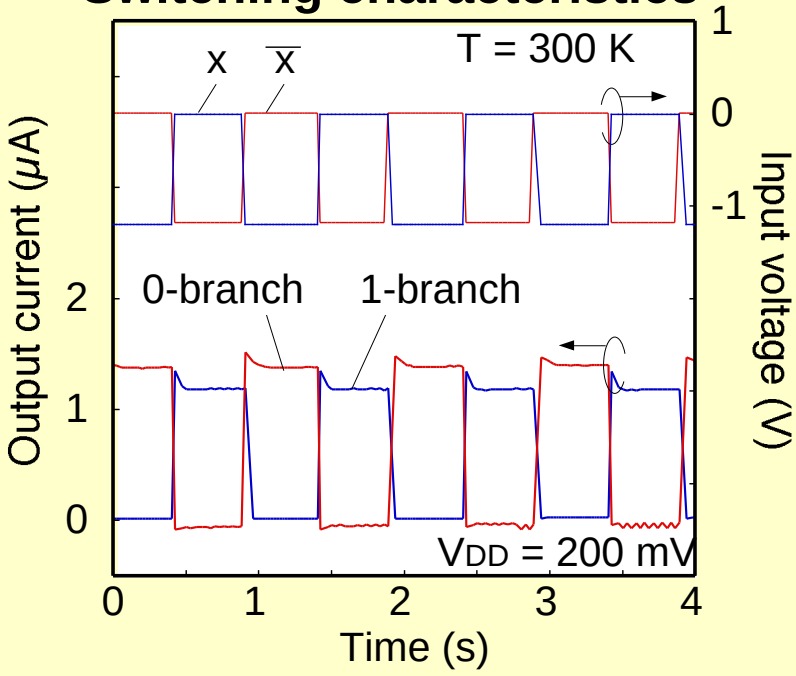
QWR branch- switch BDD node device



Branch I-V

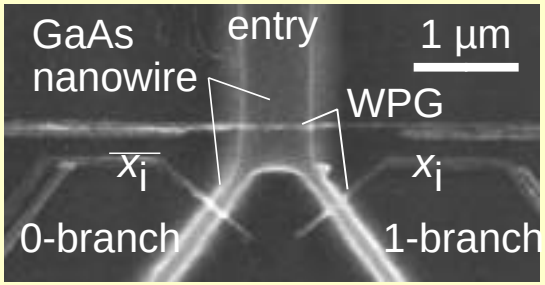


Switching characteristics

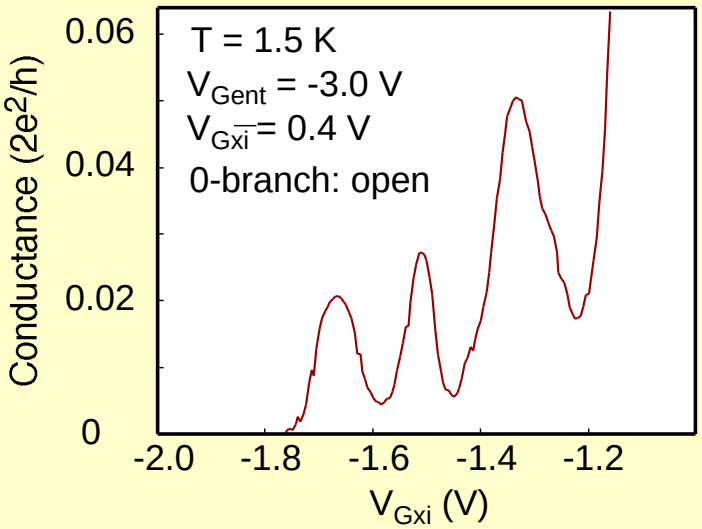


WPG BDD Single Electron Node Device

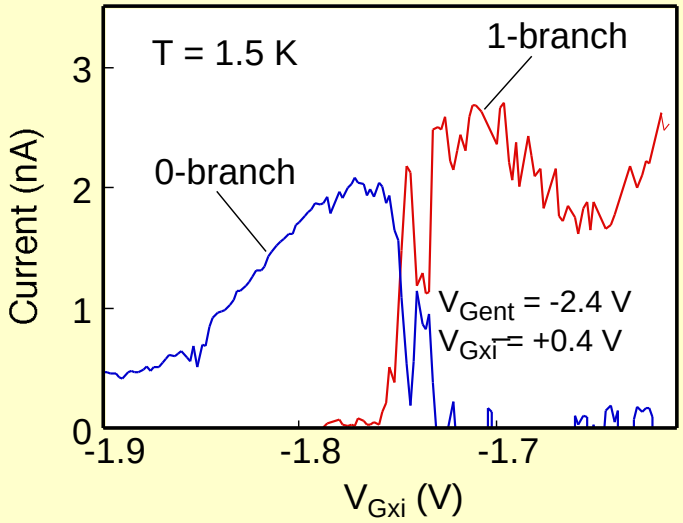
QD-based node switch device



Conductance oscillation from single channel



Switching characteristics

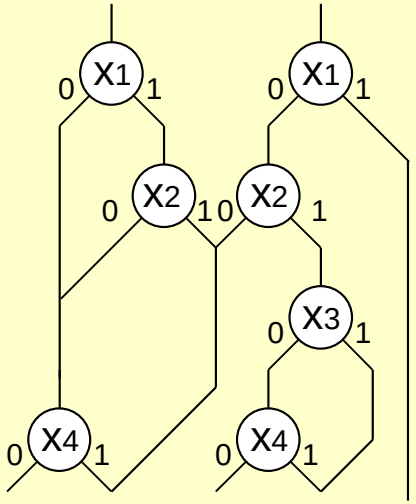


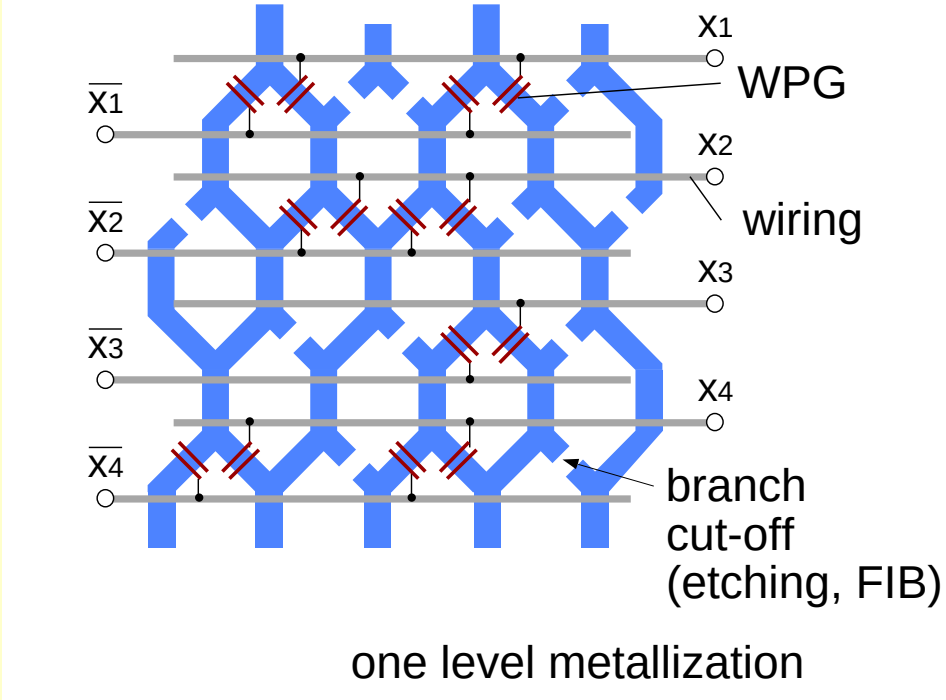
Conductance oscillation due to single electron transport
Clear path switching

Quantum BDD Implementation

Quantum BDD large scale integration

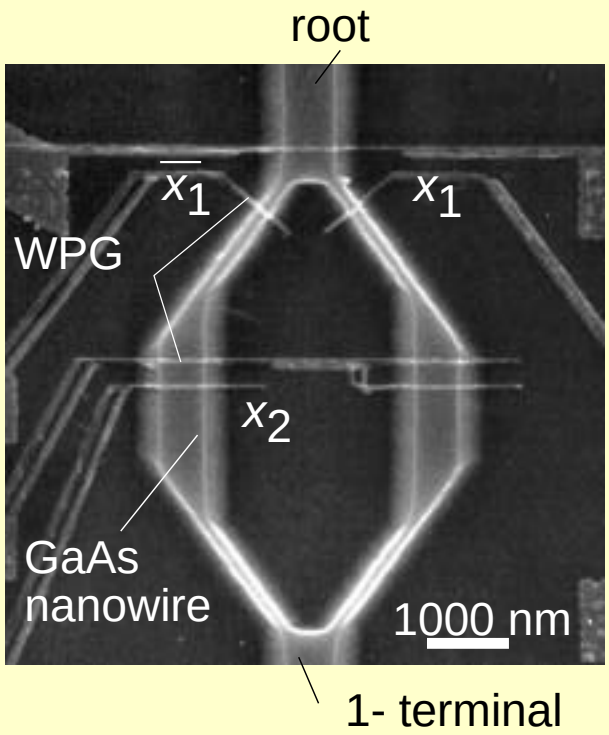
➡ **hexagonal nanowire network + WPG**

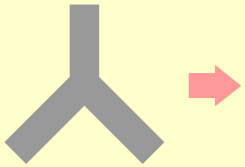




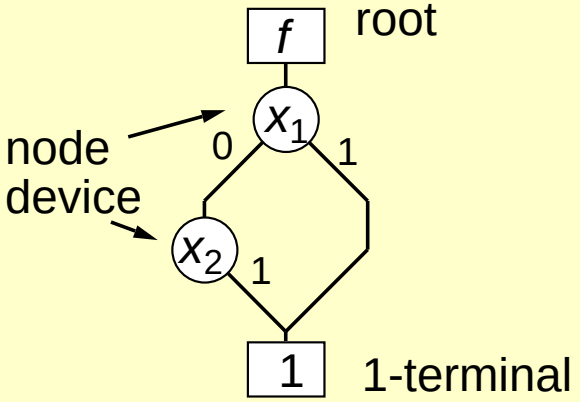
WPG BDD OR Logic Function Block

WPG single electron BDD OR circuit



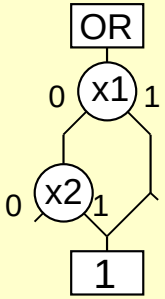


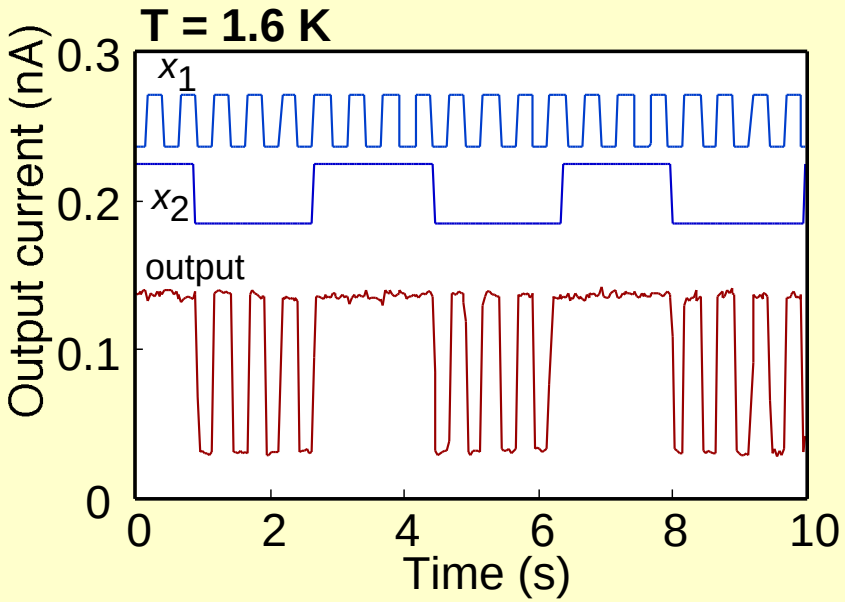
hexagonal layout



Operation of WPG BDD OR Logic

Input/Output waveform

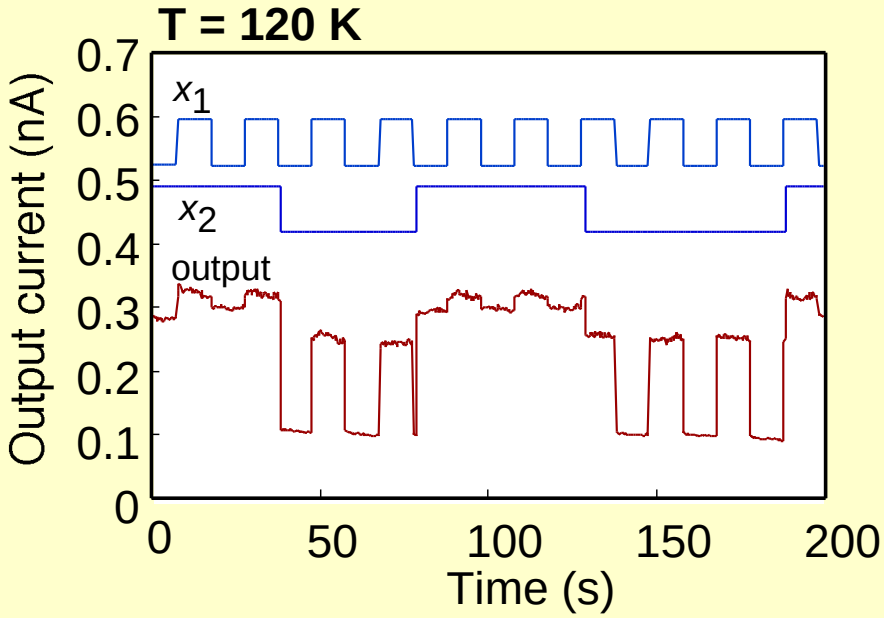




V_{DD} = 1 mV
clock: 2 Hz

pulse height
x_1: 100 mV
x_2: 250 mV

entry gate: 0 mV



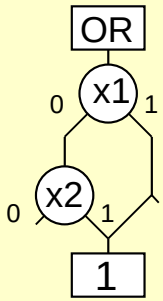
V_{DD} = 0.2 mV
clock: 0.1 Hz

pulse height
x_1: 1200 mV
x_2: 1000 mV

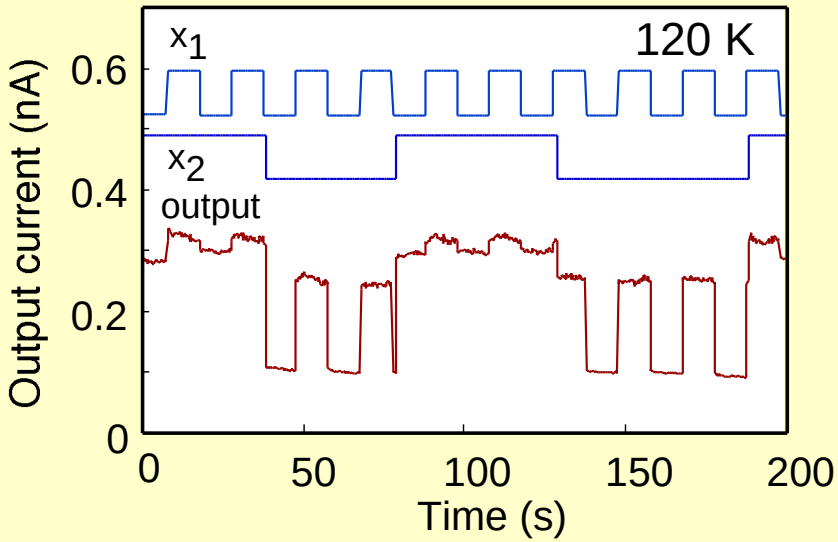
entry gate: +1000 mV

WPG BDD Fundamental Logic Family

OR

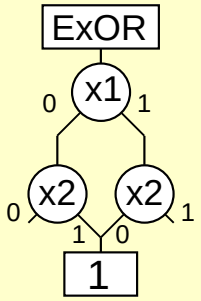


x1	x2	x1+x2
0	0	0
0	1	1
1	0	1
1	1	1

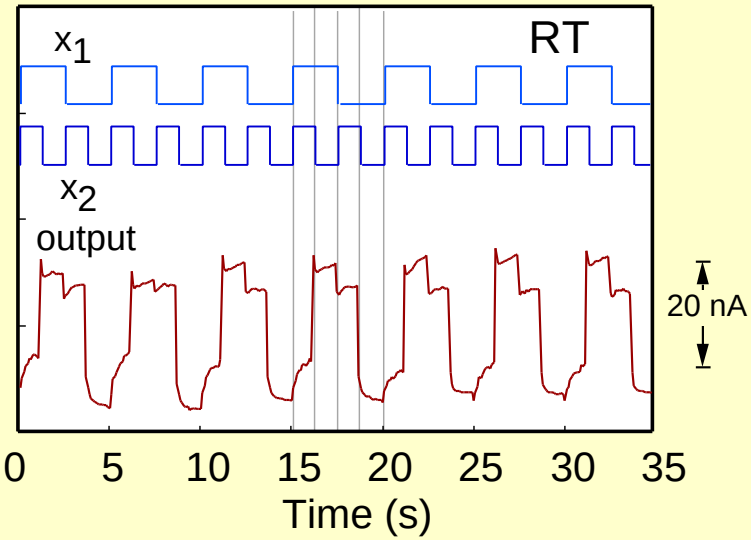


pulse height
x_1: 1200 mV
x_2: 1000 mV
entry gate: +1000 mV
V_{DD} = 0.2 mV

Half adder (exclusive OR)



x1	x2	x1⊕x2
0	0	0
0	1	1
1	0	1
1	1	0



	pulse h	offset
+x1:	0.02 V	-0.4 V
- x1:	0.44	-1.2
+x2:	1.7	1.9
- x2:	0.1	1.6

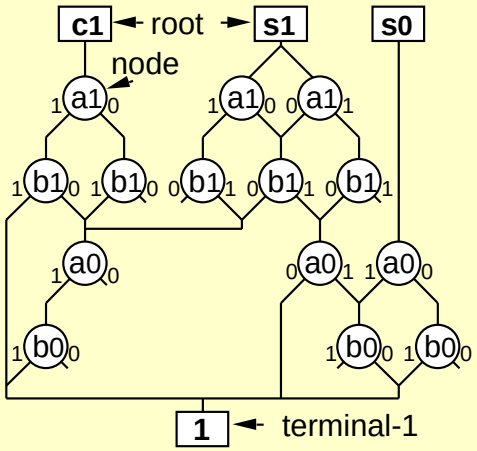
V_{DD}: 250 mV

Circuit Design and Fabrication Technology Towards BDD Quantum Integrated Circuit

Hokkaido University RC IQE

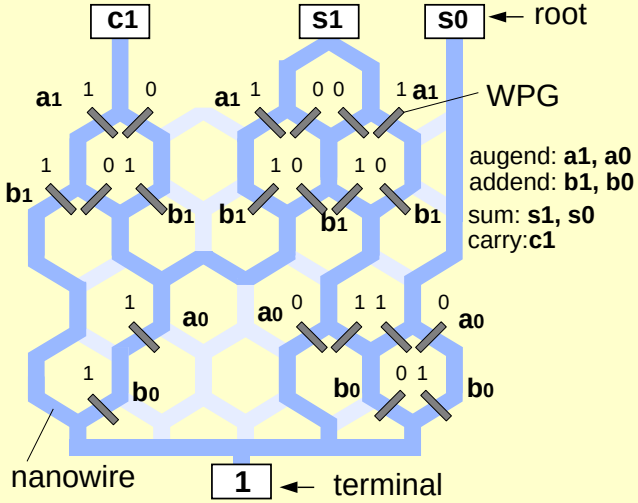
Example: BDD 2-bit adder

circuit diagram

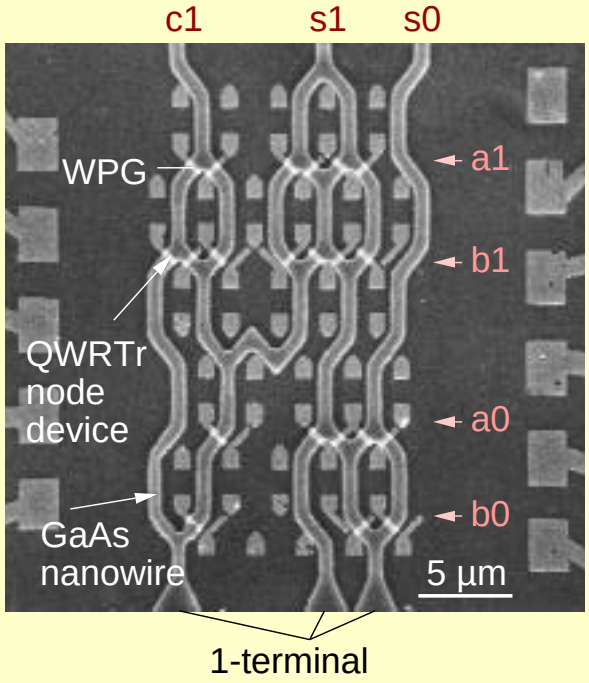


augend: **a1, a0**
addend: **b1, b0**
sum: **s1, s0**
carry:**c1**

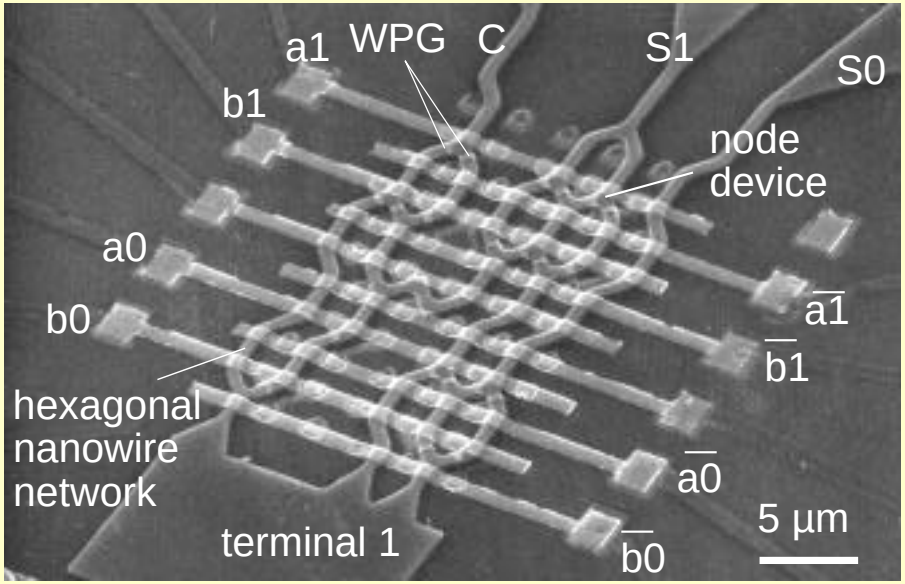
WPG/nanowire layout

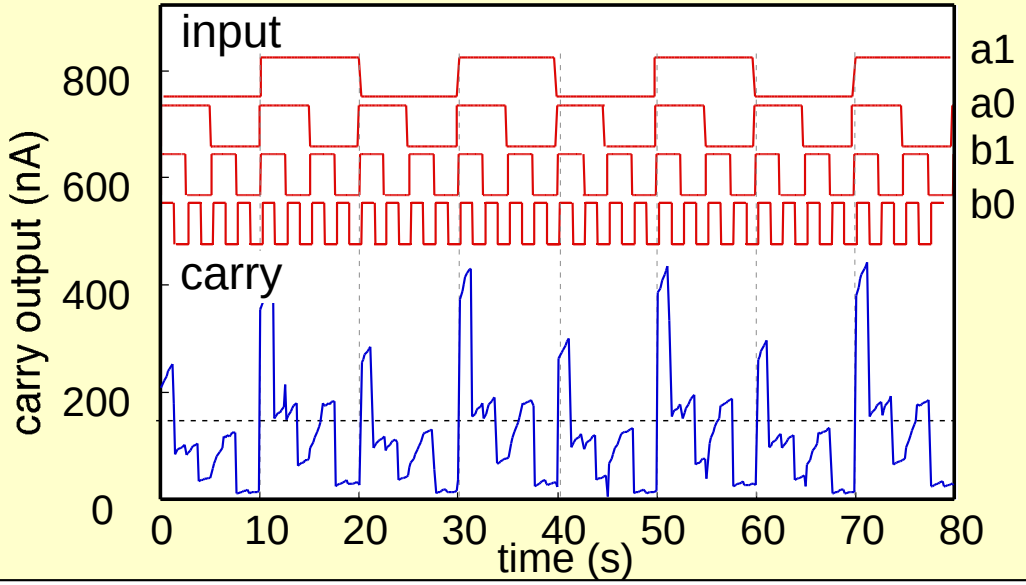


Fabricated 2-bit adder circuit



Hexagonal BDD 2 bit Adder

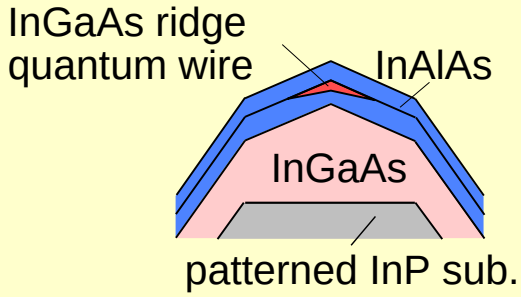


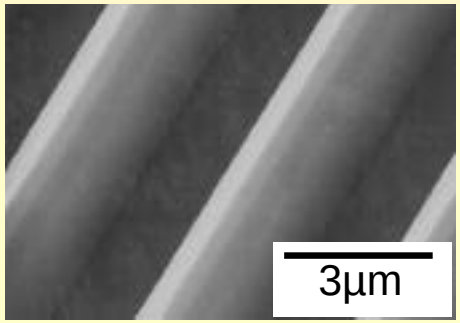


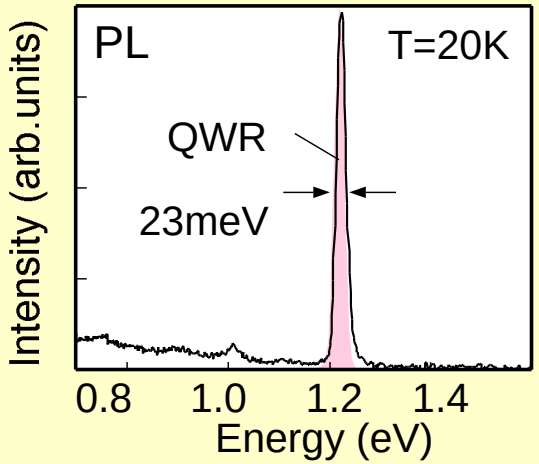
T = 300 K
VDD = 250 mV

InGaAs Ridge Nanowires for Room Temperature Operation

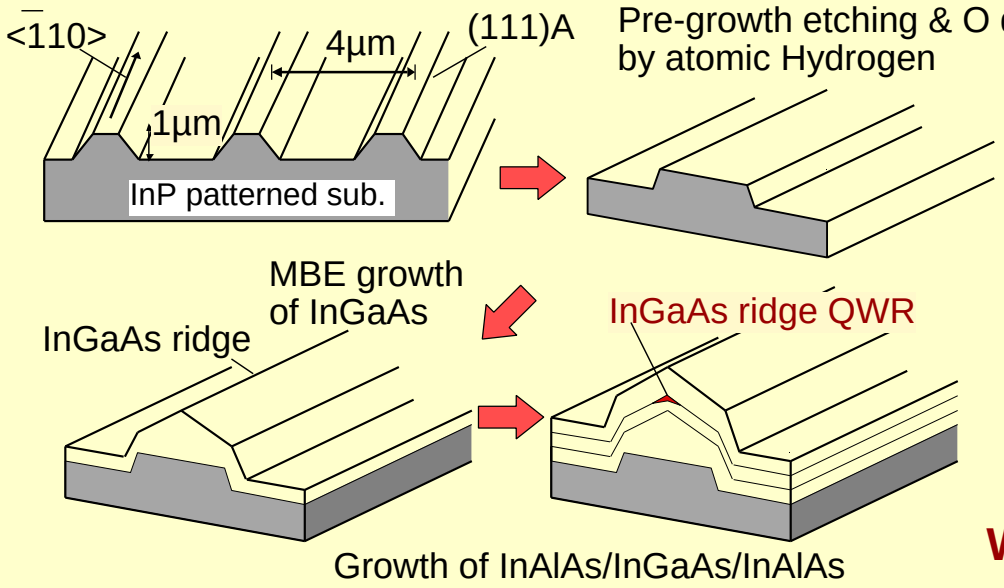
AlGaAs/GaAs etched nanowires:
possible minimum width = 70-100 nm
Room temperature operation requires sub-10 nm width

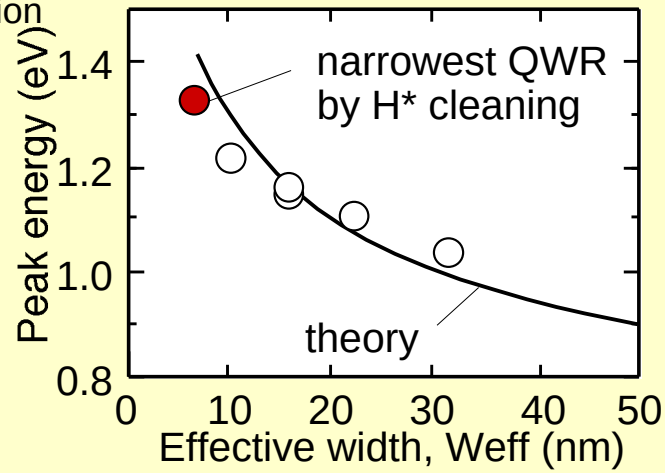






Formation Process



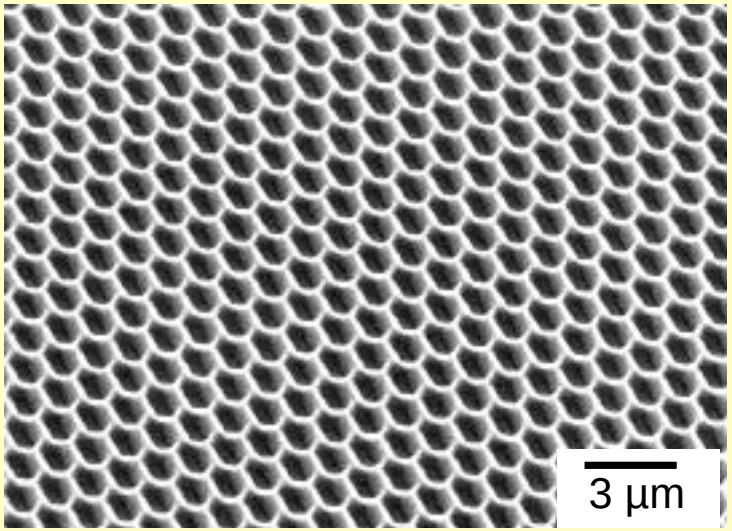


Wire width of 6 nm has been achieved

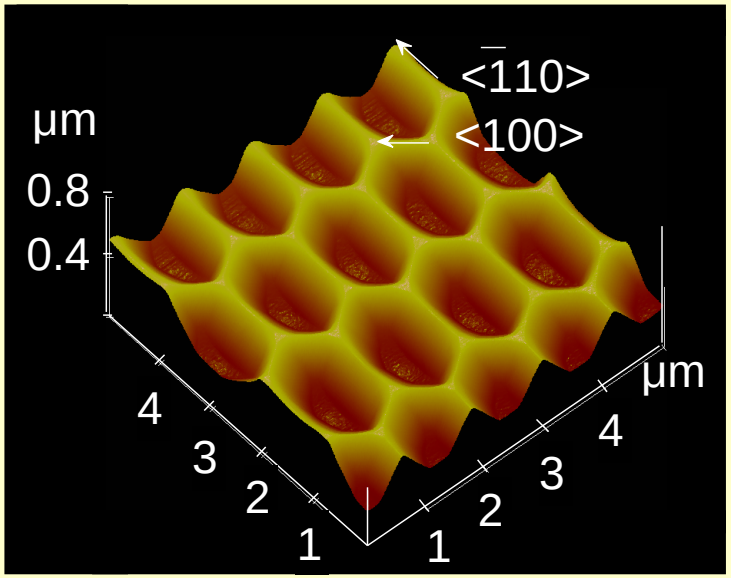
Hexagonal InGaAs Ridge Nanowire Network

Hokkaido University RC IQE

SEM image of hexagonal InGaAs nanowire network



AFM image

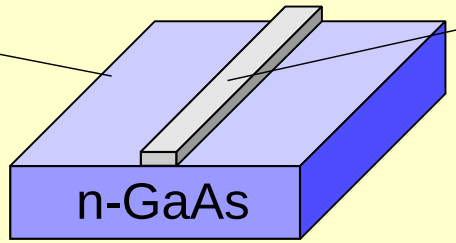


(Ito *et al*. IPRM01, ICFSI-8)

Potential Controllability of Nanometer-Sized Schottky Gates

Semiconductor surface

1. Strong pinning (0.88 eV)
2. Unpinning

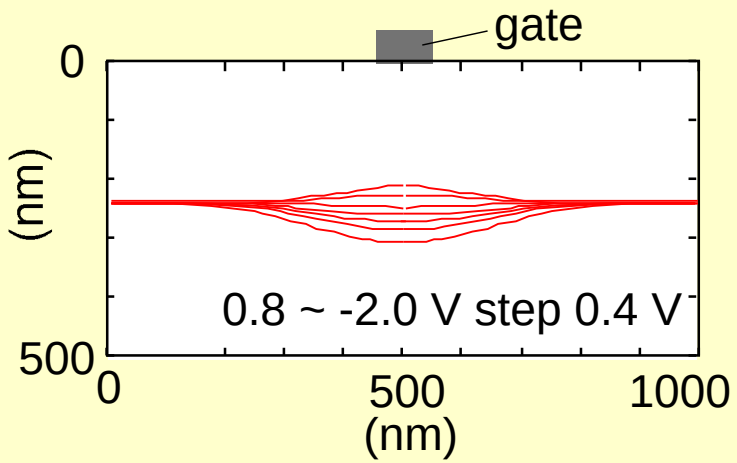


nano-Schottky gate

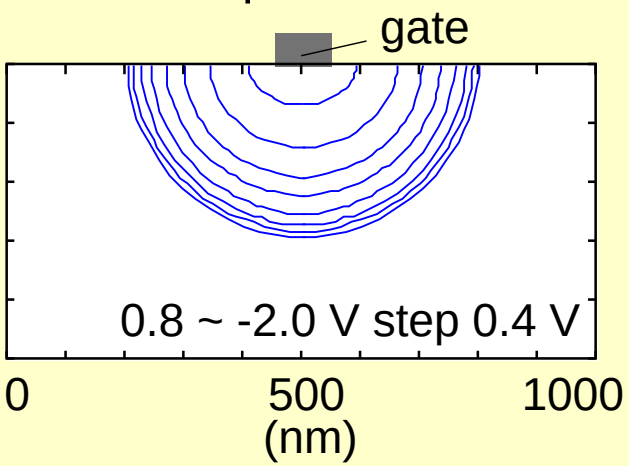
φ_{MS} = 1.0 eV

L_g = 90nm

1. With strong pinned surface



2. With unpinned surface



Control of an environmental Fermi level pinning is important

Conclusion

1) A new, simple and realistic approach for quantum LSIs is presented and discussed.

- •Architecture: BDD logic architecture
- •Hardware: Schottky WPG control of hexagonal III-V nanowire networks.

2) WPG QWR and single electron BDD node devices using GaAs etched nanowires have been fabricated and BDD switching was realized.

3) Hexagonal BDD ICs using GaAs etched nanowires have been fabricated. Logic operation has been confirmed.

4) Hexagonal InGaAs nanowire network by H* assisted selective MBE combined with IPG/WPG gate technology gives good prospect for high density BDD QLSIs that are operating at delay-power products near the quantum limit at RT.

5) Control of surface/interface remains to be a key issue.