

Problems to Final Exam in Emerging Computing Technologies in the area of Processor Architectures and Evolutionary Design

More questions, related to quantum computing and DNA computing will be added. Nano-technologies will be not included to final exam.

The exam is open book, you can use any materials during the exam. You have my promise that all questions on the exam will be selected from this list. They will be only more precisely formulated, if necessary.

A. PROBLEMS IN PARALLEL PROCESSOR DESIGN

1. Design a Hough Transform Processor for straight lines. It can be pipelined, cellular, systolic or parallel. Think about which directions of image or other parameters correspond to time and space in memory (hardware). Use either trigonometric or linear parameterization of lines.
2. Repeat problem 1 for circles.
3. Design a processor (parallel, pipelined, systolic, or cellular automata based) for edge detection. Use any algorithm for edge detection, black-and-white or grey-level images.
4. Design any processor like in point 3 for Satisfiability Checking. You can use the pipelined architecture from Monday meeting, but you have to design Boolean instructions and random number generator in more detail.
5. Repeat point 4 but for Petrick Function Minimization.
6. Repeat point 4 but for simultaneous solving of Satisfiability and Minimizing the number of positive literals in the product – solution, if the product of literals is a solution.
7. Design a pipelined processor for matching arbitrary number of patterns at the same time. Extend it to partial matching and counting of matches.
8. Given are two arrays A and B. Design a processor that calculates a Kronecker Product $A * B$ in hardware – any kind of parallelism is OK, but the processor should have some kind of parallelism.
9. What is the role of Kronecker (tensor) product in computer architecture, in quantum computing and in logic synthesis?
10. Design a processor using standard registers and binary technology that simulates (with some accuracy) the operation of a Toffoli gate (with outputs $A1, B1, A1*B1 \text{ XOR } C1$) that has Hadamard gates connected to its inputs A and B ($A1 = \text{Hadamard}(A), B1 = \text{Hadamard}(B)$). Think about the concept of Kronecker Product and Matrix Product. Draw the block diagram only, not detailed design is expected.
11. Design a processor for realization of Genetic Algorithm for Satisfiability.
12. Design a processor for realization of Genetic Algorithm for Traveling Salesman Problem.

13. Design a binary tree processor that has n leaves to calculate a greatest common divisor of $2n$ numbers. Attempt at high parallelism of operations.
14. Design a processor to calculate Fixed Polarity Reed Muller form of any function specified by minterms. Polarity is stored in additional register. The design should be correct for any of 2^n polarities.
15. Design a systolic architecture for matrix-vector multiplication
16. Design a systolic processor for matrix-matrix multiplication in which the result remains in the processors.
17. Design a systolic processor for matrix-matrix multiplication in which the result is pipelined out of the regular structure during calculation.
18. Design a systolic architecture for one-dimensional convolution
19. Design a systolic architecture for two-dimensional convolution
20. Propose any type of binary tree architecture and describe its application on which a high speedup exists. Illustrate.
21. Design a sorter-absorber in systolic or combinational architecture.
22. Design a systolic sorter that removes repeated numbers.
23. Design a sorter of pairs (number, value) that sorts according to the number, the sorted results should be in increasing order and if there are many pairs with the same number all but one are removed during sorting.
24. Design a tree architecture for the maximum clique problem.
25. Design a cellular automaton that counts in code 0, 1, 2, 00, 01, 02, 10, 11, 12, 20, 21, 22, 000, 001, etc
26. Compare briefly some typical FPGAs and EPLDs.
27. Flynn taxonomy.
28. What are systolic processors? Their advantages. Examples of most successful applications.
29. Networks for parallel processors, their characteristics and links with FPGA and CA architectures.
30. Main regular structures of systolic processors. Examples of applications for each type of structure.
31. Advantages and disadvantages of hypercubes
32. What are the similarities of architectures for FIR filters, 1-D convolution and polynomial multiplication? Explain and illustrate on examples of architectures for these problems.
33. Design and compare two systolic architectures for the same problem, it can be 1-D or 2-D convolution or any other similar problem for which systolic design is a good choice.
34. Reconfigurable pipelines – illustrate with one application – explain advantages of this approach.
35. Design two variants of an architecture for polynomial evaluation.
36. List the CAD tools that are necessary for reconfigurable pipeline design.
37. Design on block- logic level the pipelined processor for Sieve of Eratostenes.
38. Sorting and merging systolic processors other than those discussed in class and Monday meetings.
39. Design of combinational array multiplier. How to modify it to pipelined and systolic designs?
40. LFSR circuits, principle, analysis and their uses
41. Morphological Processor for Erosion and Dilation – consider pipelined versus CA designs.

B. PROBLEMS IN REGULAR ARCHITECTURES AND CELLULAR AUTOMATA

1. How to realize arbitrary Boolean function using lattice model?
2. Show how to realize a Cellular Automaton that uses only D type flip flops and Toffoli gate to implement arbitrary symmetric function. What would be the delay for a worst case symmetric function of 4 variables?
3. Design a Reversible Cellular Automaton based on Margolus method separating to odd and even cycles, the operation of which is described by two sets of arbitrary rules. Show and explain your methodology. How the rules are stored? In memory? By programming FPGA?, using multiplexers? Your choice, but explain in detail what you are doing.
4. Characterize in your own words the regular architectures and how their properties can be used for increased reliability of design.
5. Discuss using Cellular Automata for cryptography and random number generation.
6. What are the methodologies used to investigate Cellular Automata.
7. Cellular Automata versus Field Programmable Gate Arrays.
8. Show how to realize NAND and NOR using Quantum Dots.
9. What is specific about designing logic circuits using Quantum Dots?
10. What are the logic and memory functions of the cellular cell in any known to you 3D CA model. If you do not know, propose one and defend your proposal.
11. How morphogenesis is investigated using CAs?
12. Applications of Reversible CAs.
13. Design the simplest possible Reversible Cellular Automaton on the level of D type Flip-Flops and logic gates.
14. Repeat problem 13 using quantum dot CA technology to design a cell of reversible CA. This leads to a hierarchical CA, how many pulses of the low level clock correspond to one pulse of the implicit high level clock?

C. PROBLEMS IN EVOLUTIONARY ALGORITHMS

1. Explain the role of parameters of genetic algorithm that control mutation and crossover.
2. Present methods for Parent Selection.
3. Give brief definitions of various types of Evolutionary Algorithms.
4. Write short essay on the role of Fitness Function.
5. What is Darwinian, Baldwinian and Lamarckian GA?
6. Present any application of your choice of any evolutionary algorithm
7. Present a concept of GA or GP for a sorting architecture optimized for speed and cost.
8. Discuss the issue “phenotype versus genotype” in applying an evolutionary algorithm to any design problem, for instance in logic design.
9. Discuss types of crossover operations and their advantages/disadvantages
10. Pareto Points in GA

11. Present multi-criteria optimization using evolutionary algorithms.
12. The concept of fitness landscape.
13. The concept of a designer in the loop of a genetic algorithm. Discuss, analyze, propose new applications.
14. Give one application of Evolutionary Programming.
15. Operations in Genetic Programming.
16. Give an example of a GA with repair
17. Explain the principle of evolvable hardware, give examples of applications.
18. Illustrate in detail one application of GA or GP to a selected by you problem of logic synthesis, other than one discussed in the class (quantum circuits)
19. Give examples of two Evolutionary Strategies for any design problems.
20. Give a well-known example of applying any evolutionary algorithm in a practical industrial problem which led to considerable success.
21. Give examples of using EA in any design area other than “game of life”, logic design and quantum circuit design.
22. Present your own idea about linking an EA to any machine learning method.

D. PROBLEMS IN FPGAs AND PROGRAMMABLE STRUCTURES

1. Explain differences of various types of Field Programmable Arrays. What are their applications, future of this kind of devices.
2. Compare FPGAs and EPLDs to full custom and gate array designs.
3. What are EPLD architectures?
4. The concept of CPLD.
5. What are basic types of FPGAs?
6. Explain the lookup table architecture
7. What are the main issues in FPGA technologies?
8. Computer Aided Design versus FPGA technology? Why only USA produces FPGAs?
9. Compare Xilinx and Altera architectures.
10. Propose your own FPGA architecture and make a point why it may be competitive on FPGA/PLD market.
11. FPGAs versus systolic processors versus Cellular Automata.
12. List all known and possible good applications for FPGAs.