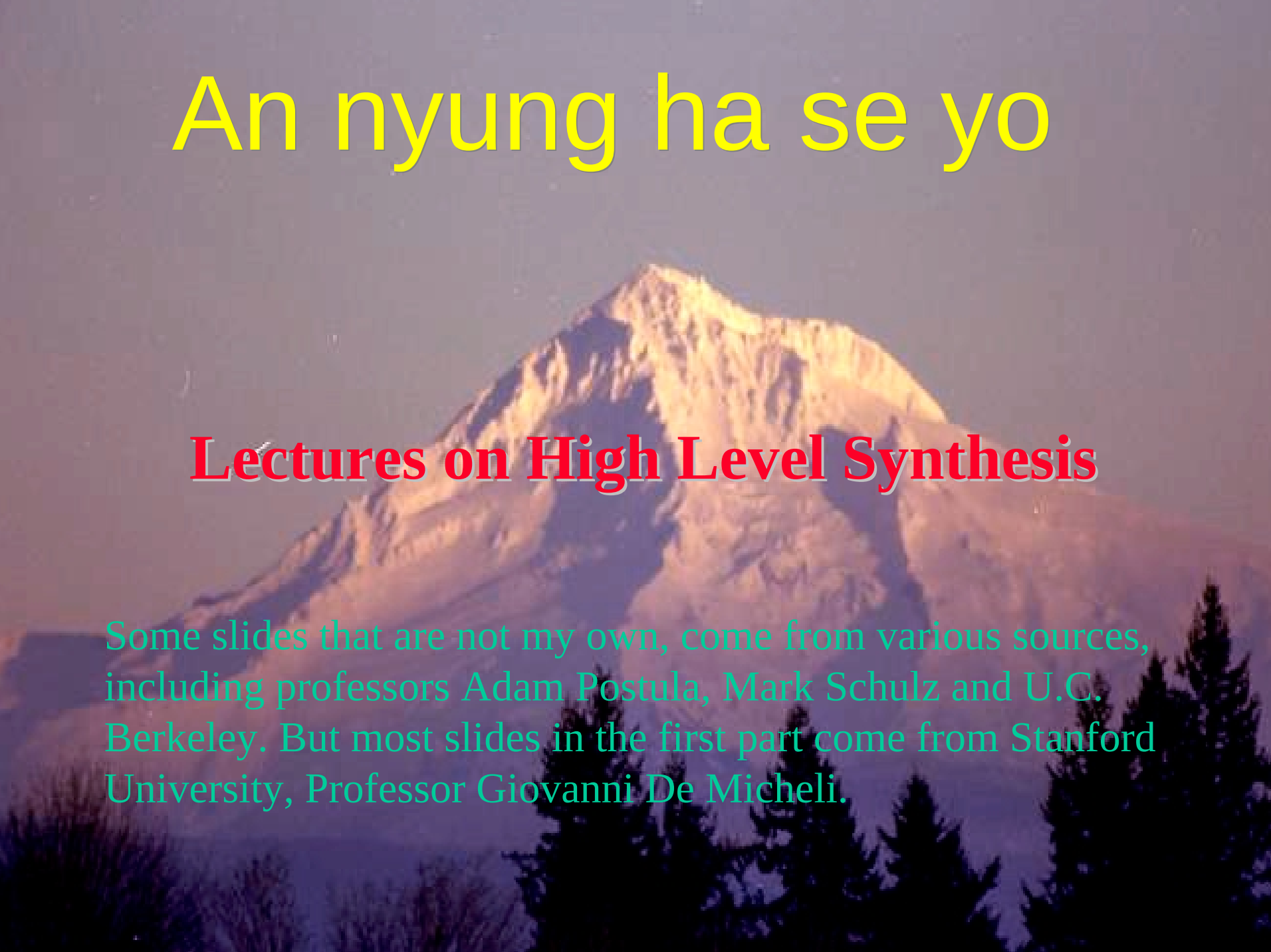


An nyung ha se yo

Lectures on High Level Synthesis

Some slides that are not my own, come from various sources, including professors Adam Postula, Mark Schulz and U.C. Berkeley. But most slides in the first part come from Stanford University, Professor Giovanni De Micheli.

878
High Level Synthesis Algorithms for CAD

Professor: Marek Perkowski

마 르 켁 표 케 르 코 쁘 스 키

mperkows@ee.kaist.ac.kr

http://www.ee.pdx.edu/~mperkows

http://eepia.kaist.ac.kr/~mperkows/

- **My room:** Yang Sang Dong, left room of 1325
- Everybody is welcome to come to my room to introduce yourself and ask questions.

878
High Level Synthesis Algorithms for CAD

- Introduction
- Grading
- What is this class about
- Example of a covering problem

Do not take notes

All slides will be on my webpage

All homework and project explanations will be on my webpage

I do not assume much background knowledge from you

Basic Boolean Logic

Basic graph theory

Basic programming skills in Basic or C, C++

The good news is that I will review much of this background material

Also, there will be additional meetings just to review the material and solve problems.

Participation in those meetings is not mandatory, and you can get an A without participating.

However, participating will help you in homeworks and projects.

Mr. Chun Ho Kim will help me as a TA for this class. Please communicate with him and he will relate your questions to me

All homeworks, projects and final exam will be graded by me only.

Participation in those meetings is not mandatory, and you can get an A without participating.

However, participating will help you in homeworks and projects.

Goals of this class

- Many of you are using some CAD tools. Do you know what is inside these tools? Here you will learn.
- Do you want to design better algorithms and software for your specific tasks? This class can help. I will teach both fundamentals and applications.
- Teach about relations between data structures, algorithms and CAD tools.
- Examples of my previous projects from US industry (companies like GTE, Sharp, Intel and Cypress) and US government (Wright Laboratories of Air Force).
- The algorithms and concepts presented in this class are very general. They can be used in Machine Learning, Testing, Data Mining, Pattern Recognition, and Robotics.
- We will concentrate on basic algorithms and how to use them for new problems that you may find in your research.

Objective of Subject

- Both theory and practical applications.
- Students will learn modern EDA (Electronic Design Automation) approaches and fundamentals of building tools
- Do not be scared that the class is taught in English.
- If I speak too quickly, please tell me. I will slow down.
- I will give you some challenging research problems that nobody solved or even formulated. You can work on them and we can publish them, **but it is not mandatory,** only for those who like a challenge.

Objective of Subject

- Students will learn about techniques of specifying sequential designs and optimizing them on a **Register Transfer Language** Level
- These techniques can be used to Computer, Digital Signal Processing (DSP) and Image Processing architectures. You can use your own examples.
- At the end, some recent research and industrial papers from top conferences and journals will be discussed to show the modern research areas.
- Modern realization technologies will be presented, **FPGAs**
- **Unified approach to many problems.**
- **After completing the class students should be able to create new applications and software for new EDA tools**

What in coming weeks?

- Look to my WWW Page.
- Review and Introduction.
- Basic graph algorithms
- Representations of Functions, Relations and State Machines.
- Overview of CAD systems
- Levels of modeling
- Basic high level synthesis methodologies

Homeworks

- Homeworks will be to solve practical problems illustrating the algorithms and data structures, such as set covering, graph coloring, shortest path, satisfiability or scheduling.
- Some homeworks will be to optimize simple processors using methods from the class.
- One homework will be to create an **animated PowerPoint** presentation and present it in the class.
- You may exchange it for creating your WWW Page with a problem solution.

Grading System

- Homeworks = 35 %
- Midterm = 15 %
- Final Exam = 20 %
- Project = 30 %
  - Final examination - Questions theoretically from all the course, but with special emphasis on the second half of the course, it means, the material covered after midterm examination and projects.
  - Midterm Examination (open book, in class)
  - Homeworks, including student presentations
  - Project: - your choice --
    - » programming assignments
    - » theoretical work
    - » literature study
    - » processor designs using optimization methods from the class

Remember that the midterm exam is:

Open Book

Remember that I really want to help you to be successful in this class and obtain a good grade.

Do not be afraid to speak in English, it is better to speak with mistakes than to avoid communication

TEXTBOOK

- Strongly Recommended
  - ***Giovanni De Micheli,*** Synthesis and Optimization of Digital Circuits. *Mc Graw Hill International Editions*, *Electrical Engineering Series*. ISBN 0-07-113271-6.

  - **This textbook is the most popular in USA and is used in top universities**
  - It has many examples and its language is quite easy.
  - Even if you do not understand my English, you can learn from this textbook to get a grade of A in this class. My examples and additional material that I will teach is just to help to illustrate the ideas better. They will be NOT required in homeworks and exams.
  - The material from the book will be on slides. All slides can be printed and used to learn the material.

- Background
  - Randy Katz, *Contemporary Logic Design*, Benjamin/Cummings, 1994. This book is already used in KAIST.

Other Information

- There is a WWW Home page for the class. I will keep updating it every day, also to reflect a feedback from you.
- All PowerPoint 4.0 slides you see here, plus a Postscript printable version with 6 slides per page will be available.
- Lectures will be available within 24 hours after the lecture is given (mainly because I will be completing the lectures on Sunday nights and Monday mornings prior to the lecture).
- All sorts of other info will be there as well.
- Class announcements will appear in the “class schedule” pages of this class at the KAIST WWW page of Marek Perkowski.
- Much additional material is on my US webpage, but using it is not mandatory.

Other Information

- Use **Internet Explorer** or **Netscape** to view these pages.
- Send emails with questions.
- If you are shy to ask in class or want to be anonymous, please leave me a question on a paper sheet before class on the desk.
- I will post news for class students of this group. I presume that it is read within 2 or 3 working days. **YOU ARE RESPONSIBLE FOR READING THE NEWS IN CLASS SCHEDULE LINK!**

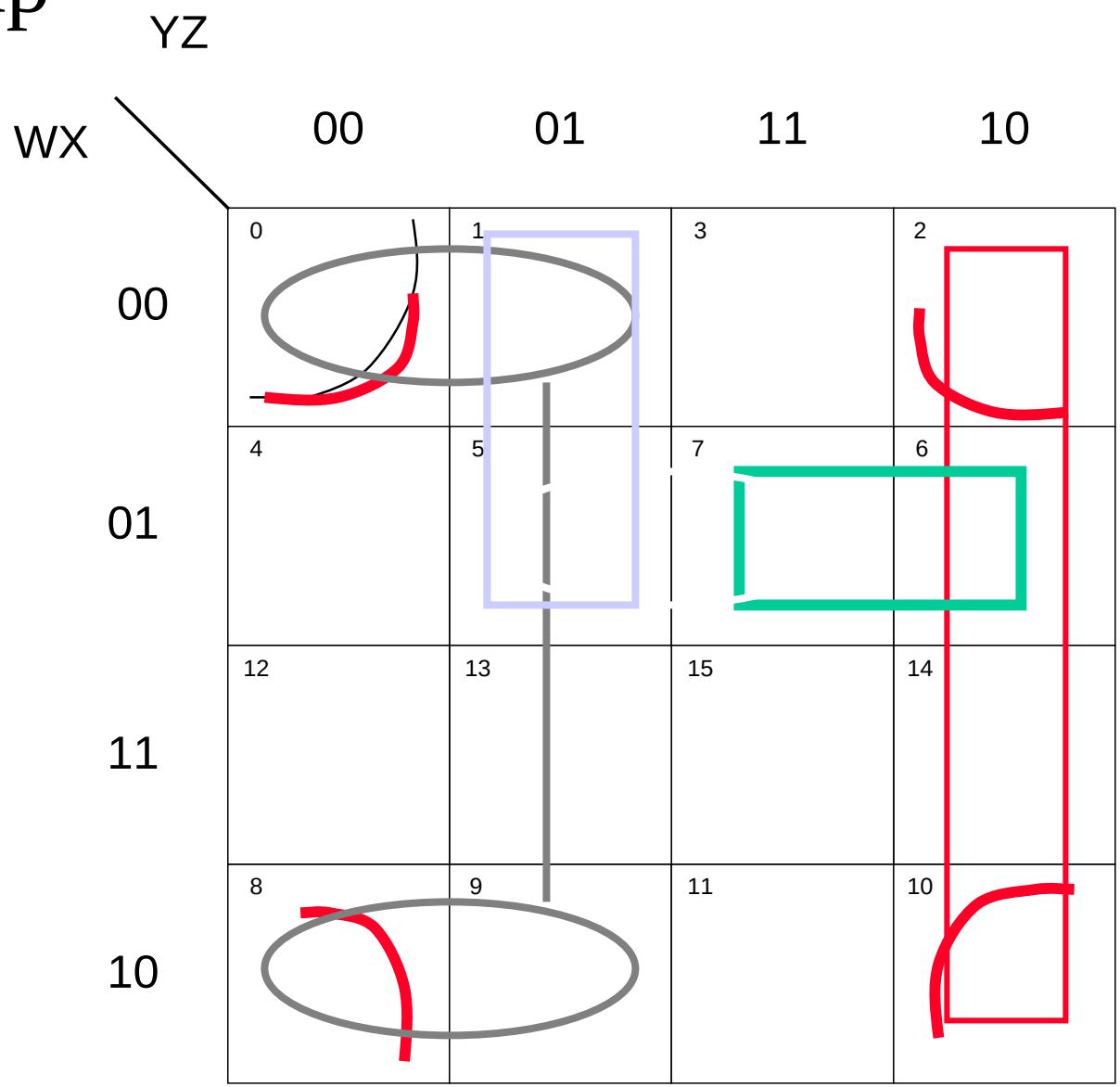
Any Other Administrative Details?

- ! Now is the time to ask

Karnaugh Map

WX \ YZ	00	01	11	10
00	0 **1**	1 **1**	3	2 **1**
01	4	5 **1**	7 **1**	6 **1**
11	12	13	15	14 **1**
10	8 **1**	9 **1**	11	10 **1**

Karnaugh Map



Prime Implicant		0	1	2	5	6	7	8	9	10	14
(1, 5)	0-01		x		x						
(5, 7)	01-1				x		x				
(6, 7)	011-					x	x				
(0, 1, 8, 9)	-00-	x	x					x	(x)		
(0, 2, 8, 10)	-0-0	x		x				x		x	
(2, 6, 10, 14)	--10			x		x				x	(x)

What should you review for next time?

- Please review the Kmap, implicants and covering from any undergraduate textbook such as Roth or Katz
- Review basic Boolean algebra, De Morgan rules, factorization and flip-flops (D,T,JK).
- You should be able to take arbitrary Kmap of 5 variables, truth table, netlist or expression and convert it to a truth table or Kmap.
- Next you should be able to minimize it and draw a schematic with gates such as EXOR, NAND, NOR, etc.
- You should be able to reformulate problem expressed in English as a Boolean minimization or decision problem.
- These are the minimum information to start practical design problems.