# Some Recent Research Issues in Quantum Logic

#### Marek Perkowski

**Part** one

# What will be discussed?

- 1. Background
- 2. Quantum circuits synthesis
- 3. Quantum circuits simulation
- 4. Quantum logic emulation and evolvable hardware
- 5. Quantum circuits verification
- 6. Quantum-based robot control



Origin of slides: John Hayes, Peter Shor, Martin Lukac, Mikhail Pivtoraiko, Alan Mishchenko, Pawel Kerntopf.

# A beam-splitter



The simplest explanation is that the beam-splitter acts as a classical coin-flip, randomly sending each photon one way or the other.





The simplest explanation must be wrong, since it would predict a 50-50 distribution.

# More experimental data





The particle can exist in a linear combination or *superposition* of the two paths



# **Probability Amplitude and Measurement**

If the photon is measured when it is in the state  $\alpha_0 |0\rangle + \alpha_1 |1\rangle$  then we get  $|0\rangle$  with probability  $|\alpha_0|^2$ 



# **Quantum Operations**

The operations are induced by the apparatus *linearly*, that is, if  $|0\rangle \rightarrow \frac{i}{\sqrt{2}}|0\rangle + \frac{1}{\sqrt{2}}|1\rangle$ 

and 
$$|1\rangle \rightarrow \frac{1}{\sqrt{2}}|0\rangle + \frac{i}{\sqrt{2}}|1\rangle$$

#### then

$$\begin{aligned} \alpha_{0}|0\rangle + \alpha_{1}|1\rangle &\rightarrow \alpha_{0}\left(\frac{i}{\sqrt{2}}|0\rangle + \frac{1}{\sqrt{2}}|1\rangle\right) + \alpha_{1}\left(\frac{1}{\sqrt{2}}|0\rangle + \frac{i}{\sqrt{2}}|1\rangle\right) \\ &= \left(\alpha_{0}\frac{i}{\sqrt{2}} + \alpha_{1}\frac{1}{\sqrt{2}}\right)|0\rangle + \left(\alpha_{0}\frac{1}{\sqrt{2}} + \alpha_{1}\frac{i}{\sqrt{2}}\right)|1\rangle \end{aligned}$$

### **Quantum Operations**

#### Any linear operation that takes states $\alpha_0 |0\rangle + \alpha_1 |1\rangle$ satisfying $|\alpha_0|^2 + |\alpha_1|^2 = 1$

#### and maps them to states $\alpha_0 | 0 \rangle + \alpha_1 | 1 \rangle$ satisfying

$$\left|\alpha_{0}^{'}\right|^{2} + \left|\alpha_{1}^{'}\right|^{2} = 1$$

must be UNITARY







# corresponds to $\begin{pmatrix} 1 & 0 \\ 0 & e^{i\phi} \end{pmatrix}$





#### corresponds to



$$\mathbf{U} = \begin{bmatrix} \mathbf{u}_{00} & \mathbf{u}_{01} \\ \mathbf{u}_{10} & \mathbf{u}_{11} \end{bmatrix}$$

#### is unitary if and only if

$$UU^{t} = \begin{bmatrix} u_{00} & u_{01} \\ u_{10} & u_{11} \end{bmatrix} \begin{bmatrix} u^{*}_{00} & u^{*}_{10} \\ u^{*}_{01} & u^{*}_{11} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} = I$$



The two position states of a photon in a Mach-Zehnder apparatus is just one example of a quantum bit or *qubit* 

Except when addressing a particular physical implementation, we will simply talk about "basis" states  $|0\rangle$  and  $|1\rangle$ 

and **unitary operations** like





An arrangement like



is represented with a network like



# **More than one qubit**

If we concatenate two qubits

 $\begin{pmatrix} \alpha_0 | 0 \rangle + \alpha_1 | 1 \rangle \end{pmatrix} \begin{pmatrix} \beta_0 | 0 \rangle + \beta_1 | 1 \rangle \end{pmatrix}$ we have a 2-qubit system with 4 basis states  $|0\rangle |0\rangle = |00\rangle \quad |0\rangle |1\rangle = |01\rangle \quad |1\rangle |0\rangle = |10\rangle \quad |1\rangle |1\rangle = |11\rangle$ and we can also describe the state as  $\alpha_0 \beta_0 |00\rangle + \alpha_0 \beta_1 |01\rangle + \alpha_1 \beta_0 |10\rangle + \alpha_1 \beta_1 |11\rangle$   $\begin{pmatrix} \alpha_0 \beta_0 \end{pmatrix}$ 

or by the vector

$$\begin{pmatrix} \boldsymbol{\alpha}_{0}\boldsymbol{\beta}_{0} \\ \boldsymbol{\alpha}_{0}\boldsymbol{\beta} \\ \boldsymbol{\alpha}_{1}\boldsymbol{\beta}_{0} \\ \boldsymbol{\alpha}_{1}\boldsymbol{\beta}_{1} \end{pmatrix} = \begin{pmatrix} \boldsymbol{\alpha}_{0} \\ \boldsymbol{\alpha}_{1} \end{pmatrix} \otimes \begin{pmatrix} \boldsymbol{\beta}_{0} \\ \boldsymbol{\beta}_{1} \end{pmatrix}$$

# **More than one qubit**

In general we can have arbitrary superpositions

$$\begin{aligned} \alpha_{00} |0\rangle |0\rangle + \alpha_{01} |0\rangle |1\rangle + \alpha_{10} |1\rangle |0\rangle + \alpha_{11} |1\rangle |1\rangle \\ &|\alpha_{00}|^{2} + |\alpha_{01}|^{2} + |\alpha_{10}|^{2} + |\alpha_{11}|^{2} = 1 \end{aligned}$$

where there is no factorization into the tensor product of two independent qubits. These states are called *entangled*.

### **Measuring multi-qubit systems**

#### If we measure both bits of

$$\alpha_{_{00}} \big| 0 \big\rangle \big| 0 \big\rangle + \alpha_{_{01}} \big| 0 \big\rangle \big| 1 \big\rangle + \alpha_{_{10}} \big| 1 \big\rangle \big| 0 \big\rangle + \alpha_{_{11}} \big| 1 \big\rangle \big| 1 \big\rangle$$

#### we get $|x\rangle|y\rangle$ with probability $|\alpha_{xy}|^2$







## **Classical vs. Quantum Circuits**

- <u>Goal</u>: Fast, low-cost implementation of useful algorithms using standard components (gates) and design techniques
- <u>Classical Logic Circuits</u>
  - Circuit behavior is governed implicitly by classical physics
  - Signal states are simple bit vectors, e.g. X = 01010111
  - Operations are defined by Boolean Algebra
  - No restrictions exist on copying or measuring signals
  - Small well-defined sets of universal gate types, e.g. {NAND}, {AND,OR,NOT}, {AND,NOT}, etc.
  - Well developed CAD methodologies exist
  - Circuits are easily implemented in fast, scalable and macroscopic technologies such as CMOS

## **Classical vs. Quantum Circuits**

- Quantum Logic Circuits
  - Circuit behavior is governed explicitly by quantum mechanics
  - Signal states are vectors interpreted as a superposition of binary "qubit" vectors with complex-number coefficients

$$|\Psi\rangle = \sum_{i=0}^{2^n-1} c_i |i_{n-1}i_{n-1}\dots i_0\rangle$$

- Operations are defined by linear algebra over Hilbert Space and can be represented by unitary matrices with complex elements
- <u>Severe restrictions</u> exist on copying and measuring signals
- Many universal gate sets exist but the <u>best types are not obvious</u>
- Circuits must use microscopic technologies that are slow, fragile, and not yet scalable, e.g., NMR

## **Quantum Circuit Characteristics**

- Unitary Operations
  - Gates and circuits must be reversible (information-lossless)
    - Number of output signal lines = Number of input signal lines
    - The circuit function must be a bijection, implying that output vectors are a <u>permutation</u> of the input vectors
  - Classical logic behavior can be represented by <u>permutation</u> matrices
  - Non-classical logic behavior can be represented including state sign (phase) and entanglement

## **Quantum Circuit Characteristics**

- Quantum Measurement
  - Measurement yields <u>only one state</u> X of the superposed states
  - Measurement also <u>makes X the new state</u> and so *interferes with computational processes*
  - X is determined with some **probability**, implying uncertainty in the result
  - <u>States cannot be copied</u> ("cloned"), implying that signal fanout is not permitted
  - <u>Environmental interference</u> can cause a measurement-like state collapse (decoherence)

### **Classical vs. Quantum Circuits**

Classical adder



#### **Classical vs. Quantum Circuits**

#### Quantum adder









# **Reversible Circuits**

- Reversibility was studied around 1980 motivated by power minimization considerations
- Bennett, Toffoli et al. showed that any classical logic circuit *C* can be made reversible with modest overhead



# **Reversible Circuits**

- How to make a given *f* reversible
  - Suppose  $f: i \rightarrow f(i)$  has *n* inputs *m* outputs
  - Introduce *n* extra outputs and *m* extra inputs
  - Replace *f* by  $f_{rev}$ :  $i, j \rightarrow i, f(i) \oplus j$  where  $\oplus$  is XOR
- Example 1: f(a,b) = AND(a,b) $a = [Reversible] \\ b = [AND] \\ gate \\ c = [f = ab \oplus c] \\ f = ab \oplus c \\ c = [f = ab \oplus c] \\ c = [f \oplus c] \\ c$
- This is the well-known Toffoli gate, which realizes AND when *c* = 0, and NAND when *c* = 1.

# **Reversible Circuits**

• Reversible gate family [Toffoli 1980]



- Every Boolean function has a reversible implementation using Toffoli gates.
- There is no universal reversible gate with fewer than three inputs





# Quantum Gates

- One-Input gate: NOT
  - Input state:  $c_0|0\rangle + c_1|1\rangle$

  - Pure states are mapped thus:  $|0\rangle \rightarrow |1\rangle$  and  $|1\rangle \rightarrow |0\rangle$
  - Gate operator (matrix) is  $\begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}$   $|0\rangle = \begin{pmatrix} 1 \\ 0 \end{pmatrix}$   $|1\rangle = \begin{pmatrix} 0 \\ 1 \end{pmatrix}$

### **Quantum Gates**

#### • **One-Input gate:** "Square root of NOT"

- Some matrix elements are imaginary
- Gate operator (matrix):

– We find:

$$\begin{pmatrix} i/\sqrt{1/2} & 1/\sqrt{1/2} \\ 1/\sqrt{1/2} & i/\sqrt{1/2} \end{pmatrix} = \frac{1}{\sqrt{2}} \begin{pmatrix} i & 1 \\ 1 & i \end{pmatrix}$$

 $\frac{1}{\sqrt{2}} \begin{pmatrix} i & 1 \\ 1 & i \end{pmatrix} \begin{pmatrix} 1 \\ 0 \end{pmatrix} = \frac{1}{\sqrt{2}} \begin{pmatrix} i \\ 1 \end{pmatrix} \text{ so } |0\rangle \rightarrow |0\rangle \text{ with probability } |i/\sqrt{2}|^2 = 1/2$ and  $|0\rangle \rightarrow |1\rangle \text{ with probability } |1/\sqrt{2}|^2 = 1/2$ Similarly, this gate randomizes input  $|1\rangle$ 

– But concatenation of two gates eliminates the randomness!



• One-Input gate: Hadamard

$$\frac{1}{\sqrt{2}} \begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix} \qquad -\mathbf{H}$$

- $\text{ Maps } |0\rangle \rightarrow 1/\sqrt{2} |0\rangle + 1/\sqrt{2} |1\rangle \text{ and } |1\rangle \rightarrow 1/\sqrt{2} |0\rangle 1/\sqrt{2} |1\rangle.$
- Ignoring the normalization factor  $1/\sqrt{2}$ , we can write  $|x\rangle \rightarrow (-1)^{x} |x\rangle - |1-x\rangle$
- One-Input gate: Phase shift



- **Universal One-Input Gate Sets**
- Requirement:

$$|0\rangle - U$$
 Any state  $|\psi\rangle$ 

- Hadamard and phase-shift gates form a <u>universal</u> gate set
- *Example*: The following circuit generates  $|\psi\rangle = \cos \theta |0\rangle + e^{i\phi} \sin \theta |1\rangle$  up to a global factor


# Quantum Gates

• **Two-Input Gate:** Controlled NOT (CNOT)



- CNOT maps  $|x\rangle|0\rangle \rightarrow |x\rangle||x\rangle$  and  $|x\rangle|1\rangle \rightarrow |x\rangle||NOT x\rangle$  $|x\rangle|0\rangle \rightarrow |x\rangle||x\rangle$  *looks like cloning*, <u>but it's not</u>. These mappings are **valid only for the pure states**  $|0\rangle$  and  $|1\rangle$
- Serves as a "non-demolition" measurement gate



• **3-Input gate:** Controlled CNOT (C<sup>2</sup>NOT or Toffoli gate)







• General controlled gates that control some 1qubit unitary operation *U* are useful





#### **Universal Gate Sets**

- To implement any unitary operation on *n* qubits exactly requires an infinite number of gate types
- The (infinite) set of all 2-input gates is universal

   Any *n*-qubit unitary operation can be implemented using Θ(n<sup>3</sup>4<sup>n</sup>) gates [Reck et al. 1994]
- CNOT and the (infinite) set of all 1-qubit gates is universal



## **Discrete Universal Gate Sets**

• The error on implementing U by V is defined as

$$E(U,V) = \max_{\|\Psi\}} \|(U-V)\|\Psi\|$$

- If *U* can be implemented by *K* gates, we can simulate *U* with a total error less than  $\varepsilon$  with a gate overhead that is polynomial in  $\log(K/\varepsilon)$
- A discrete set of gate types G is universal, if we can approximate any U to within any ε > 0 using a sequence of gates from G



## **Discrete Universal Gate Set**

• Example 1: Four-member "standard" gate set



• Example 2: {CNOT, Hadamard, Phase, Toffoli}

# Quantum Circuits

# **Quantum Circuits**

- A quantum (combinational) circuit is a sequence of quantum gates, linked by "wires"
- The circuit has fixed "width" corresponding to the number of qubits being processed
- Logic design (classical and quantum) attempts to find circuit structures for needed operations that are
  - Functionally correct
  - Independent of physical technology
  - Low-cost, e.g., use the minimum number of qubits or gates
- Quantum logic design is not well developed!

# **Quantum Circuits**

- Ad hoc designs known for many specific functions and gates
- Example 1 illustrating a theorem by [Barenco et al. 1995]: Any  $C^2(U)$  gate can be built from CNOTs, C(V), and  $C(V^{\dagger})$  gates, where  $V^2 = U$





#### **Example 1**: Simulation





**Example 1**: Simulation (contd.)



• *Exercise*: Simulate the two remaining cases



**Example 1**: Algebraic analysis



• Is  $U_0(x_1, x_2, x_3) = U_5 U_4 U_3 U_2 U_1(x_1, x_2, x_3)$ =  $(x_1, x_2, x_1 x_2 \oplus U(x_3))$  ?



#### Example 1 (contd);

 $U_{1} = I_{1} \otimes C(V)$   $= \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \otimes \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & v_{10} & v_{11} \end{pmatrix} = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & v_{00} & v_{01} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & v_{00} & v_{01} \\ 0 & 0 & 0 & 0 & 0 & v_{00} & v_{0} \\ 0 & 0 & 0 & 0 & 0 & v_{0} & v_{0} \\ 0 & 0$ 



#### Example 1 (contd);

# **Quantum Circuits**

#### Example 1 (contd);

- $U_5$  is the same as  $U_1$  but has  $x_1$  and  $x_2$  permuted (tricky!)
- It remains to evaluate the product of five 8 x 8 matrices  $U_5U_4U_3U_2U_1$  using the fact that  $VV^{\dagger} = I$  and VV = U

 $|001000000||00100000||00\mathbf{v}_{00}\mathbf{v}_{10}00000||00100000||00\mathbf{v}_{00}\mathbf{v}_{01}0000||00\mathbf{v}_{00}\mathbf{v}_{01}0000||00\mathbf{v}_{00}\mathbf{v}_{01}0000||00\mathbf{v}_{00}\mathbf{v}_{01}0000||00\mathbf{v}_{00}\mathbf{v}_{01}0000||00\mathbf{v}_{00}\mathbf{v}_{01}0000||00\mathbf{v}_{00}\mathbf{v}_{01}0000||00\mathbf{v}_{00}\mathbf{v}_{01}0000||00\mathbf{v}_{00}\mathbf{v}_{01}0000||00\mathbf{v}_{00}\mathbf{v}_{01}000||00\mathbf{v}_{00}\mathbf{v}_{01}000||00\mathbf{v}_{00}\mathbf{v}_{01}000||00\mathbf{v}_{00}\mathbf{v}_{01}\mathbf{v}_{01}000||00\mathbf{v}_{00}\mathbf{v}_{01}\mathbf{$  $(1 \ 0 \ 0 \ 0 \ 0 \ 0$ 0 1 0 0 0 0 0 0 1 0 0 0 0 0 0 1 0 0 0  $| = U_0$ 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0  $\mathbf{v}_{00}v_{00} + \mathbf{v}_{10}v_{10}$   $\mathbf{v}_{00}v_{01} + \mathbf{v}_{10}v_{11}$  $\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & \mathbf{v}_{01} v_{00} + \mathbf{v}_{11} v_{10} & \mathbf{v}_{01} v_{01} + \mathbf{v}_{11} v_{11} \end{bmatrix}$ 



- Implementing a Half Adder
  - *Problem*: Implement the classical functions  $sum = x_1 \oplus x_0$  and  $carry = x_1 x_0$
- Generic design:



# **Quantum Circuits**

• Half Adder. Generic design (contd.)



• Half Adder. Specific (reduced) design



## Walsh Transform for two binary-input many-valued variables

### Classical logic

Quantum logic





Butterfly is created automatically by tensor product corresponding to superposition

# **Portland Quantum** Logic Group (PQLG) What we do?

## **People at PSU and collaborators**

- Marek Perkowski
- Martin Zwick
- Xiaoyu Song
- William Hung
- Anas Al-Rabadi
- Martin Lukac
- Mikhail Pivtoraiko
- Andrei Khlopotine
- Alan Mishchenko (University of California, Berkeley, USA)
- Bernd Steinbach (Technical University of Freiberg, Germany)
- Pawel Kerntopf (Technical University of Warsaw, Poland)
- Mitch Thornton (Southern Methodist University, Dallas, USA)
- Lech Jozwiak (Technical University of Eindhoven, The Netherlands)
- Andrzej Buller (ATR, Kansai Science City, Japan)
- Tsutomu Sasao (Kyushu University of Technology, Iizuka, Japan).

# **Current Projects**

- Logic Synthesis for Reversible Logic
  - decomposition
  - Decision Diagram Mapping
  - composition
  - regular structures lattices, PLAs, nets
- Logic Synthesis for Quantum Logic
- Quantum Simulation using new Decision Diagrams



paper

submitted

# **Current Projects**

- FPGA-based model of Quantum Computer
- Reversible FPGA using CMOS.
- Realization of new spectral transforms using quantum logic.
- Non-linear Quantum Logic solves NP problems in polynomial time.
- Quantum-inspired search algorithms for robotics

## Where to learn more

- Web Page of Marek Perkowski
  - class 572 see description of student projects
  - Portland Quantum Logic Group



**Automated Synthesis of Generalized Reversible Cascades using Genetic** Algorithm



- Introduction and history
- Reversible Logic and Reversible Gates
- Genetic algorithms
- The Model
- Simulation
- Conclusion

# **Reversible gates...**

Feynman, Toffoli, Fredkin, ...

$$A \longrightarrow P = A$$
$$B \longrightarrow Q = P \oplus$$

Mapping of I/O allows unique (P,Q)⇒(A,B)

## and Reversible Circuits

•To reduce the RL synthesis limitations one can insert constants in order to modify the functionality

B

## **Generalized Reversible Gates**





# **Perkowski gates family**





- Mixed data/control inputs (generalized complex control gates)
- *All* :
- ESOP
- Factorized-ESOP
- MV Complex Terms
- XOR family

#### Example:



# **Genetic algorithms**



# **Encoding & operations**



C-O



## **Circuit Encoding**



## **GA's settings**

- Stochastic universal sampling
- Fitness:

$$F_i = \frac{1}{1 + error_i} - \Lambda_i$$

Error:

$$error = \sum_{i=1}^{n} \sum_{j=1}^{2^{n}} |U_{ij} - S_{ij}| \quad S, U \in U(2^{n})$$

Error evaluation:

-comparison outputs / LUT -Permutations of all constants and inputs

- -Normalization of error by wires and patterns
- -Penalization for length

LUT for Fredkin gate:

А, В,	A'	B,	С'
D			
000	0	0	0
001	0	0	1
010	0	1	0
011	0	1	1
100	1	0	0
101	1	0	1
110	1	1	1
111	1	1	0



Mutation	Gates Blocks	Position (block/circuit)
Cross-Over*	Segments	Experimental (unitary matrices)
Reproduction	Circuits	Best gates Best Circuits

\* - for circuits having only same number of I/O

# **Experimental settings**

- Each input is equivalent with any other
- Evolving new circuits by recombination
- Non specific conditions
- Population 100-150
- Mutation = 0.01 1
- Crossover = 0.3 0.8
- Specifications:
  - Genetic operations based on RCB > minimal element
  - The noise in these experiments is not only a mutation but an random operator on random blocks !!!

Number of wires	Gates
1	Wire, Inverter
2	Feynman, Swap
3	Fredkin, Toffoli
4	Margolus


### -No starting set restriction

-Mutation only on blocks



#### Unitary gate search

# of	Number	Number of	Real	Real
inputs	of	generations	gate	Time
	individu		found	
	als			
2	10/50	10/1	*	<1 Min
3	10/50	10/1	*	<1 Min
4	10/50	10/1	*	<1 Min

### Random function search

# Improvements

- Using min(ESOP( $F \oplus G$ )) for fitness
- Lamarckian learning
  - One genotype  $\Rightarrow$  multiple possibilities of phenotype
  - Using to minimize Exorcism-4

## **Circuit search**

-Starting set restriction

-Mutation all levels (0.01 - 0.1)

Circuit/Gate	# of Gen.	R.T.	Exact/s imilar
Toffoli	5/1	0	*/*
Fredkin	5/1	0	*/*
Adder	?/200,000	120 sec	0/*





- Ideas:
  - Using GA to evolve arbitrary Reversible Circuit
  - Specific Encoding helps the evolution
  - Alternative encoding presented
- Future works:
  - Apply Lamarckian GA and other new variants of evolutionary approaches
  - Create hybrid algorithms by mixing evolutionary and logic-symbolic methods
  - Use new representations such as permutations and decision diagrams
  - Use Logic minimizer to minimize the ESOP expression of the circuit
  - THIS IS WORK IN PROGRESS, EVERYBODY IS WELCOME TO JOIN.
  - Publishing