SIGNAL PROPAGATION

FROM ONE SOURCE TO MANY SINKS

A

AND

XOR

AND

AND

Signal line - FANOUT = 3

B

Signal Line - BUS LINE

Signal Driver - Single Source

Many Sinks

Signal Buffer - Single Sink
SIGNAL PROPAGATION

FROM ONE SOURCE TO MANY SINKS

A

Signal line - FANOUT = 3

B

BUS LINE

Signal Driver -
Single Source

Many Sinks

Signal Buffer -
Single Sink
SIGNAL PROPAGATION

FROM MANY SOURCES TO ONE SINK

signal 1

MUX

common signal line

signal N

Select signal
SIGNAL PROPAGATION

FROM MANY SOURCES TO ONE SINK

FROM MANY SOURCES TO MANY SINKS
TriState Buffer Concept

Switch model of a multiplexer

- signal 1
- signal N
- signal line
- select decoder
- Mutually exclusive select signals
- Binary select signal
TriState Buffer Concept

Switch model of a multiplexer

signal 1

signal N

Mutually exclusive select signals

select decoder

Binary select signal

TRISTATE buffer signal drivers - a DISTRIBUTED MULTIPLEXER

sig 1  sel 1  sig 2  sel 2  sig N  sel N

Mutually exclusive select signals
**TriState Buffer**

**SYMBOLS**

![Symbol diagram]

**SWITCH MODEL**

<table>
<thead>
<tr>
<th>OE</th>
<th>in</th>
<th>out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Z</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Z</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

$Z$ = High Impedance
output not connected to input

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TriState Buffer

SYMBOLS

SWITCH MODEL

OE - output enable
TriState Buffer

SYMBOLS

in → out
OE

in → out
OE

in → out
OE

in → out
OE

in → out
OE - output enable

SWITCH MODEL

CMOS IMPLEMENTATION

in

OE

Vdd

out

OE

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UNIDIRECTIONAL BUS LINE

Propagation from many sources to many sinks

signal 1
signal N

Mutually exclusive select signals

BUS line

signal 1 signal N

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UNIDIRECTIONAL BUS LINE

Propagation from many sources to many sinks

Mutually exclusive select signals

TriState Signal Drivers

signal 1

signal 2

TriState Signal Buffers

signal 1

signal 2
BIDIRECTIONAL BUS LINE

Mutually exclusive select signals

OE 1 = 1
source 1

OE n = 0
sink n
BIDIRECTIONAL BUS LINE

OE 1 = 0
sink 1

Mutually exclusive select signals

OE n = 1
source n
WIRED LOGIC

TRANSISTORS WORK AS INVERTERS

OPEN COLLECTORS NEED PULL_UP RESISTORS
WIRED LOGIC BUS

signal 1
select 1

signal N
select N

F1 AND F2

F1 selected

<table>
<thead>
<tr>
<th>sel1</th>
<th>sig1</th>
<th>F1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
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</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
REGISTER FILE

Di0  Do0

Di1  Do1

Di2  Do2

Di3  Do3

word 0
REGISTER FILE

Di0  Do0  Di1  Do1  Di2  Do2  Di3  Do3

D  Q
EN

word 0

Di0  Do0  Di1  Do1  Di2  Do2  Di3  Do3

D  Q
EN

word 1

D  Q
EN

D  Q
EN

D  Q
EN

D  Q
EN
REGISTER FILE

word select decoder

word 0

D  Q
EN

D  Q
EN

D  Q
EN

D  Q
EN

word 1

D  Q
EN

D  Q
EN

D  Q
EN

D  Q
EN

MUX

MUX

MUX

MUX

MUX
MEMORY ELEMENTS

THE BASIC ELEMENT IS A STATIC LATCH THAT HOLDS THE STORED VALUE AS LONG THE POWER IS ON.
MEMORY ELEMENTS

STATIC MEMORY CELL

READ WRITE CIRCUITRY
(conceptual view)
MEMORY ARRAY

D0  !D0  

word select

D1  !D1

Column select

Do0  Di0

D2  !D3

Column select

Do1  Di1

Do2  Di2

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RAM - Random Access Memory

- Each word in the RAM memory can be read by giving its address and observing the data lines after some time.
- Each word can be re-written by giving its address, presenting the new data and keeping it stable for some time.
- Addressing can be random (there are no requirements for any sequence in addresses) - hence Random Access Memory.
- Storage matrix is usually very large and organized as a square matrix of word cells.
What have we learnt?

- TriState buffers allow to connect many signal sources to the same signal line. Wired logic can provide the same functionality although is less popular.

- Flip-flops can be organized in registers, registers in register files.

- RAM - Random Access Memory allows to read/write data at a randomly chosen address.