A List of Topics to be Tested in Mideterm Exam

The exam is on April 22, Tuesday.
This is open book, open notes exam.

There will be a review of all these subjects before the exam.

Other material discussed in class, from a book, or during additional meetings will be not tested. It will be possibly covered by the Final Exam.

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1. Karnaugh Maps, Boolean Logic, Boolean Algebra, De Morgan theorems. Logic Factorization of AND/OR and AND/EXOR logic. NAND and NOR gates.
2. Minimization of two level AND/OR and AND/EXOR circuits. The concept of PLA and PAL.
3. Covering problem and the methods of solving it. Petrick Function. Recursive tree paradigm and its use to solve the Petrick function.
4. Tautology and Satisfiability. Use of recursive tree paradigm.
5. Even-odd covering problem and its use in ESOP minimization.
6. Rules for simplifying EXOR logic circuits
7. Analysis of Exor-based circuits using even-odd covering in Kmaps.
8. Shannon, Positive Davio and Negative Davio expansions and their uses.
9. Binary Decision Diagrams, definitions, how to create, applications.
10. Kronecker Functional Decision Diagrams.
11. How to find a circuit from such diagram
12. What is the meaning of a branch (path) in a diagram.
13. Use of diagrams in ESOP synthesis.
14. The role of complemented inputs, use in synthesis of circuits.
15. Linear and non-linear preprocessors for Decision Diagram based circuits.
16. Shannon and Kronecker Lattices.
17. Basic concept of reversible logic and reversible gate.
18. Feynman, Toffoli, Fredkin gates and their quantum notation.
19. Pseudo-Kronecker Diagrams and Lattices and their use to minimize reversible circuits.
20. Naïve method of synthesizing reversible logic by converting from AND/OR/NOT based circuit. Introducing constants and garbages.
21. The concept of global and local mirrors, inverse gates and their uses. What are the inverse gates of Toffoli, Feynman and Fredkin gates. You should be able to find an inverse gate to any given gate. The concept of spy circuit.
22. Billiard Ball Model of computing. Conservative gates.
23. Concept of cascades. Reversible cascades. Width of circuit, use of global and local mirrors, input constants, cost of garbages. Other structures of circuits.
24. Linear circuits, how to recognize linear Boolean function and how to minimize it. Use of EXOR and Feynman gates. Why linear circuits are not sufficient.

25. How to convert an arbitrary circuit to a reversible circuit (using Kmaps, truth tables or networks).
26. Example – Gray to Binary and Binary to Gray code converters. Any other code converters in EXOR logic.
27. Realization of adders and code converters using reversible logic.
28. Advanced reversible gates, Margolus, Kerntopf, multi-input gates and generalizations of basic gates. The concept of cofactors of a function (gate) and its uses.
29. Reusing of sub-functions in reversible synthesis – examples are Adder and Miller gate.
30. Reversible circuit as a set of permutations, use of this representation in synthesis.
31. What are balanced functions? How are they used?
32. Realization of gates from other gates, for instance swap from Feynman, Feynman from Swap (can it be done?), Margolus from Fredkin, Fredkin from Toffoli, Toffoli from Fredkin, etc.
33. The concept of Positive Polarity Reed Muller (PPRM) circuit. Its canonicity, conversion from Kmap to PPRM.
34. The concept of Fixed Polarity Reed Muller Form. The concept of polarity of a FPRM for a Boolean function and its use.
35. Symmetric functions. Symmetry indices. Recognition of symmetric functions on Kmaps. Synthesis of incomplete functions as symmetric functions. Use of lattices to realize symmetric functions. Use of lattices to realize non-symmetric functions.
36. Multi-valued logic. Post, Generalized Post and Universal literals and gates. MIN and MAX gates. Modulo Addition gates. Ternary logic as an example. Maps for ternary logic and synthesis of MAX of MIN functions from such maps.
37. Examples of other ternary gates.
38. The concept of controlled reversible gate. Examples of controlled gates.
39. The concept of generalized multi-input reversible gate. Composing of complex gates.
40. The transformational method to prove equivalence and simplify reversible circuits.
41. Role of swap gates and transformation from a general (non-planar) reversible circuit to quantum notation circuit (planar).
42. Synthesis of reversible circuits using factorization
43. Synthesis of reversible circuits using composition
44. Search from inputs to outputs, from outputs to inputs and mixed (bidirectional search).
45. Synthesis of reversible circuits using levellized expansions and lattices, especially for incompletely specified multi-output functions.
46. Finite State Machines. Transition graphs, tables. Synthesis using D Flip-Flops. Analysis and synthesis of machines. Autonomous and non-autonomous machines, Mealy, Moore and Rabin-Scott machines.
47. Non-deterministic Finite State Machines and conversion of a non-deterministic to deterministic machine in reachability analysis. Complexity.
48. Probabilistic Finite State Machines.
49. Uniform (one-hot-coded) circuit realization of deterministic, probabilistic and non-deterministic state machines.

50. Synthesis of standard and reversible iterative circuits. Comparator, MAXIMUM, sequence detection, sequence filtering. Use of Mirrors.
51. Stack Automata and languages.
52. Turing and Post Machines. The concept of Universal Post (Turing) Machine. Machines for adding and copying as examples.
53. The concept of canonicity.
54. Universal logic systems, how to check if the system is universal. Examples.
55. Cellular Automata and reversible cellular automata, one-dimensional, two-dimensional (Game of Life and generalizations), three dimensional. Examples, image processing, shifter, GAPP, other.
56. Genetic Algorithm.
57. Search algorithms, Dept First, Breadth First and A* Search. Strategies and heuristics.
58. Branch and Bound and backtracking.
59. Hamiltonian Path, shortest path, Traveling Salesman, graph coloring, maximum clique and graph coloring problems as examples of combinatorial optimization and decision problems and the respective algorithms.
60. Neural Nets and evolvable Neural Nets. Realization using Cellular Automata.
61. Multi-valued reversible logic. Feynman, Toffoli, 1*1 gates, Conditional gates, and their use in synthesis.
62. Quantum logic notation (matrix notation) for permutation logic, both binary and ternary.
63. Use of matrix multiplication and Kronecker (tensor) multiplication for reversible circuit analysis. Use of swap gate to convert a circuit to parallel/serial form. The problem of reversible circuit synthesis as an inverse problem to analysis problem (composition versus decomposition)