ECE 715
Introduction to VLSI
Prof. Andrzej Rucinski

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ECE 715 - Introduction to VLSI

Credits: 4.00

- Principles of VLSI (Very Large Scale Integration) systems at the physical level
- CMOS circuit and logic design,
- CAD tools,
- CMOS system case studies
- + building working? Chips!

Organizational Issues

- Course Schedule Website:
  - http://www.ece.unh.edu/courses/ece715/classes.htm
- **Topics:**
  - **CMOS technologies**
  - **VLSI system design principles**
  - **Computer Aided Design tools (Mentor Graphics suite)**
  - **Technology Migration (from FPGA into ASIC)**
  - **Integrated circuits manufacturing**
  - **VLSI technologies constraints**
  - **VLSI testing**
- Text:
  - Neil Weste and David Harris, CMOS VLSI Design - A Circuits and Systems Perspective, Addison Wesley, 2005.

Calendar

Date	Topic & Reading Assignment	Homework/Lab Assignment
Aug.29	Getting Started Course Organization (Dr. Kochanski)	
Aug.31	CAD Environment (Frank Hludik), Tutorial1 Tutorial2	Lab One , Lab Two Assigned
Sept. 5	Lab Overview (Frank Hludik),	
Sept. 8	Project Overview (Dr. Kochanski), *Chapter 8. Design Methodology and Tools*	Lab #1 Due, Lab Three Assigned,
Sept. 12	Project Details VLSI Design Philosophy, *Chapter 2. MOS Tarnsistor Theory, Page 67 - 108*	
Sept. 14	Review of nMOS Fundamentals	Lab #2 Due
Sept. 19	Student Project Proposal	
Sept. 21	Review of CMOS Fundamentals	Lab #3 Due, Homework #1 Assigned
Sept. 26	Logic Design, *Chapter 6. Combinational Circuit Design, Page 319 – 378, Chapter 7. Sequential Circuit Design, Page 383 - 475*	
Sept. 28	Logic Design (Continued)	Lab #4 Due
Oct. 3	Labs and Project Review (project leaders)	Lab Four ,Assigned, Homework #1 Due
Oct. 5	Boundary scan, seminar by CJ Clark, Intellitech Corp.	Lab #5 Due, Homework #2 Assigned
Oct. 9	Columbus Day – no classes	

Calendar

Date	Topic & Reading Assignment	Homework/Lab Assignment
Oct. 17	Design Rules, *Page 125 – 136*	
Oct. 19	Simple Layout Examples	Homework #2 Due
Oct. 24	Preliminary Design Review	Reverse Engineering Problem Assigned
Oct. 26	System Design, *Chapter 10. Datapath Subsystems*	Lab Exercise Five Assigned
Oct. 31	System Design (Continued)	
Nov. 2	Floorplanning	
Nov. 7	Performance Characterization, *Chapter 4. Circuit Characterization and Performance Estimation*	Reverse Engineering Problem Due
Nov. 9	Performance Characterization (Continued)	
Nov.14	Scaling, *Page 239 - 266*	
Nov.16	Critical Design Review	
Nov.21	Manufacturing, *Chapter 3. CMOS Processing Technology -- Guest Lecture?*	
Nov.23	Thanskgiving	-
Nov.28	« From Sand to Circuit « Video	
Nov.30	Testing, and Testability, *Chapter 9. Testing and Verification*	
Dec.5	Field trip	
Dec. 7	Boundary Scan, *Page 609 - 636*	
Dec.11	Final Design Review	

ECE-715
09/12/06-tpk

- Systems Engineering – what is a system
- Methodology – getting from a problem to a solution
- Test & Evaluate
- Example from past
- 2006 Fall Problem
- Prof R. Returns -- the real course begins

Systems Engineering

- What is a System?
  - Organized collection of interconnected elements arranged for one or more purposes
- Systems Engineering:
  - Process and discipline of analyzing, designing, implementing and applying systems to solve specific problems
    - Typically focused on systems with substantial complexity

Methodology of Systems Engineering

1. Define Problem[s]
    1. Identify Key System Requirements
2. Propose Conceptual System
    1. Test & Evaluate CS to meet KSR
3. Analyze Implementation Technologies
4. Identify Preferred Implementation
    1. Have a Plan B
    2. Develop Budgets for all resources
    3. Develop realistic implementation schedule
    4. Test and Evaluate to meet KSR

Methodology of Systems Engineering cont.

5. Implement Prototype System
    1. Detailed Design [HW, SW, FW]
    2. Test & Evaluate PS to meet KSR
6. Re-evaluate Problem to confirm KSR
7. Revise System Design based on T&E of PS
8. Identify Preferred Implementation
    1. Have a Plan B
    2. Develop Budgets for all resources
    3. Develop realistic implementation schedule
    4. Test and Evaluate to meet KSR

Methodology of Systems Engineering cont 2.

9. Implement Operational System
    1. Detailed Design [HW, SW, FW]
    2. Test & Evaluate OS to meet revised-KSR
10. Re-evaluate Problem to re-confirm KSR
11. Operational Testing
12. Finalize Documentation
    1. Present your wok

Importance of Testing, Documentation and Planning

- Can't Test too much
  - Develop test plan as early as possible
  - Testing should be ready at each stage of development
  - Testing should be based on real-world as much as possible
- Documentation should parallel design and testing
- Planning should be updated based on testing and changing requirements

Past Projects

- Fast Fourier Transform (2005)
- Biometrics Memory (2004)
- DES Encryption/Decryption (2003)
- Analog Boundary Scan (2002)

FAST FOURIER TRANSFORM COMPONENTS

- 2005 **PROJECT GOAL**
  - This project is a continuation of an effort initiated a few years ago based on the hardware part of the pattern recognition application developed by FPR Corp.

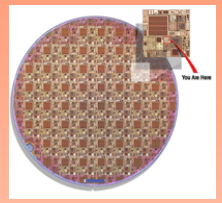
2005 FFT Project

- **Multiplier** A 16 bit complex multiplier; a synchronous multiplier triggered on a rising edge of the system clock. Different multiplier algorithms are acceptable provided that they obey the general specifications listed under the **Project Goal**.
- **Adder** A 16 bit adder; see requirements for multiplier
- **Butterfly** Radix – 4 butterflies – a basic building block for an FFT algorithm - consists of multipliers, adders and a twiddle factor memory
- **Input/ Output Interface**
  - FFT algorithm requires the entire sequence of input samples to be provided on its input port in order to initiate the operation. The input interface should capture all input samples and order it in a way specified for a chosen FFT algorithm. After the entire sequence is collected and properly ordered, the input interface should generate a START signal indicate that data are ready for processing. Similar (but reversed) operation should be performed on the output of FFT. DONE signal indicating completion of processing should be followed by data on the following 16 rising edges of the clock.

2005 Project Description

- The course project: ASIC/VLSI for biometric purposes using AMI 0.5µ technology (2003 - To Be Determined)
- (2005/2006) Implementation 16 point radix 4 FFT Library :
  - 4point FFT
  - Complex Multiplier
- 7 designs have been developed by a team of students of two, each group is responsible for design and implementation of a VLSI subsystem

Fast Fourier Transform Components – 4 point FFT



–Final Design Review – Dec. 12

–Team Leader: Luo Yifei
–Team Member: Tomasz Jankowski

–Course : ECE 715/815 -VLSI
–Partners: Mosis, GigaIC

Project Definition

- Description
  - The purpose of the project is to develop a library of components for a 4 point FFT algorithm
- Specifications
  - suggested clock speed: 100 MHz (note: if the speed of 100 MHz can not be achieved in AMI05 technology then a lower frequency is acceptable)
  - algorithm radix-4
  - arithmetic: 16 bit fixed point, 2's complement
  - complex arithmetic operations should be divided into smaller tasks (pipelining) if the assumed target frequency could not be achieved otherwise
  - All control and status signals should follow the same standard
  - All components should have a clock input (CLK), reset (RST)
  - Arithmetic operators should contain a status line (OVFL) indicating whether an overflow has occurred
  - The cooperation among the design teams is encouraged!!!

Implementation Project Team

Project Leader
Team 1 Leader
Team 1
Team 1
Team 2 Leader
Team 2
Team 3 Leader
Team 3
Team 4 Leader
Team 4
Team 5 Leader
Team 5
Team 6 Leader
Team 6
Team 7 Leader
Team 7

- Tomasz Jankowski tmj@unh.edu
- Mike Fucillo fuccillo@cisunix.unh.edu
- Chuck Deloid cdeloid@cisunix.unh.edu
- Travis Boucher travisb@cisunix.unh.edu
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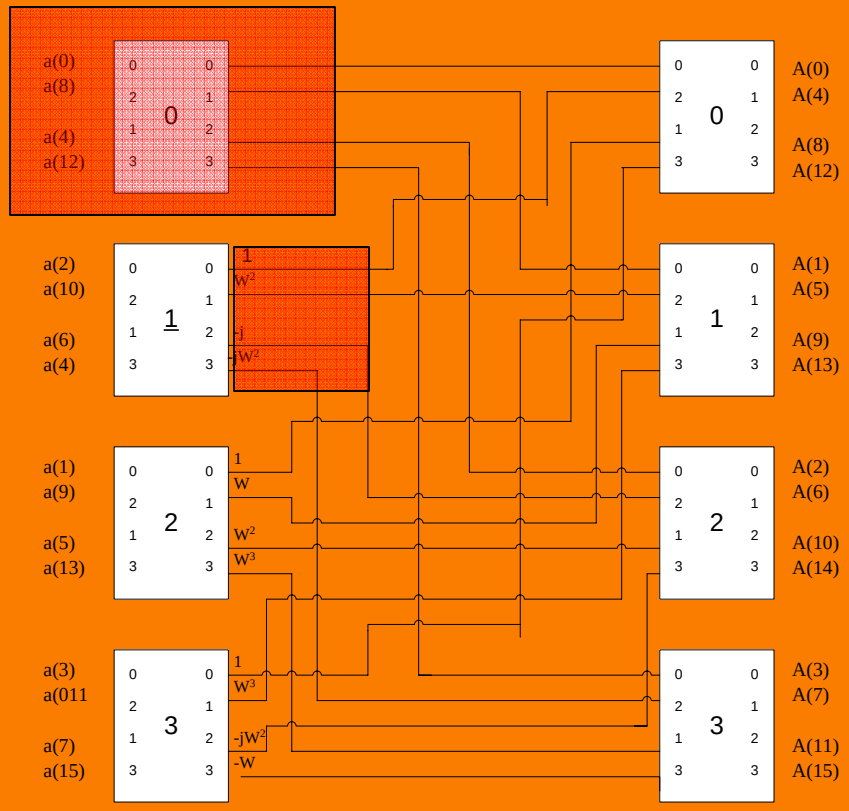
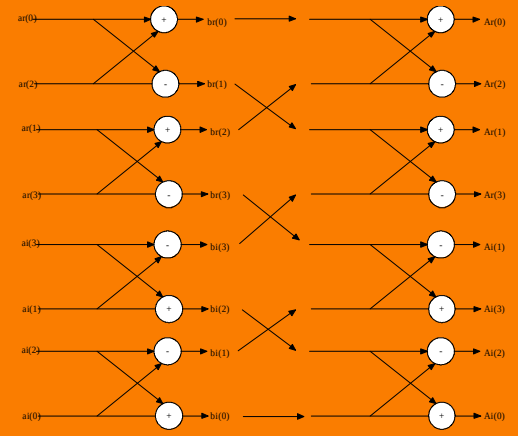
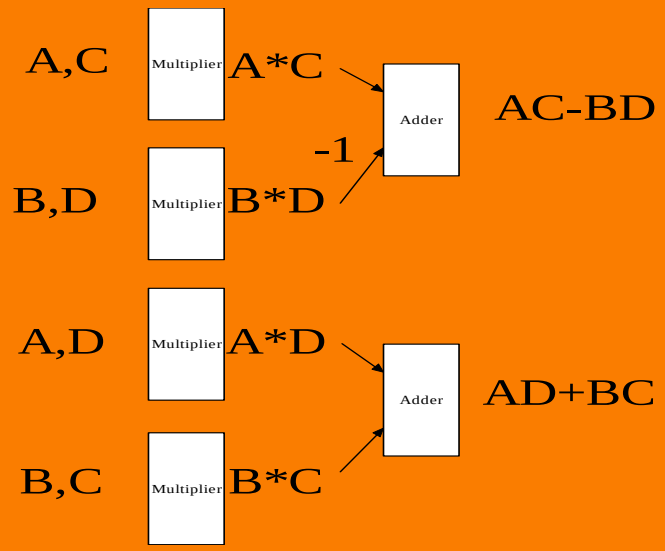
- Kevin Arruda karruda@cisunix.unh.edu
- Scott Crawford sac7@unh.edu
- Jon Oppelaar jeo@cisunix.unh.edu
- Tri Le tl9830@gmail.com
- Ellie Dagher edagher@unh.edu
- Luo Yifei lgo2@unh.edu
- Tomasz Jankowski tmj@unh.edu

Components

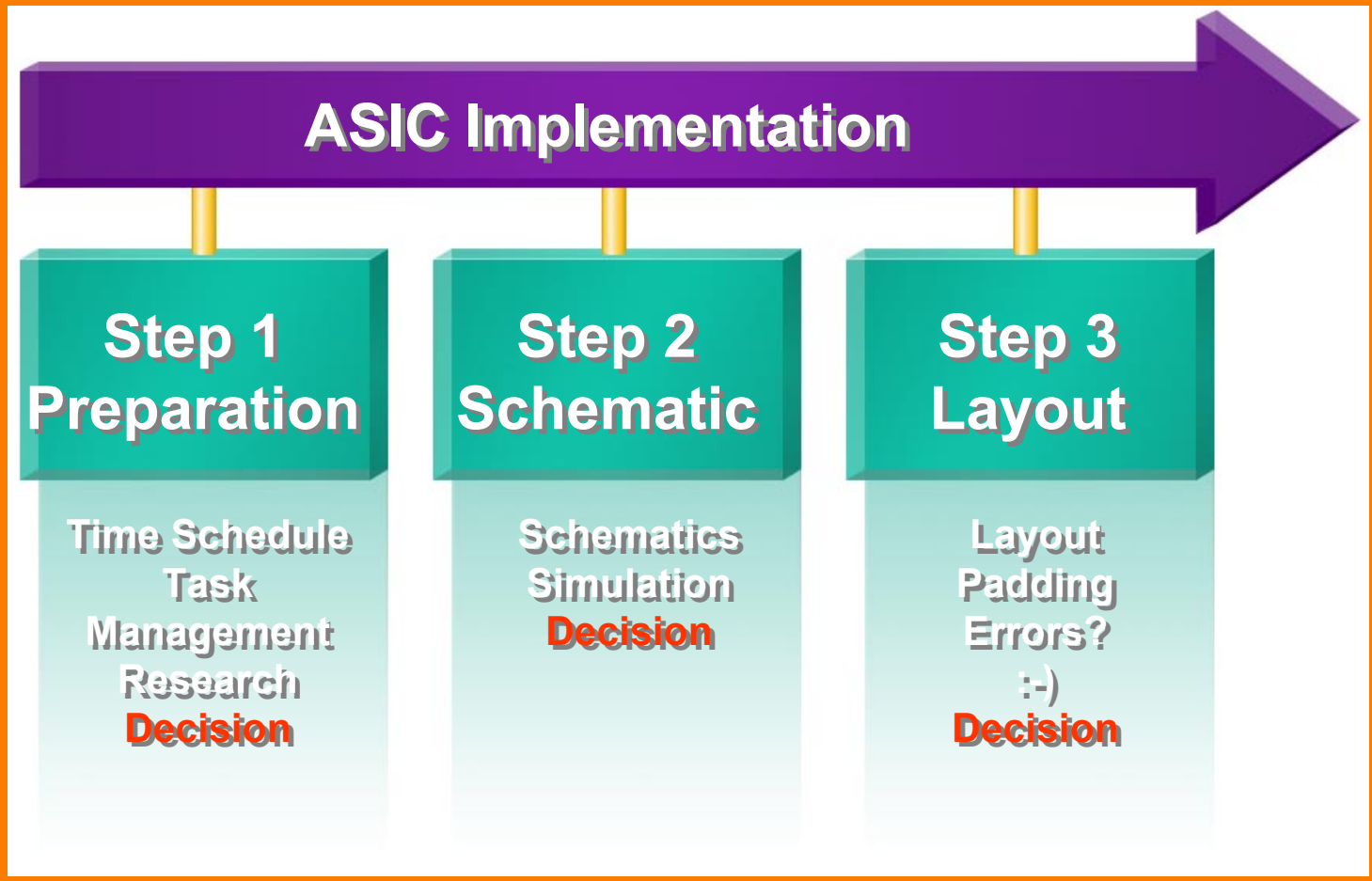
FFT 4-point + Complex Multiply







Methodology

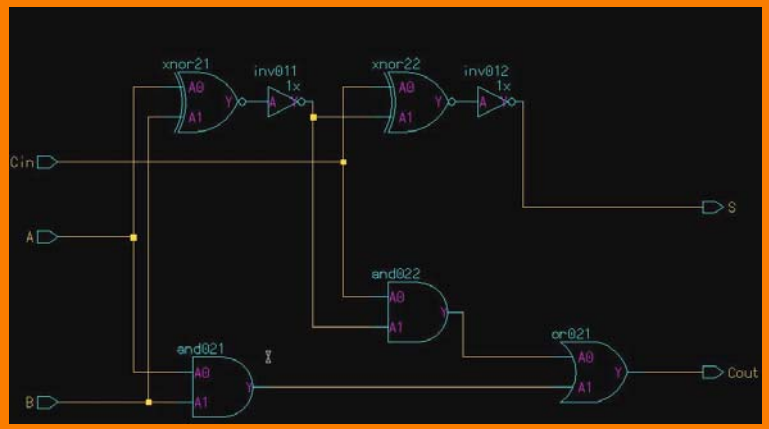


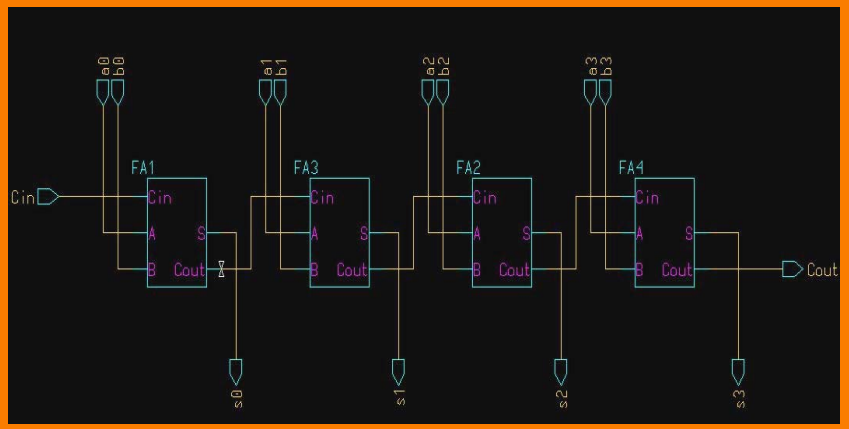
Project Schematics

- Design components

- 4 bit Adder
- 4 bit Subtractor
- 16 bit Register
- 16 bit Output

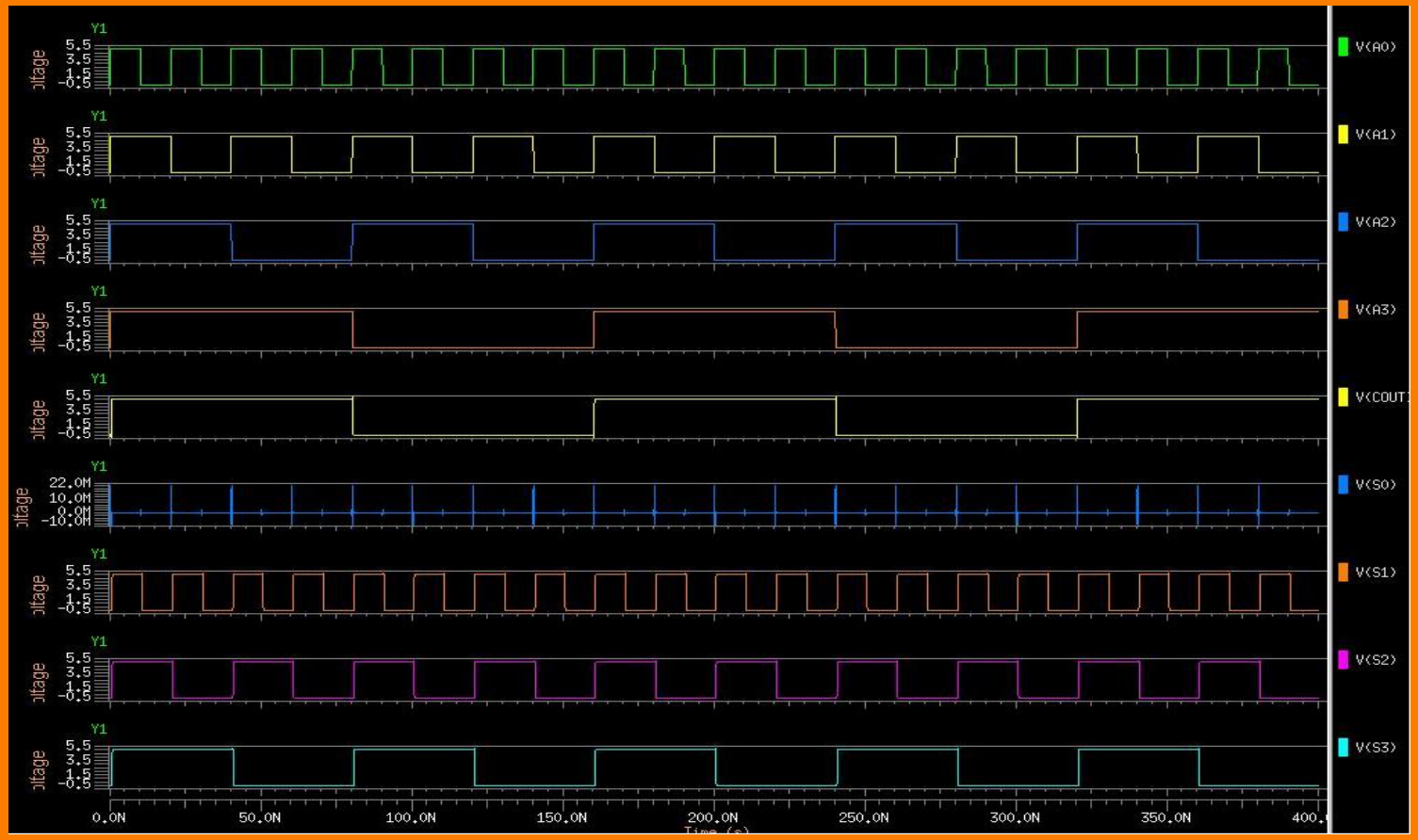
- 4 bit Adder





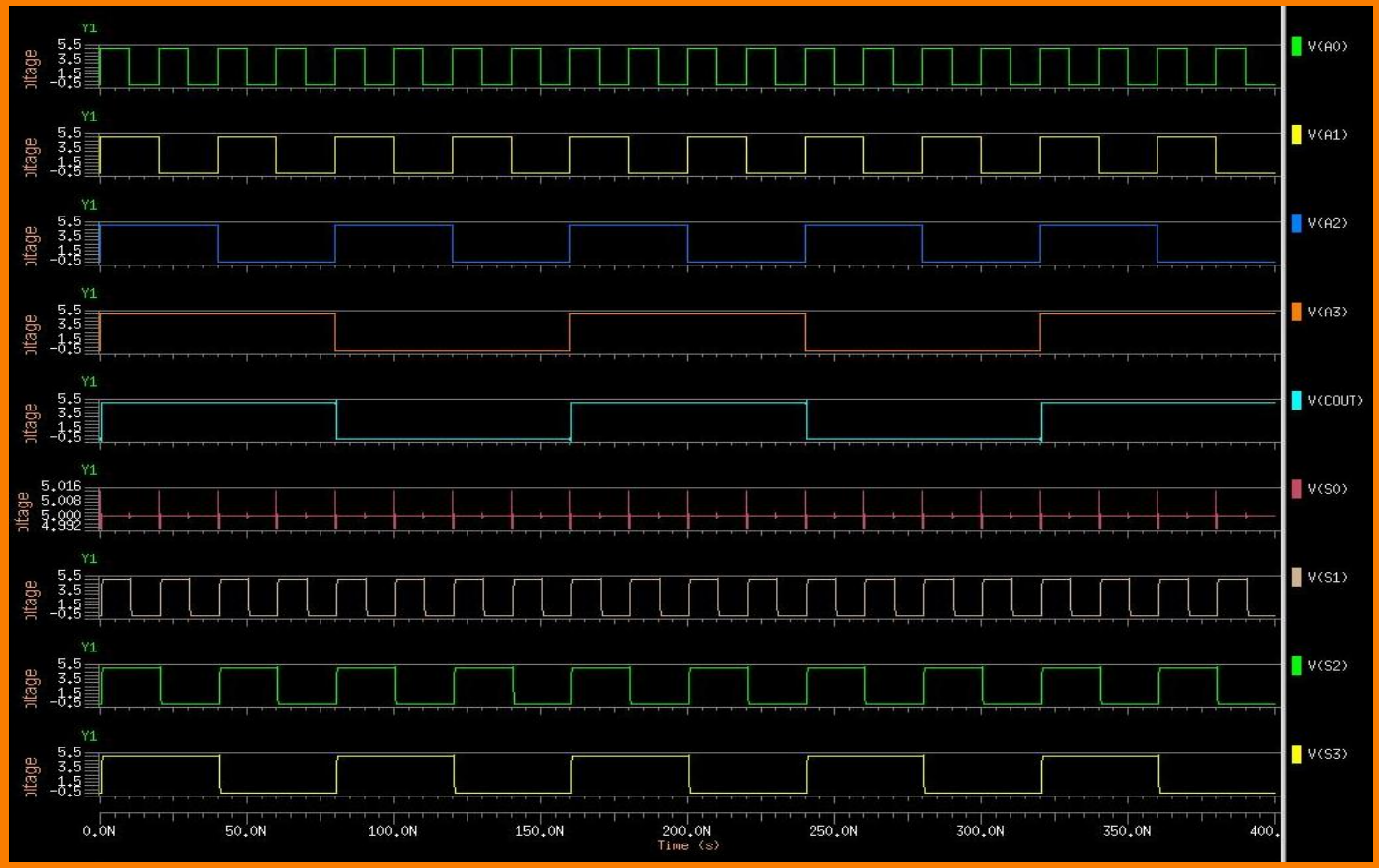
Simulation Waveforms

- 4 bit adder with Cin=0



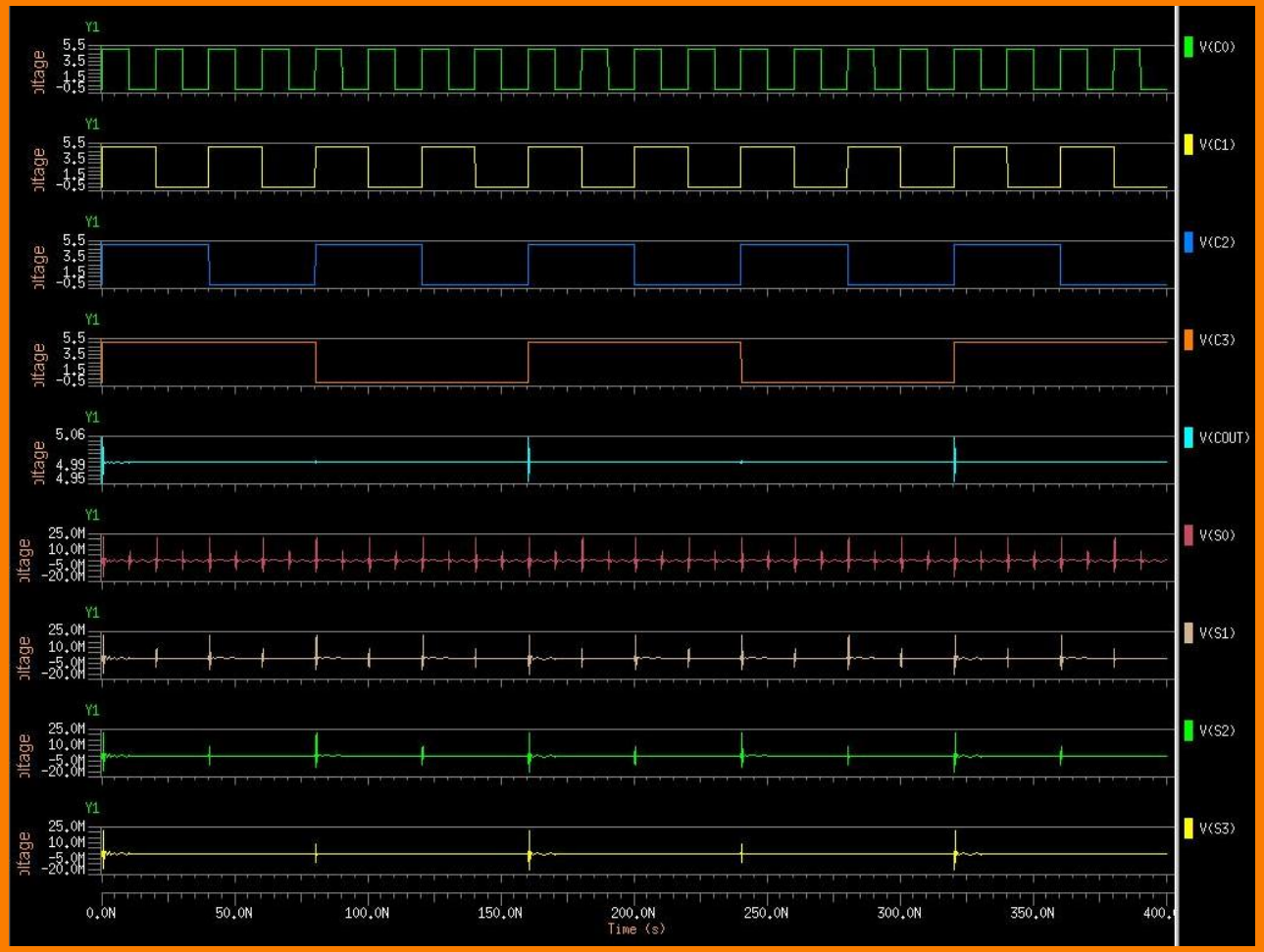
Simulation Waveforms

- 4 bit adder with Cin=1



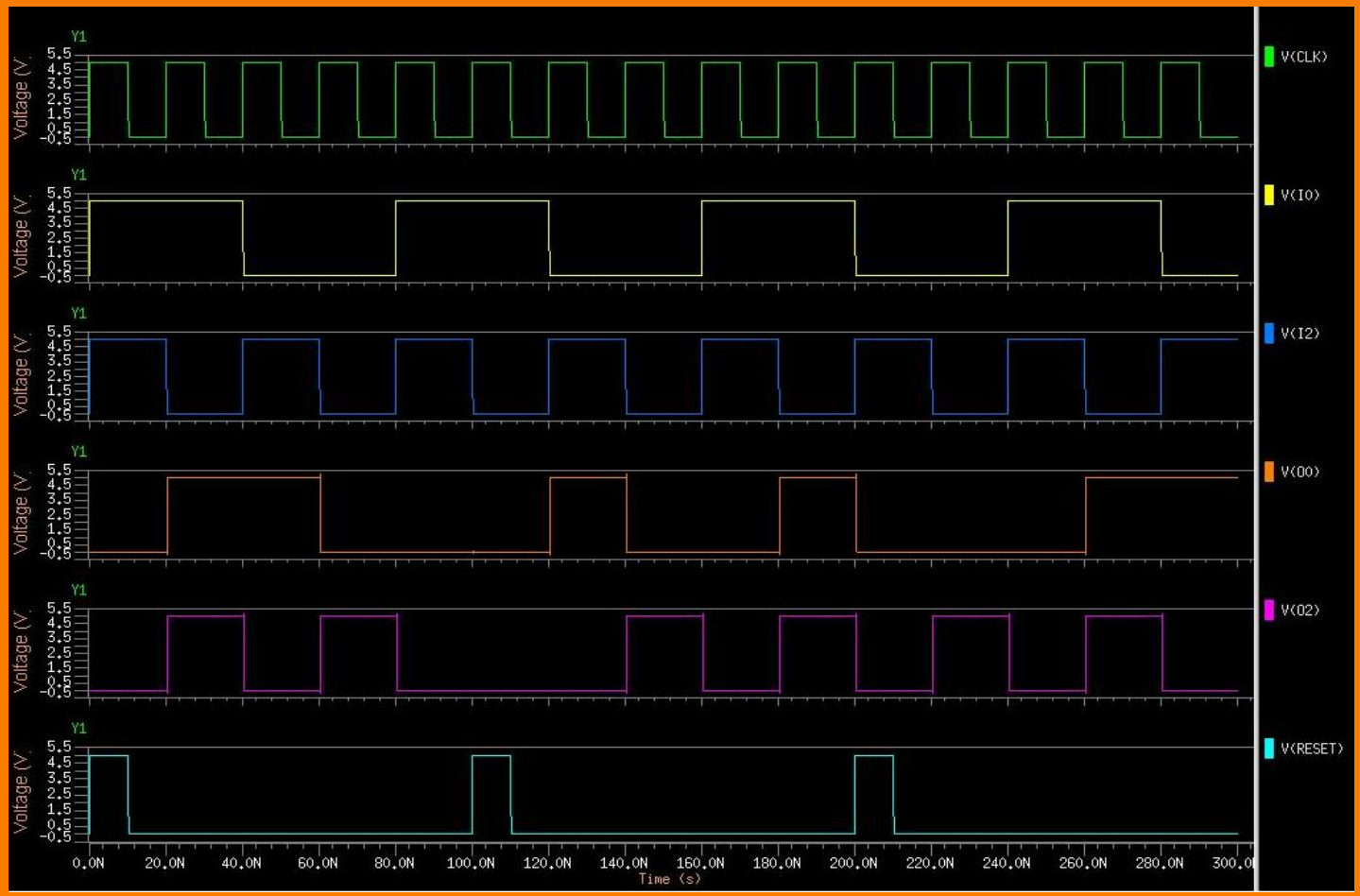
Simulation Waveforms

- 4 bit Subtractor



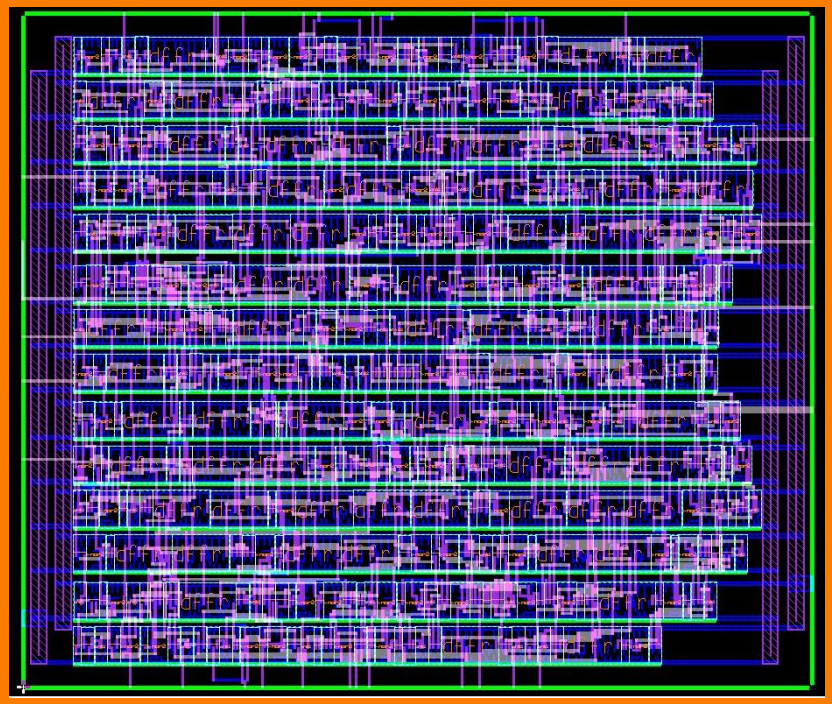
Simulation Waveforms

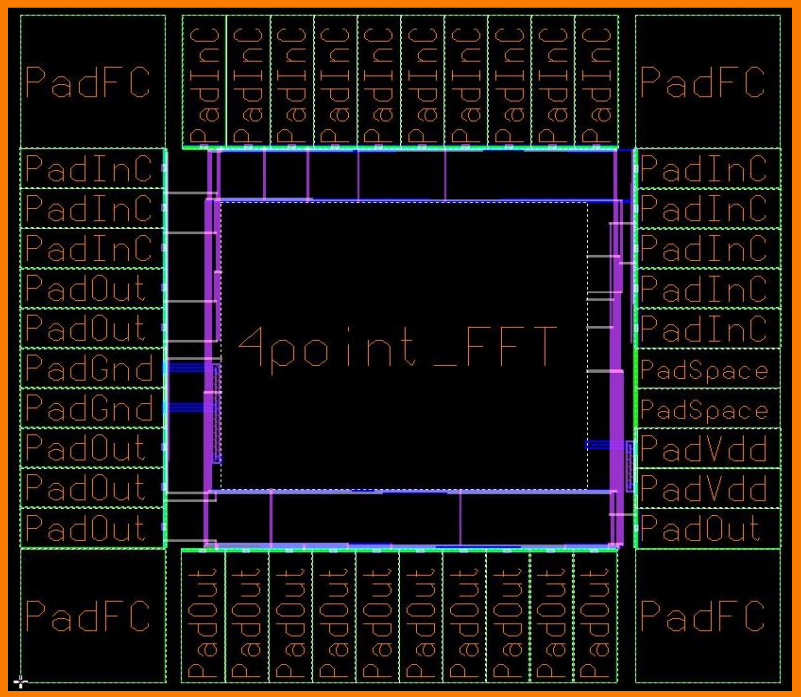
- 16 bit Register



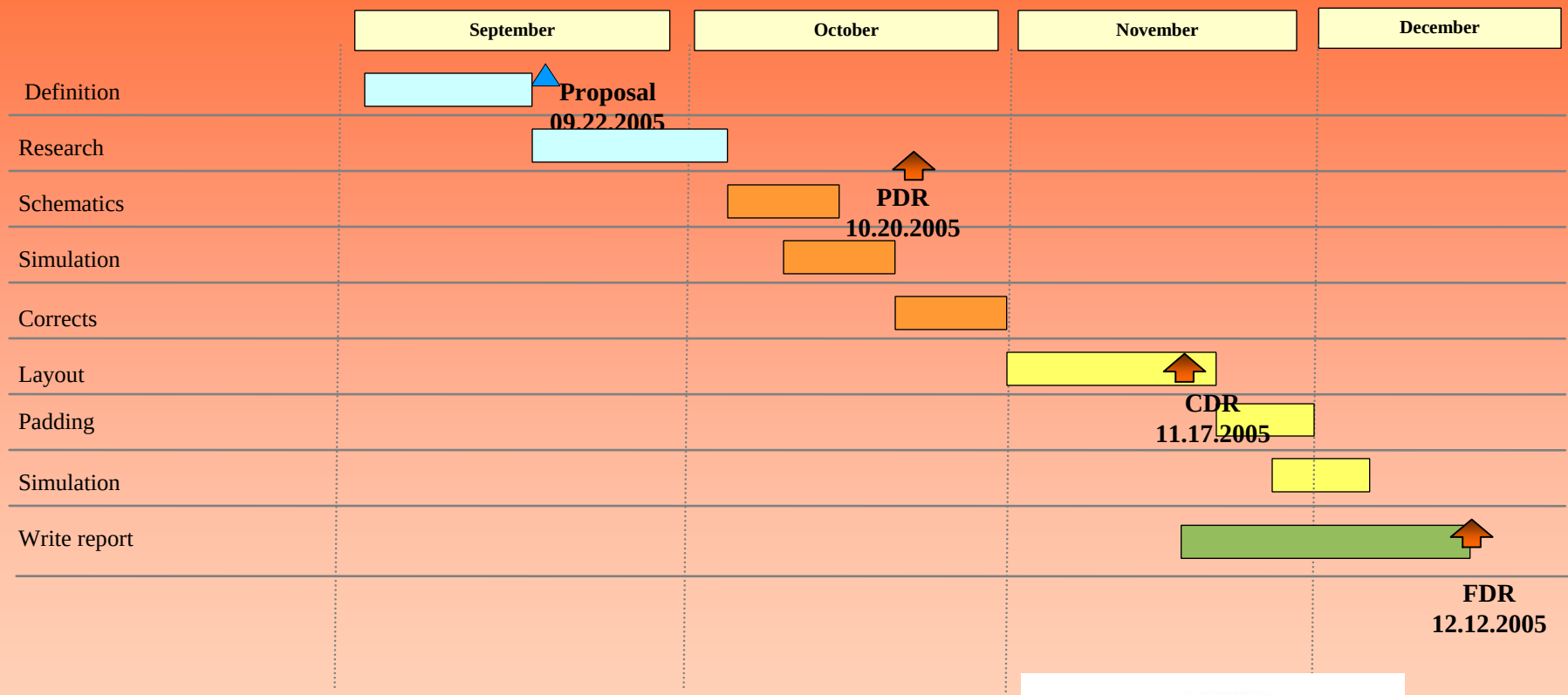
Layout

- 4 Point FFT





Project plan



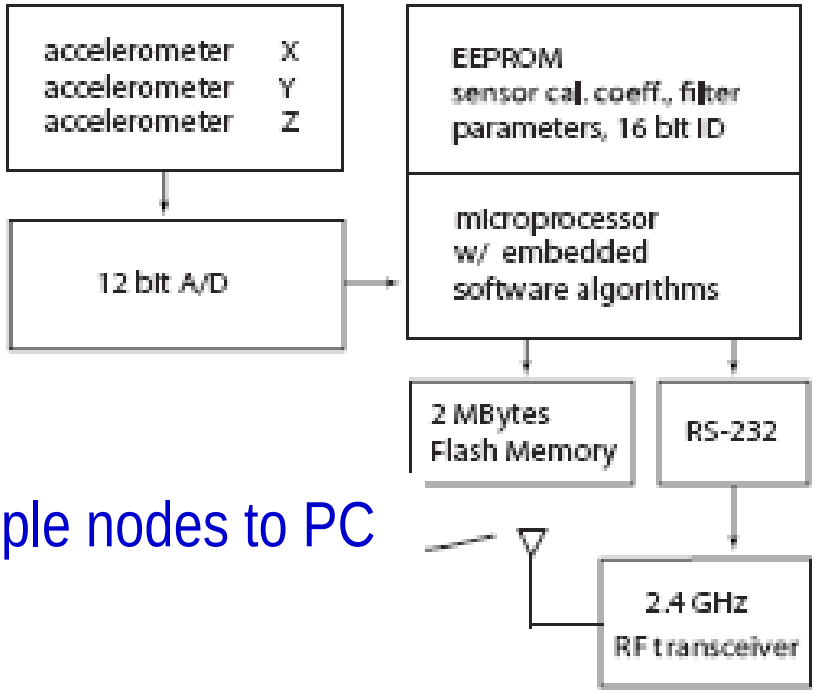
*Agenda

- project preparation
- project schematics + simulation
- layout, padding +simulations
- report

The Goal of the 2006 Project

- Relates to the work of the Rucinski Group and the Critical Infrastructure Dependability Laboratory
- Can be completed within the resource constraints {time primarily} of the course
- Can be extended into the Programmable System on a Chip Sensor Network Project in ECE-994

Microstrain G-Link



- Supports simultaneous streaming from multiple nodes to PC
- Available with 2g or 10g range
- Datalogging rates up to 2048 Hz
- Real-time streaming rates up to 736 Hz
- On-board memory stores up to 1,000,000 measurements
- Communication range up to 70m line-of-sight
- Low power consumption for extended use

MicroStrain®

Homeland SECURITY

2006 Project: Johnny SensorSeed

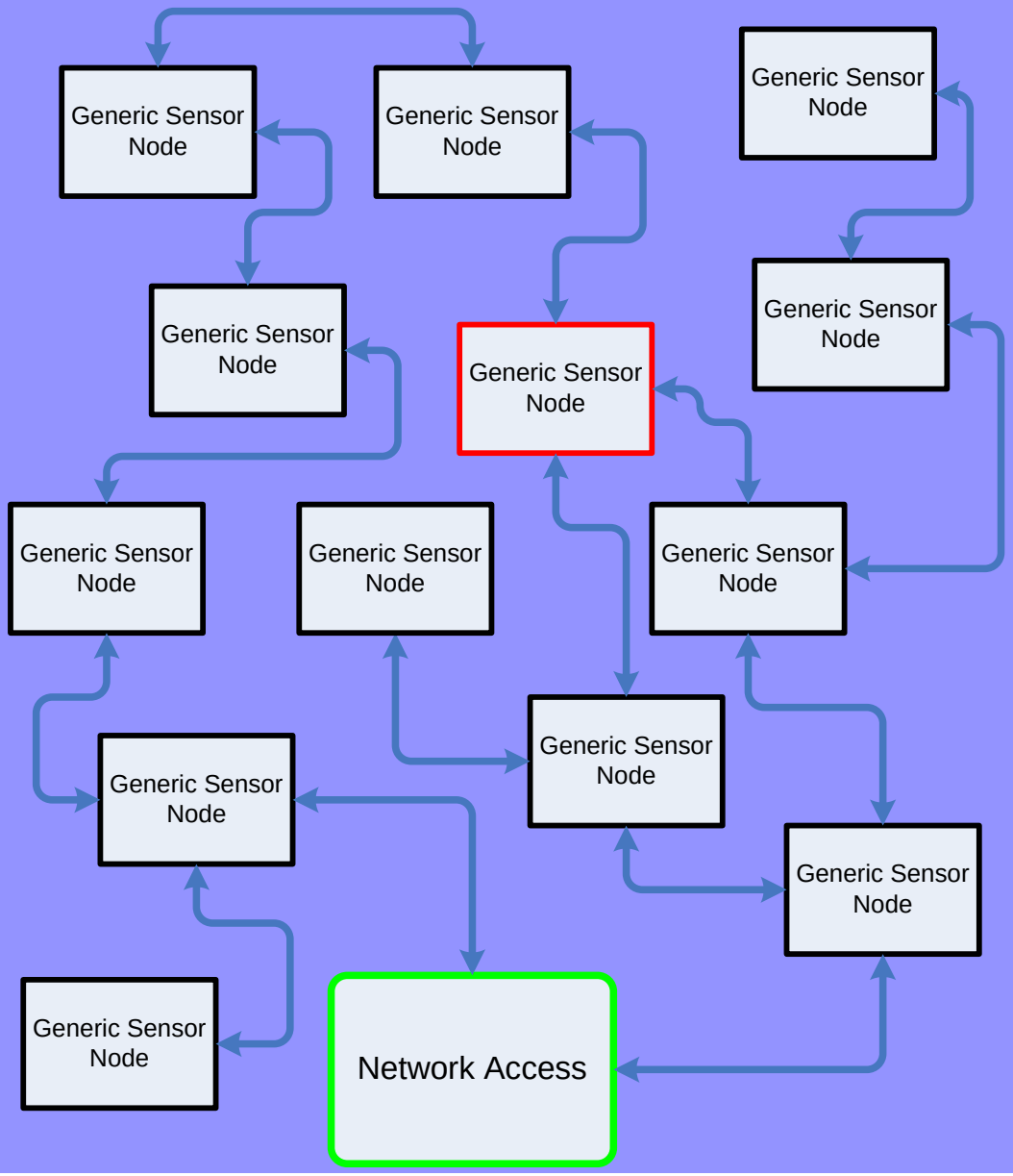
- Networkable Sensor Element
  - Low cost
  - Compact
  - Easily deployable
- Put the core of a MicroStrain Glink on a Chip
  - Or at least design the digital components that can be in principle integrated on a CMOS VLSI chip
  - that can be fabbed by MOSIS

2006 ECE-715 Project
Design a Generic Sensor Signal Preprocessor

- Part of a Node {Networkable Sensor Element} in a Sensor Network that includes a number of microaccelerometers
- The preprocessor provides:
  - The interface between the FPGA-based node processor and the
  - Parallel digital output of an A/D connected to the micoaccelerometer
  - Scaling and other signal functions
  - Control and Timing to the A/D
  - Status reports to the FPGA

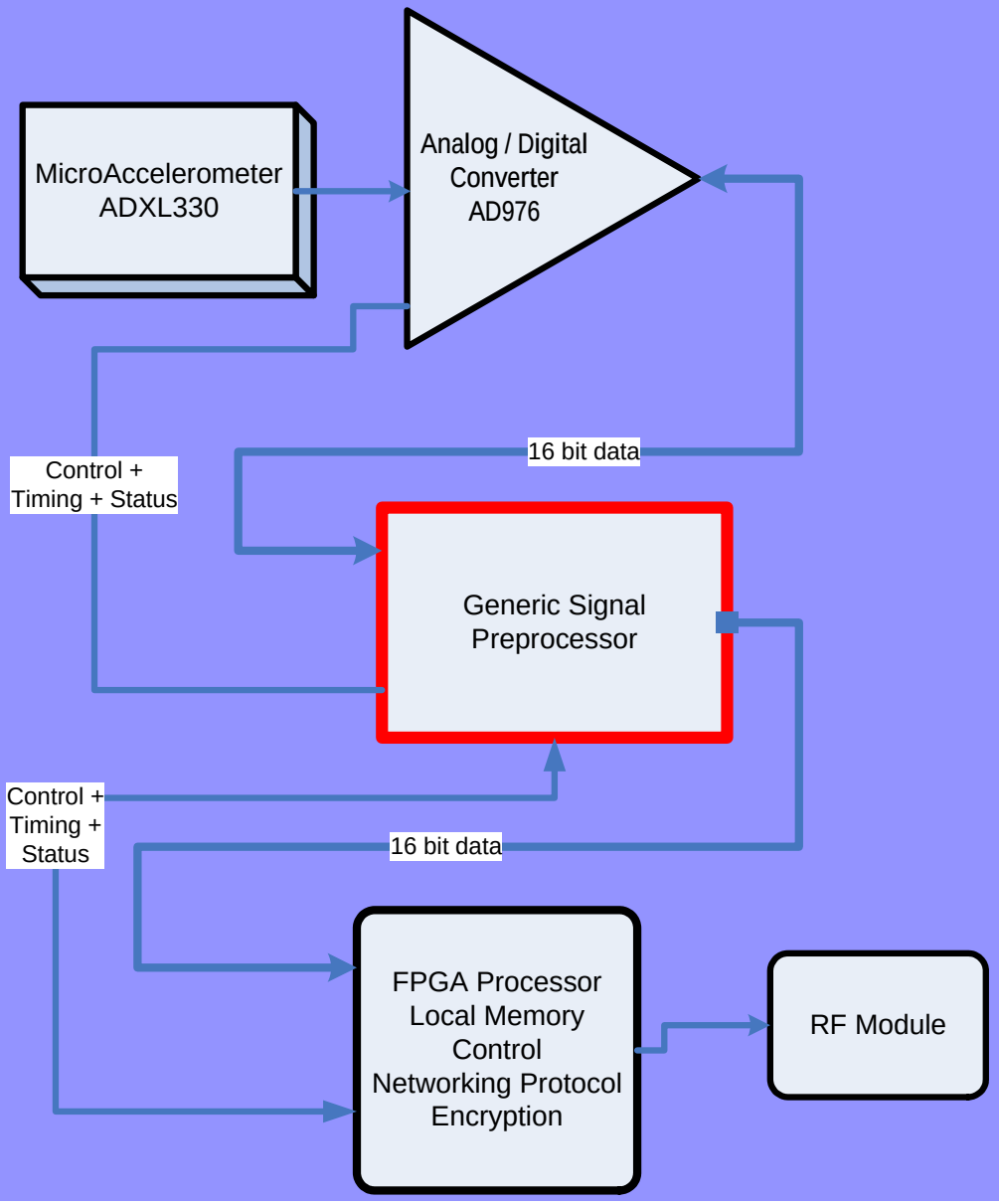
Overall Generic Sensor Network

Sensor Network Top-level Diagram



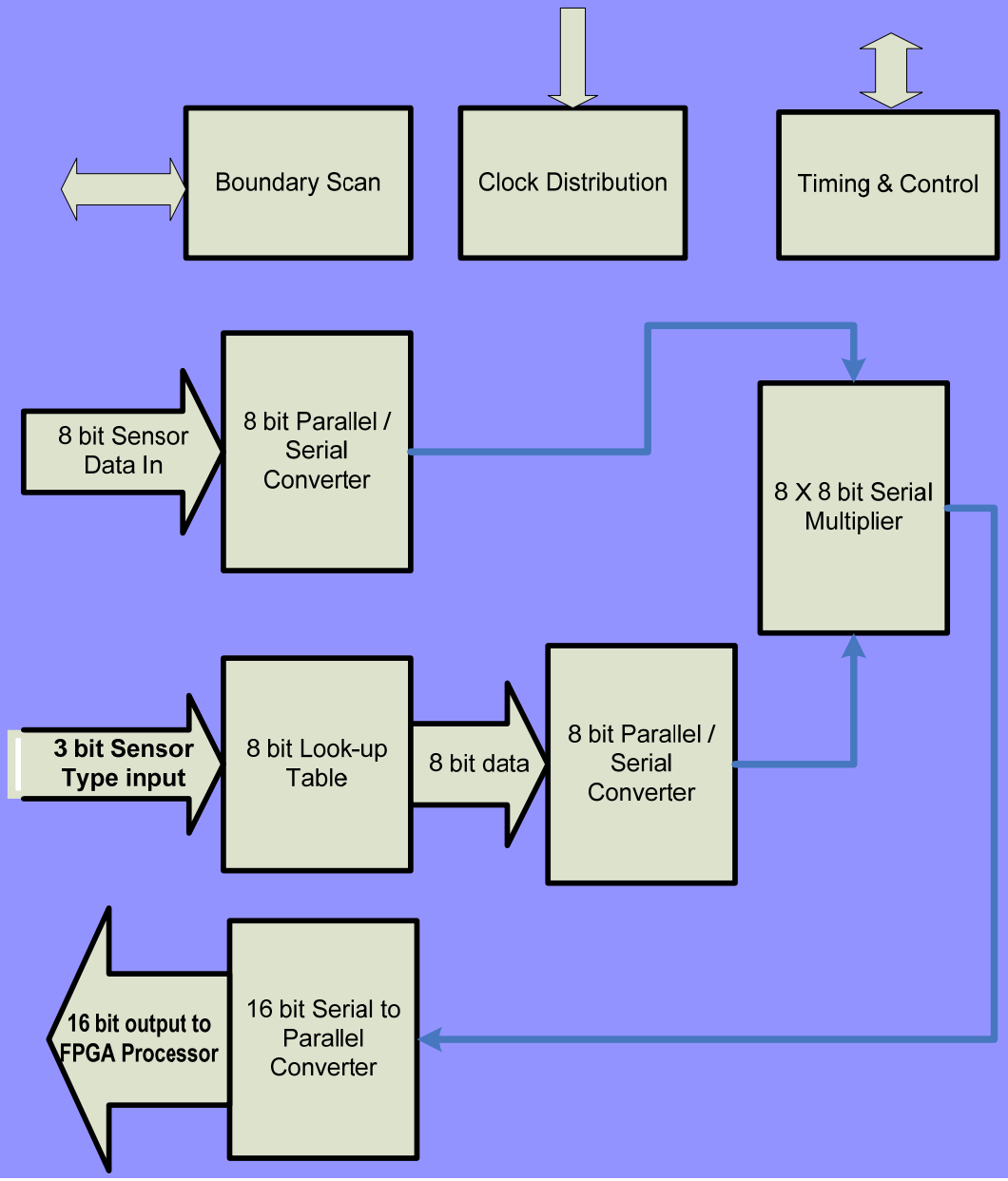
Node Top-Level Diagram

Sensor Network Generic Node



Generic Preprocessor Top-level Diagram

Sensor Generic Signal Preprocessor



2006-2007 SEMESTER II

- Monday, Jan. 15: Martin Luther King Day, University holiday
- Tuesday, Jan. 16: Classes begin
- Friday, March 9: Mid-semester
- Mon-Fri, March 12-16: Spring recess
- Tuesday, April 3: Passover*
- Friday, April 6: Good Friday*/Orthodox Good Friday*
- Monday, May 7: Last day of classes
- Tues-Wed, May 8-9 Reading Days
- Thursday, May 10 -- Thursday, May 17: Final exams
- Friday, May 18: Senior Day
- Saturday, May 19: Commencement

Result of Fab run

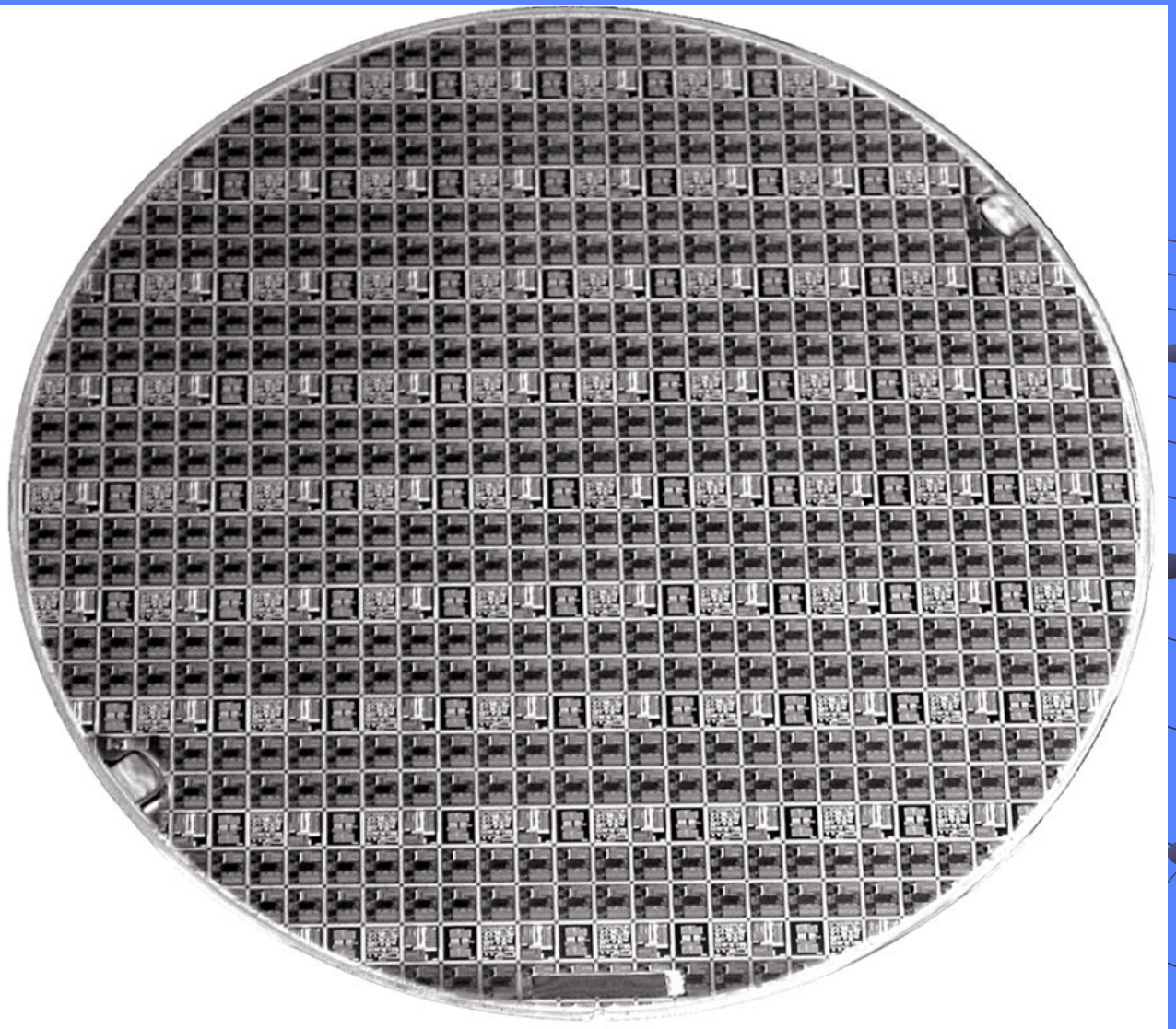


FIG 1.70 Processed 8-inch wafer

Final Product of Class:

a working CMOS VLSI Chip in 40 pin DIP

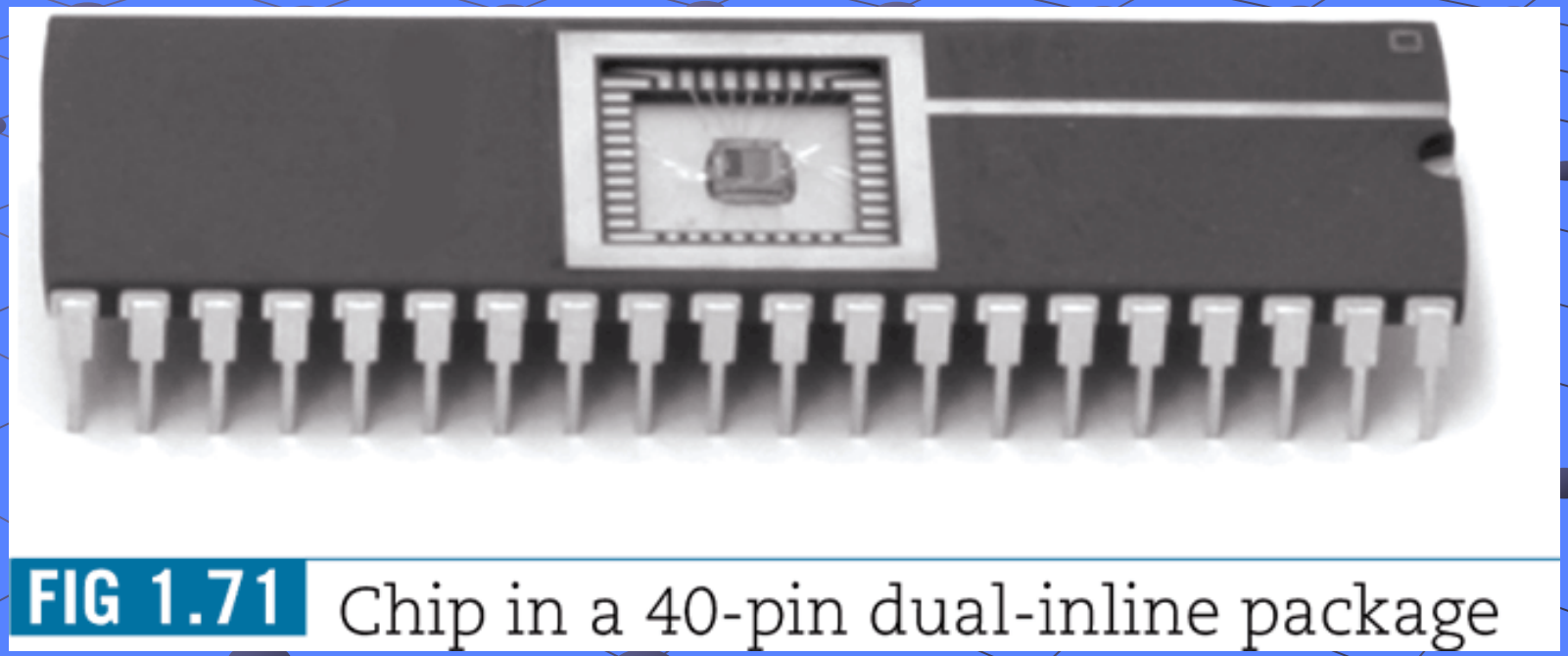


FIG 1.71 Chip in a 40-pin dual-inline package

VIII. Conclude

CONTACT INFO

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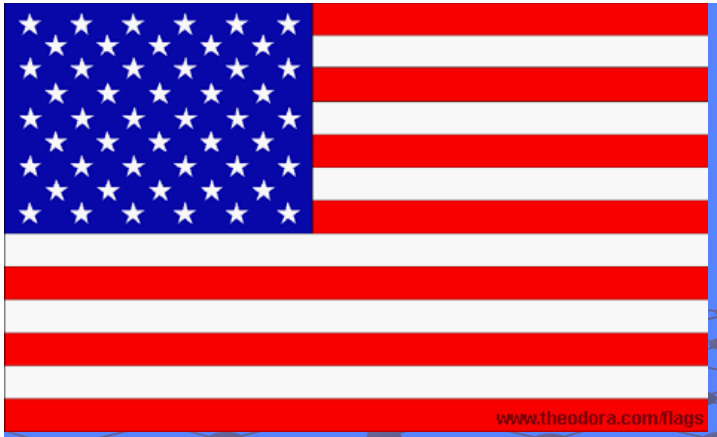

Thank You

Muchas Gracias

Dziękuję za uwagę

END Presentation

Following slides for backup only

DO NOT PRINT