ties of Edinburgh [5] and Zurich [6], and at the Supercomputer Research Center in Maryland [7].

The ENABLE machine is a system, built from FPGAs and SRAM, specifically constructed at the university of Mannheim [8] for solving the TRT problem of section 3.2. A second-generation board called ENABLE++ is already being built [25]. Many similar application-specific reconfigurable machines have been built in the recent years: the reconfigurable nature is only exploited while developping and debugging the application. Once done, final configuration is done, once and for all—until the next "hardware release".

Commercial products already exist: QuickTurn [9] and Meta-Systems[4] sell large configurable systems, dedicated to hardware emulation. Compugen [10] sells a modular PAM-like hardware, together with several configurations focusing on genetic matching algorithms. More systems exist than just the ones mentioned here.

A thorough presentation of the issues involved in PAM design, with alternative implementation choices, is given by Bertin [11].

2.1. The DECPeRLe-1 board

The overall structure of DECPeRLe-1 is shown in figure 4. Each of the 23 squares denotes one Xilinx XC3090 FPGA [12]. Each of the 4 rectangles represents 1 MB of static RAM (letter R). Each line represents 32 wires, physically laid out on the printed circuit board (PCB) of DECPeRLe-1. A photo of the system is shown in figure 4.

Depending upon the application, individual units are implemented within one to many FPGAs; they may also be implemented as *look-up tables* (LUT) through the local RAM; some slow processes are implemented by software running on the host. Connections between processing units are mapped, as part of the design configuration, either on PCB wires or on internal FPGA wires.

2.2. FPGA matrix

The computational core of DECPeRLe-1 is a 4×4 matrix of XC3090—letter M in figure 4. Each FPGA has 16 *direct connections* to each of its four Manhattan neighbors. The four FPGAs in each row and each column share two common 16-bit buses. There are thus four 64-bit buses traversing the array, one per geographical direction N, S, E, W.

The purpose of this organization is to best extrapolate, at the PCB level, the internal structure of the FPGA. What we have is close to a large FPGA with 64×80 Programmable Active Bits—except for a connection bottleneck every quarter of the array, as there are fewer wires on the PCB than inside the FPGA. By Noyce's thesis, DECPeRLe-1 implements, with 1992 technology,

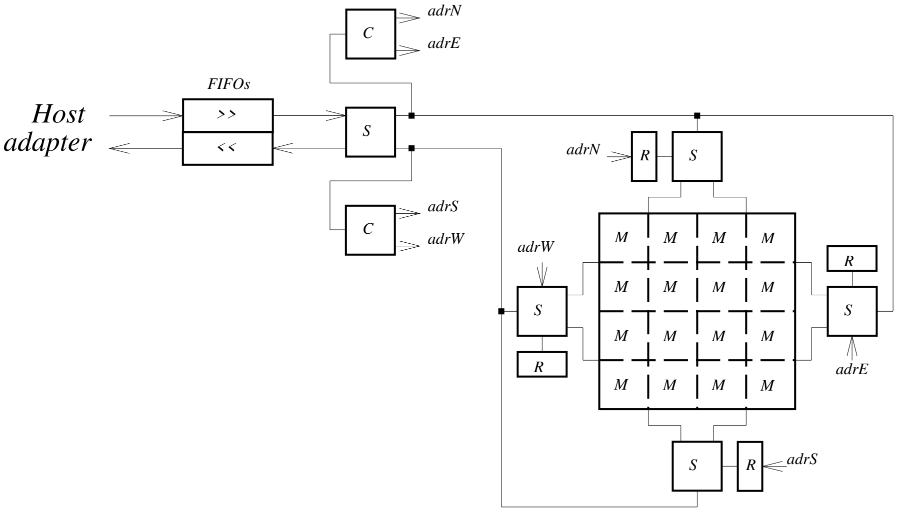

Fig. 4. DECPeRLe-1 architecture