Highly Linear VHF Current-Mode Miller Integrator with 90 dB DC Gain[1]

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Abstract

This paper presents a concept and an implementation of a current-mode integrator based on the Miller effect. The circuit has a highly linear, no feedback, current path, implemented using a Gilbert amplifier cell, and a voltage feedback path with capacitors, realizing integration. A bipolar transistor array process with devices with an f_T of 8 GHz *has been used for the circuit simulation. Phase response of* –90±0.5° *has been obtained in the frequency range* of 1 MHz *to* 670 MHz *(the low-frequency pole can be tuned electronically down to about* 3 Hz*). Excess phase can be compensated electronically to obtain exactly* –90° *for any frequency in the entire useful range. The gain of the circuit can be tuned electronically over at least* 40 dB. *THD for* 1 MHz *is better than 0.052% for an output current of* 2.8 mA_{pp}*, which represents 93% of the output tail current. DC gain of the circuit can be turned up to over* 90 dB.

1. Introduction

The integrator is a basic building block for many analog signal processing systems, *e.g.* filters [6, 10, 11]. The main requirements in integrator design are: low excess phase, high linearity, high speed (frequency range and slew rate), high DC gain, and availability of electronic tuning. In a popular OTA-C (operational transconductance amplifier and capacitor) technique of filter implementation, integrators are realized by loading a transconductor (OTA) with a capacitor [10]. The output signal is usually taken directly from the capacitor, and the circuit has high output impedance, inherited from the OTA. This high impedance, somewhat unusual in a voltage-mode output, is of course vital for the proper operation of the integrator. Due to the loading effect of the inputs of other OTAs typically connected to this high-impedance output, the integrator performance depends on a particular circuit configuration in which it is used. Various methods of accounting for this loading effect, such as parasitic absorption [10, 12], and the use of negative impedance [11], have been developed. Also, designs based on transimpedance opamps and current feedback [1] overcome these problems.

Another solution is a voltage-to-voltage, or current-to-voltage integrator based on the Miller effect. To realize a current-to-current integrator, a voltage-output Miller integrator is followed by an OTA [5]. In this arrangement, the linearity of the integrator depends on the linearity of the OTA, which in large-signal operation must convert the full swing of the voltage which builds up on the capacitor.

2. The concept

This paper presents a variation of the Miller integrator, general concept of which was presented for the first time in [8]. Instead of converting the output voltage into current, an internal current proportional to the output voltage is tapped to the output. This idea can be implemented in a variety of ways, one of which is shown in Figure 1. The core

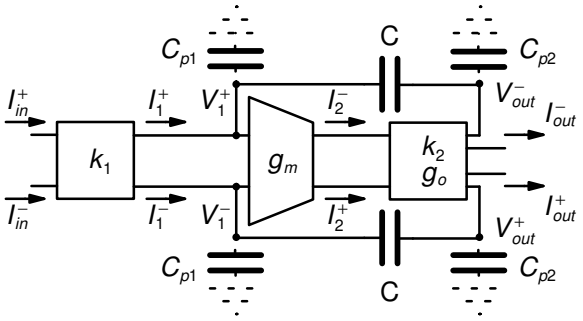

FIGURE 1. Current-mode integrator.

of this fully-differential circuit comprises an OTA input stage of transconductance $g_m = I_2/V_1$ and a current amplifier of gain $k_2 = I_{out}/I_2$, where $X_\alpha = X_\alpha^+ - X_\alpha^-$, $X \in \{V, I\}$, $\alpha \in \{in, 1, 2, out\}$. The current amplifier has an additional voltage-mode output with associated transresistance $1/g_o = V_o/I_2$. Capacitors C are connected to this output and to the input of the OTA, thus realizing a Miller integrator. A current buffer of gain $k_1 = I_1/I_{in}$ separates the high-impedance point at the input of the OTA from

1. Patent pending.

the signal source. Simplifying assumptions will be made in order to keep the analytical derivation of the integrator transfer function tractable. Thus, parasitic capacitances C_{p2} can be ignored, as they are connected to low impedance points and typically contribute a pole at over 10 GHz. The output impedances for the voltage and current outputs of the amplifier will be assumed to be equal to zero and infinity, respectively, and g_m, g_o, k_2 will be assumed to have neither zeros nor poles in or near the frequency range of interest. With these assumptions, the transfer function can be shown to equal

$$\frac{I_{out}}{I_{in}} = \frac{k_1\ k_2\ g_m}{s\left[\left(1 + \frac{g_m}{g_o}\right)C + C_{p1}\right] + \frac{1}{R_M}\left(1 + \frac{g_m}{g_o}\right)}, \quad (1)$$

where $g_m/g_o = V_{out}/V_1$ represents the low-frequency voltage gain in the loop, and

$$R_M = (g_o + g_m)R_{in}/g_o = R_{in}\left(1 + \frac{g_m}{g_o}\right) \quad (2)$$

represents resistance seen by the capacitors C, where R_{in} is the input resistance of the OTA input stage. Substituting (2) into (1) yields

$$\frac{I_{out}}{I_{in}} = \frac{k_1\ k_2\ g_m}{s\left[\left(1 + \frac{g_m}{g_o}\right)C + C_{p1}\right] + \frac{1}{R_{in}}}. \quad (3)$$

It follows that the DC gain of the integrator equals

$$A_{DC} = R_{in}\ k_1\ k_2\ g_m, \quad (4)$$

and the pole frequency is

$$f_p = \frac{1}{2\pi} \cdot \frac{1/R_{in}}{\left(1 + \frac{g_m}{g_o}\right)C + C_{p1}}. \quad (5)$$

To maximize A_{DC} and minimize f_p one should maximize R_{in}, k_2, and g_m, and minimize g_o, *i.e.* maximize both input resistance of the OTA and the voltage gain in the loop. High voltage gain in the loop additionally results in a low V_1 swing, relaxing the requirements on the OTA linearity.

Additionally

$$\frac{V_{out}}{I_o} = \frac{1}{k_2\ g_o}, \quad (6)$$

where

$$1/(k_2\ g_o) = R_E \quad (7)$$

is the emitter degeneration resistor in the particular circuit implementation presented further in this paper. Therefore k_2 should not be used for tuning of the integrator, as its changes result in changing g_o. The gain of the input current buffer, k_1, should be used instead. The buffer has low input impedance and it isolates the high-impedance input of the core circuit from the signal source, whose impedance thus is not critical for the circuit performance. Additionally, the buffer blocks the common-mode input signals. The current output of the integrator has high impedance and can be connected to the input of another integrator.

3. An implementation

A simplified schematic of a particular implementation is shown in Fig. 2A. Transistors $Q_1 \div Q_4$ form a Gilbert "type A cell" [4], working as the input buffer, with current sources I_A biasing the input pair Q_1, Q_2. This circuit is characterized by excellent linearity and high bandwidth [2, 4] (simulated –3 dB frequency for unity gain is better than 6 GHz). The buffer blocks the common-mode input signals, and additionally provides tunability of k_1 at least in the range of –20 dB to 20 dB [4] (by means of changing the ratio I_A/I_B). Current sources I_G are necessary to achieve high impedance at the OTA input and eliminate the common-mode component of the collector currents of Q_3 and Q_4. Transistors $Q_5 \div Q_8$ realize the OTA input stage. Changing I_C and I_D allows tuning of g_m. The current-mode amplifier, again based on the Gilbert "type A cell" is realized by $Q_9 \div Q_{12}$. Changing I_D/I_F allows tuning of k_1, again over at least 40 dB. This arrangement is similar to the one presented in [13]. Active loads I_H provide required voltage gain in the feedback loop. The voltage signal is then connected to the emitter follower Q_{13}, Q_{14}, providing also the output current. Linearity of the emitter resistors R_E (Eq. 7) in the follower is critical to the linearity of the integrator.

For proper operation, the circuit contains two common-mode cancellation subcircuits, one of which is shown in Fig. 2B. Their function is to assure adequate DC voltages at the two pairs of high-impedance points in the integrator, *i.e.* at the collectors of Q_3, Q_4, and the collectors of Q_{11}, Q_{12}. The circuits sense voltages on the emitters of the respective current gain cells and compare them with constant voltages, V_{B1} and V_{B2}. Any mismatch of the collector currents at the high-impedance points is corrected by adjusting the base-emitter voltages of the respective current mirror transistors, by means of dumping additional current onto their emitter resistors (R_1 and R_2 in Fig. 2B). The gain of the common-mode cancellation circuits can be adjusted by changing the tail current I_{b1} and I_{b2}.

4. Simulation results

With C of 0.8 pF the circuit demonstrates simulated phase response of –90±0.5° in the range of 1 MHz to 670 MHz (Fig. 3). The gain can be adjusted by changing the tail current of the input buffer (Fig. 4), without affecting the phase response significantly. The low-frequency pole can be moved down to about 3 Hz by changing the operating conditions of the circuit. With sufficiently high gain in the feedback loop, the circuit has THD of less than 0.052% for the output signal current of over 2.8 $mA_{p\text{-}p}$ (Tab. 1).

Table 1

Frequency	I_{out}	$I_{out}/I_E \cdot 100\%$	THD
1 MHz	200 µA	6%	0.0486%
1 MHz	2.83 mA	93%	0.0514%

Emitter area mismatches in the current gain cells will lead to nonlinearities which can be eliminated by applying measures prescribed in [3]. Mismatches of the emitter resistors in the current sources can be eliminated by applying correcting currents, in a similar manner as in the common mode cancellation circuits. Proper values of the R_E resistors are critical for high-frequency operation of the circuit because of a parasitic pole-zero pair near 500 MHz, not predicted by the simplified analytical derivation presented in the paper. However, even considerable departures from the required values can be corrected by changing the current I_E. I_E can also be used to correct the excess phase.

5. Conclusions

A current-mode, Miller integrator concept and implementation has been presented. The circuit combines good properties of the voltage-output Miller integrator as it is known in the literature, with the excellent linearity and speed of the gain cell proposed by Gilbert [2, 4]. The design is a core of a programmable amplifier-integrator [9] for a field programmable analog array [7, 8], currently under development. Voltage output from the integrator is possible if desired.

Future work includes improvement of the critical parameters, alleviating of some of the secondary effects not discussed in the paper, and simplification of the circuit implementation.

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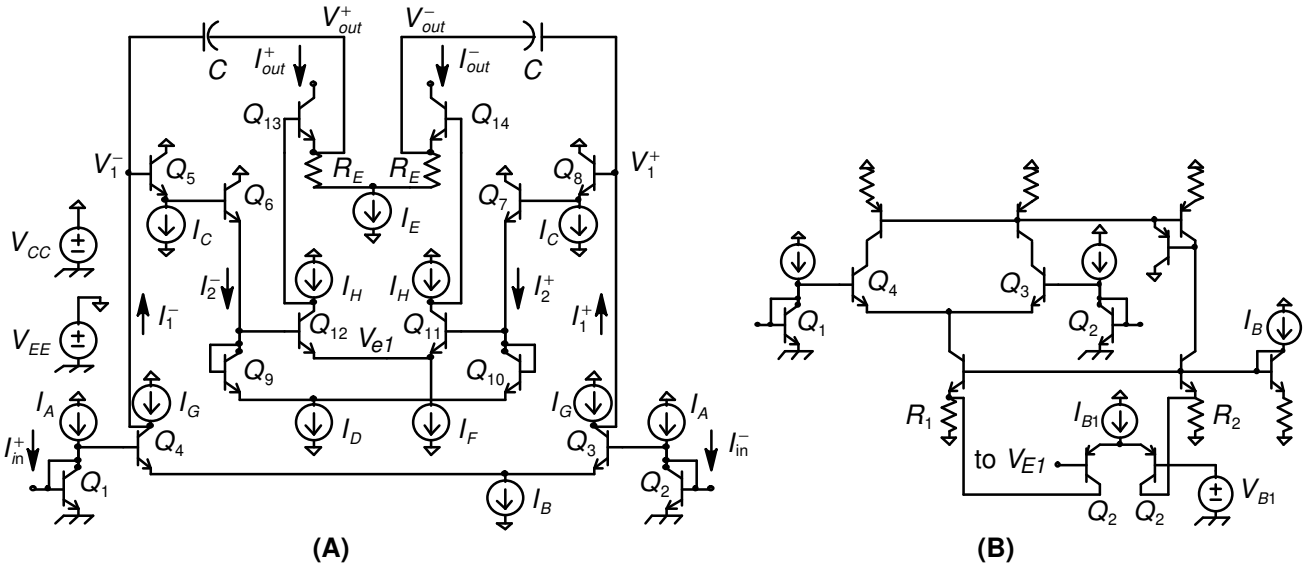

FIGURE 2. Electrical schematic of the integrator.

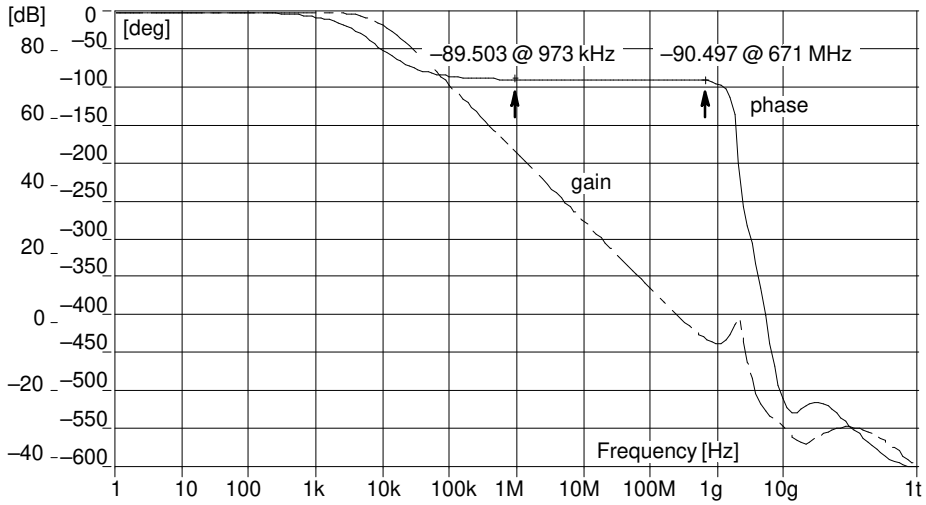

FIGURE 3. Frequency response of the integrator.

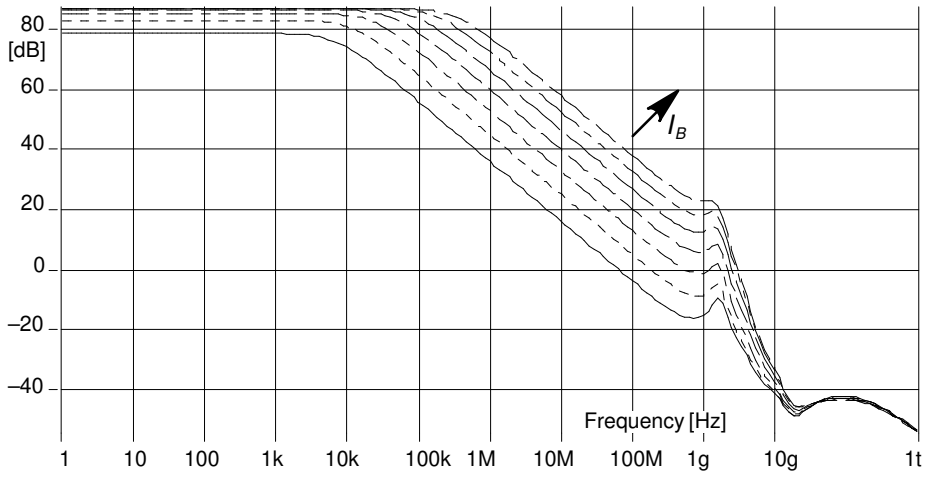

FIGURE 4. Tuning the gain of the integrator.