High-Frequency Field-Programmable Analog Arrays

a dissertation proposal

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Outline

1. Introduction
2. Proposed research
3. Preliminary research results
4. Conclusions

1. Introduction

1.1. Field-programmable devices

1.2. *Field-programmable analog arrays* (FPAAs)—state of the art; related work (ANNs, CNNs)

1.3. Wide-band FPAAs—the need and the challenges

Field-programmable devices

Field Programmable Gate Arrays (FPGAs) are revolutionizing digital circuits and systems design.

Why?

According to Sangiovanni-Vincentelli (UC Berkeley), **1992**:

- "[...] increasing pressure to bring to market new products and the more rapid obsolescence of existing products makes designing semi-custom circuits more and more problematic [...]"
- "The trend is clearly towards the more and more extensive use of programmable devices."

- “FPGAs are very appealing products: on one hand, they allow flexibility, fast time-to-market, customizability, just-in-time production, on the other they are ‘standard’ parts and can be manufactured in high volumes.”
- “The growth of the market in terms of dollars is staggering.”

Three main applications of FPGAs:

- **Rapid prototyping** and general purpose **hardware emulation**
- **System implementation**: “higher price/performance ratios for FPGAs versus semi-custom are compensated by time-to-market advantages.”
- **Dynamically reconfigurable subsystems**

Field-programmable analog arrays (FPAAs)—state of the art

FPGAs—in their current form—can handle **only digital applications**.

- The first commercial "analog" FPGA has become available: EPAC (Electrically Programmable Analog Circuit) from IMP, Inc., San Jose, Calif., based on switched capacitor (SC) technology, with bandwidth up to 120 kHz.
- There are no commercially available field programmable analog **continuous-time** devices.

Sivilotti, **1988** and Lee and Gulak, **1991–present**, demonstrated research results on continuous-time programmable analog devices.

- Emphasis on flexibility (full connectivity).
- Programming by means of switches (CMOS pass transistors).
- Bandwidth under 1 MHz.

Related work: analog circuits for *artificial neural networks* (ANNs) and *cellular neural networks* (CNNs):

- *High information throughput* due to *massively parallel processing*.
- Predominantly global signal connections in ANNs.
- Relatively low bandwidth (typically under 1 MHz).
- Hardware designed to implement specifically ANNs or CNNs—these are not general-purpose programmable analog circuits.

Wide-band FPAAs—the need

There is a need for wide-band field-programmable analog devices.

Example

- In a commercial application, three band-pass filters implemented in *surface acoustic wave* (SAW) technology are used to filter signals in one of three selected bands: VHF (138–174 MHz), UHF (403–470 MHz), and in the "900 MHz" band (806–941 MHz).

- The SAW filters are an obstacle to the full integration of the circuit, desired in order to decrease the cost. A HF field-programmable active filter might be a solution.
- In contrast, a high-throughput, low-frequency approach typical of analog ANN and CNN implementations cannot be used here because of the required bandwidth.
- The low-frequency FPAA circuits mentioned above also do not provide bandwidth nearly as high as is required.□

Example

- A computer disk drive custom IC contains two linear filters of drastically different characteristics. One is used in the servo control system for positioning disk heads, the other in the read channel.
- The two filters never work simultaneously, as either the disk heads are being moved to another track, or they have been moved and a read operation is being performed.

- A single filter of electronically tunable parameters (such as the cut-off frequency) cannot be used as the required characteristics for the two filters differ too much.
- A field-programmable approach would be an ideal solution, but the state-of-the-art field-programmable analog circuits have insufficient bandwidth.□

Wide-band FPAAs—the challenges

- To achieve *full programmability*, an analog circuit must support programming of:
  1. **parameters**,
  2. **structure** and **functions**.
- It must work in continuous time (c-t) mode to achieve maximum bandwidth.

Full programmability requires:

1. designing a **multi-function cell** (basic circuit block),
2. providing a **flexible architecture** (scheme of interconnections) between programmable cells.

The goal of the proposed research is to achieve it without compromising performance (bandwidth).

State-of-the-art c-t field-programmable analog circuits suffer bandwidth limitations:

- Emphasis on *full connectivity* leads to the use of *global signal interconnections*, which compromise HF performance.
- To program the structure and functions, switches are used in the signal path.
- Long signal interconnections and switches cause phase errors in transmitted signals, effectively limiting the bandwidth of the programmable circuit.

2. Proposed research

2.1. General research objective

2.2. Research hypotheses

2.3. Research plan

2.4. Research results evaluation

2.5. Specific contribution of this research

General research objective

- The purpose of the proposed research is to examine the feasibility of HF, digitally field-programmable c-t analog circuits, *i.e.* high-speed FPAAs.
- It is of utmost importance to examine the sources of bandwidth limitation in field-programmable c-t circuits, and to find methods of overcoming those limitations.

Research hypotheses

Hypothesis 1.

The most serious limitation of the bandwidth of field-programmable analog circuits comes from two sources:

1.1. the signal interconnection scheme (architecture): current field-programmable c-t circuits use interconnection schemes emphasizing full connectivity (flexibility), and

1.2. non-ideal behavior of switches placed in the signal path in order to program the circuit.

Hypothesis 2.

There exists a methodology of limiting (constraining) the architecture, which yields performance benefits that exceed loss in flexibility. Moreover, performance measures of resulting field-programmable c-t circuits are comparable to the same performance measures of custom (non-programmable) circuits, manufactured for the same task, in the same (or similar) technology. Common performance measures, such as *bandwidth*, *S/N ratio*, *dynamic range*, will be used.

Hypothesis 3.

There exists a method of radically reducing adverse effects on the field-programmable c-t circuits' performance caused by switches in the signal path.

Research plan

1. Literature supporting hypothesis 1. will be cited. Additionally, computer simulations will be used to demonstrate problems caused by long signal interconnections and switches. These problems include *crosstalk*, *RC time-constant delays* and *phase errors*.

2. A family of FPAA architectures designed to alleviate the problems listed in 1. will be proposed. The flexibility of the architectures will be demonstrated in the following process:

- **2.1.** A basic architecture with local interconnections, supporting only linear filters, will be presented.
- **2.2.** Selected nonlinear circuits, such as rank and median filters, adaptive filters, PLLs, will be considered, and extensions required to support these circuits will be studied.
- **2.3.** Circuits requiring global connections will be taken into consideration. Required FPAA architecture modifications will be studied. Non-planar architectures will be studied as well.

3. Flexibility of the family of architectures developed in 2. will be studied as a function of the architecture complexity.

4. Circuits designed to alleviate the problems introduced by switches in the signal path will be presented.

5. Computer simulations of complete FPAAs of architectures developed in 2. and circuits developed in 4. will be used to demonstrate the performance of the proposed architectures and circuit solutions.

6. Silicon implementation of test circuits will be examined.

Research results evaluation

1. A benchmark of circuits representative of modern electronic designs will be created. Flexibility of example architectures will be evaluated by calculating the percentage of circuits from the benchmark which can be realized in a given architecture *vs.* their performance. Performance measures such as bandwidth and other common circuits' parameters will be used.

2. The performance will also be compared

- with the same or similar circuits implemented in other FPAAs, as reported in the literature, and
- with the same or similar circuits implemented directly (*i.e.* without the use of an FPAA).

Specific contribution of this research

- Addressing the performance issue of FPAAs in a systematic way for the first time.
- Proposing a methodology of creating a family of flexible architectures with restricted connections.
- Demonstration of family of FPAA architectures with predominantly local signal interconnections.
- Elimination of switches from the HF signal path of programmable circuits.

3. Preliminary research results

3.1. State-of-the-art FPAAs and their bandwidth limitations

3.2. Methodology for the creation of FPAA architectures—an outline

3.3. A specific FPAA architecture: an exemplification of the methodology

3.4. Programming of the cell function without switches in the HF signal path

3.5. Flexibility of the exemplary architecture—examples

State-of-the-art FPAAs and their bandwidth limitations

Long signal interconnections and **switches** in the signal path cause

- RC time-constant delays and phase errors:
  - ☞ transfer function distortion,
  - ☞ stability problems,
- undesired coupling and noise susceptibility:
  - ☞ performance degradation,
  - ☞ stability problems.

Methodology for the creation of FPAA architectures—an outline

No programmable devices are expected to target all possible applications. A specification of the target class of circuits is assumed as a prerequisite to the proposed methodology.

1. Select circuits representative of the target class (*e.g.* linear filters).
2. Identify basic signal-processing operations (*e.g.* gain, integration). This steps leads to the identification of the "atomic" processing units—cells.

3. Examine the topology of the target class (*e.g.* ladder).

4. Create an FPAA architecture as a generalization of this topology (topologies) (*e.g.* a planar, locally-connected square or hexagonal grid). This is an optimization step with the objective function being the total interconnection length.

5. Examine the performance of the circuits selected in 1., when mapped into the FPAA.

An exemplary FPAA architecture

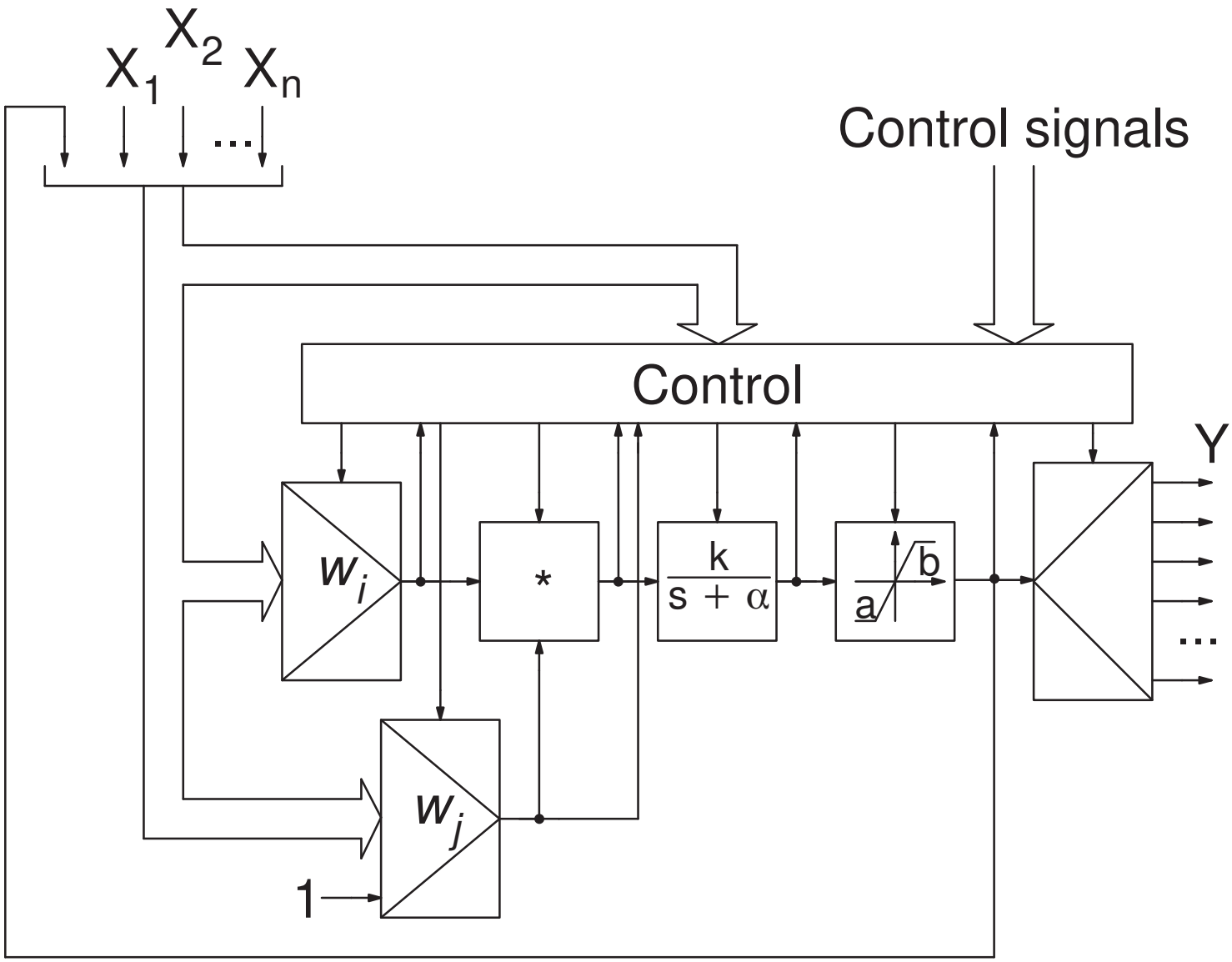
An *architecture* comprises:

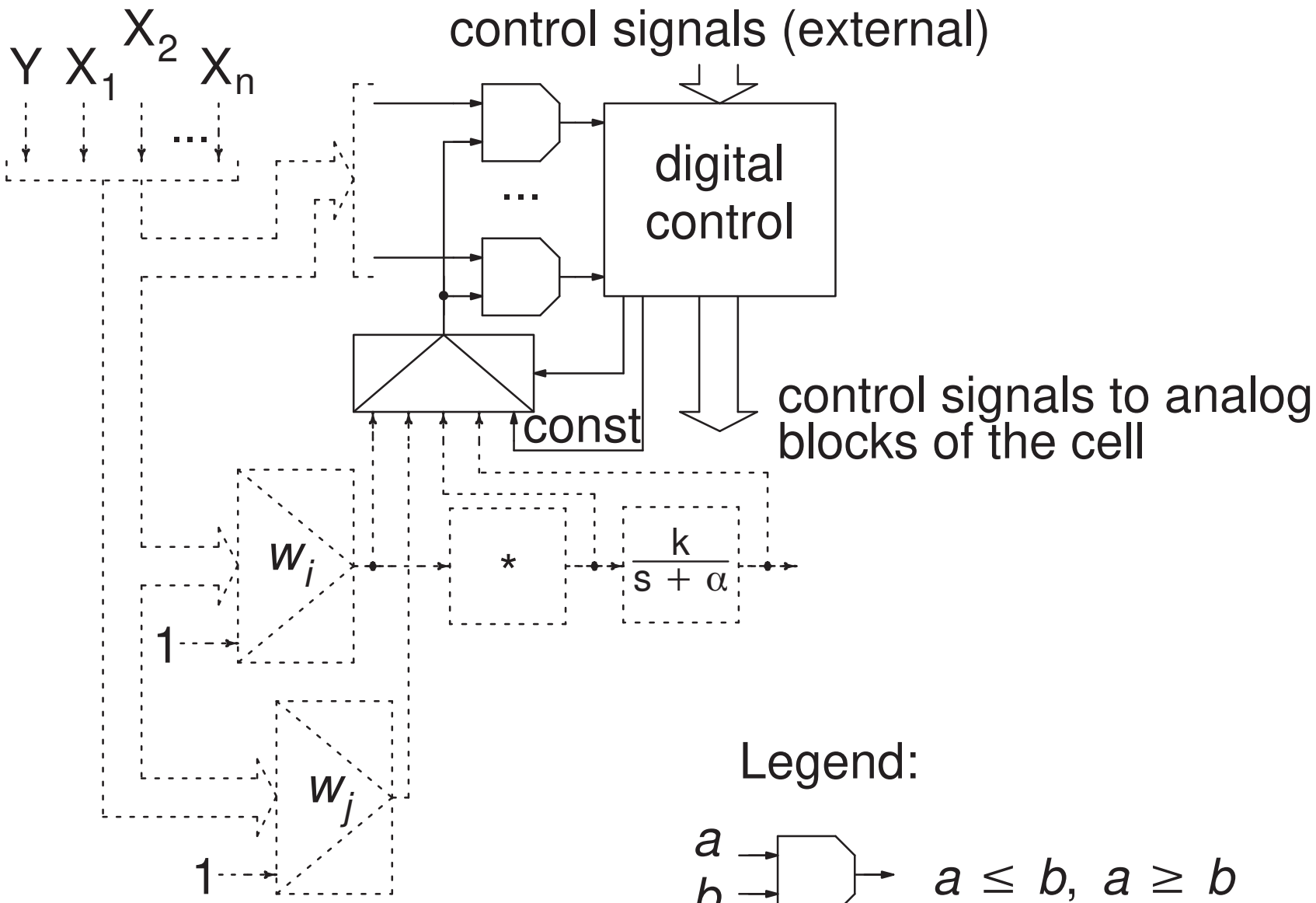
1. functionality of a single cell,
2. pattern of interconnections between the cells.

Basic cell functions

- Weighted addition/subtraction
- Multiplication/phase detection
- Integration over time
- Clipping (limiting) of the signal level

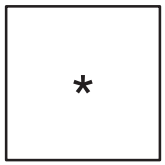
All operations can be **programmed**.


X1
X2
Xn
...
Control signals
Control
Y
wi
*
k
s + α
a
b
wj
1
...

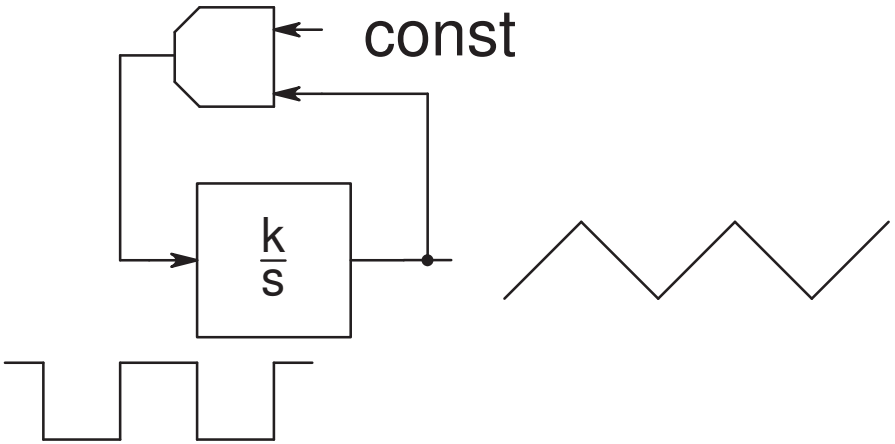

control signals (external)
Y
X1
X2
Xn
digital control
const
control signals to analog blocks of the cell
wi
1
wj
1
*
k
s + α
Legend:
a
b
a ≤ b, a ≥ b

The control block enhances functionality of the cell:

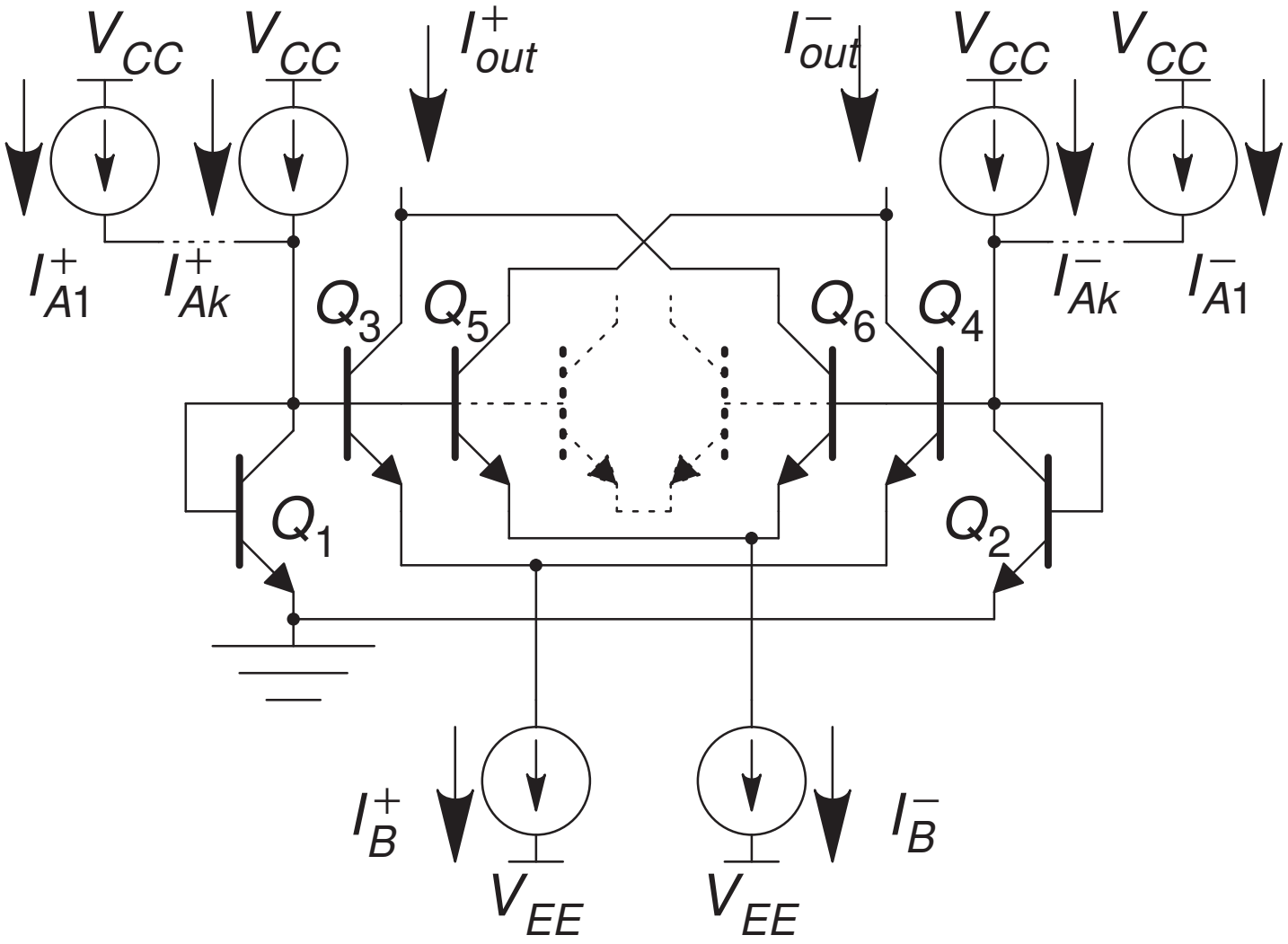
- Nonlinear operations such as min/max follower
- Signal-controlled generation of programmed waveforms
- Signal-to-frequency conversion (VCO)
- Phase-Locked Loops (PLLs)
- Multi-Valued Logic (MVL)
- Fuzzy logic

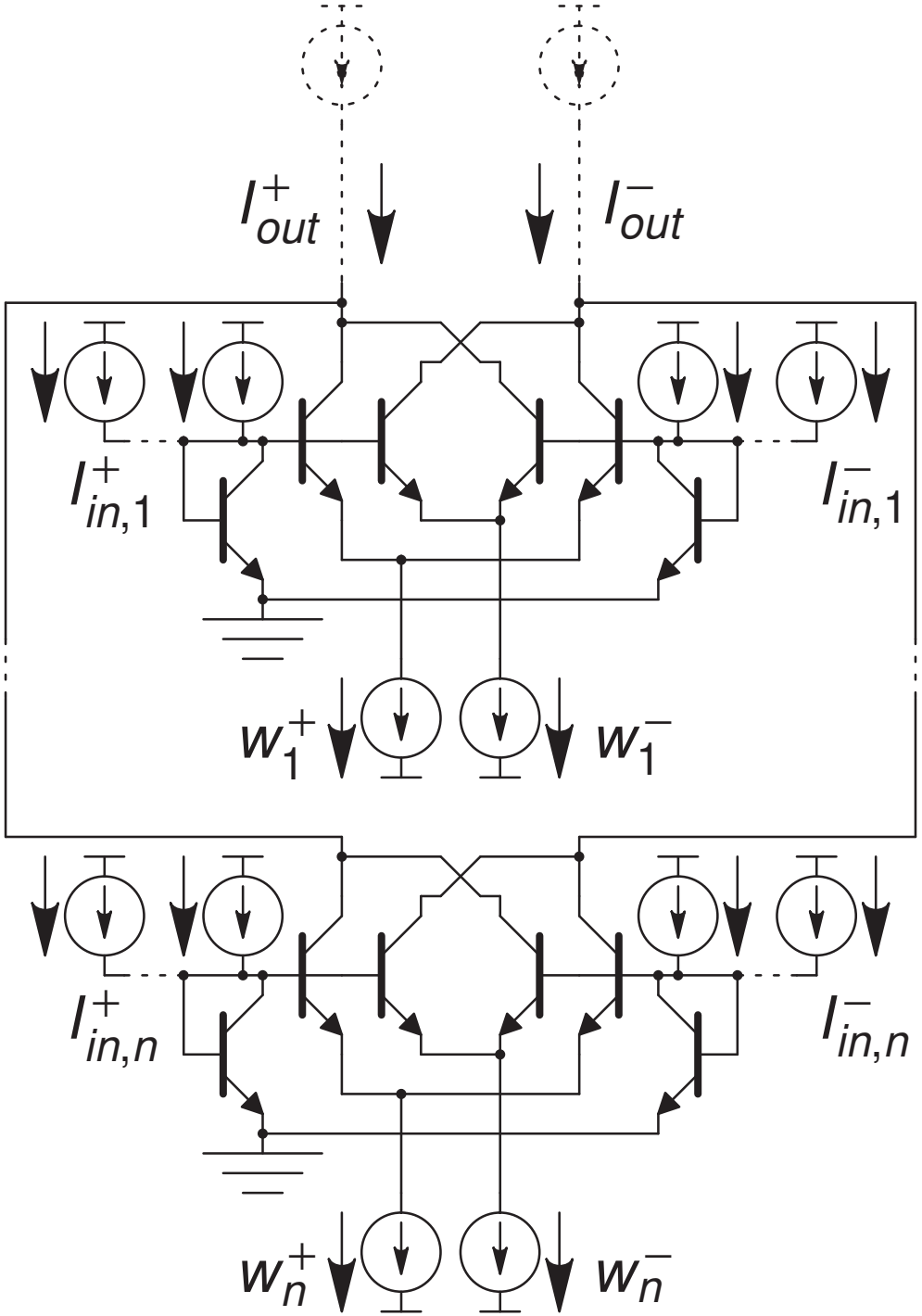


Gilbert multiplier—it can also be used as a balanced modulator and phase detector



- programmed sine waves can be generated by a linear circuit composed of several cells


V_{CC}
V_{CC}
I^{+}_{out}
I^{-}_{out}
V_{CC}
V_{CC}
I^{+}_{A1}
I^{+}_{Ak}
Q_3
Q_5
Q_6
Q_4
I^{-}_{Ak}
I^{-}_{A1}
Q_1
Q_2
I^{+}_{B}
I^{-}_{B}
V_{EE}
V_{EE}


I^+_{out}
I^-_{out}
$I^+_{in,1}$
$I^-_{in,1}$
w^+_1
w^-_1
$I^+_{in,n}$
$I^-_{in,n}$
w^+_n
w^-_n

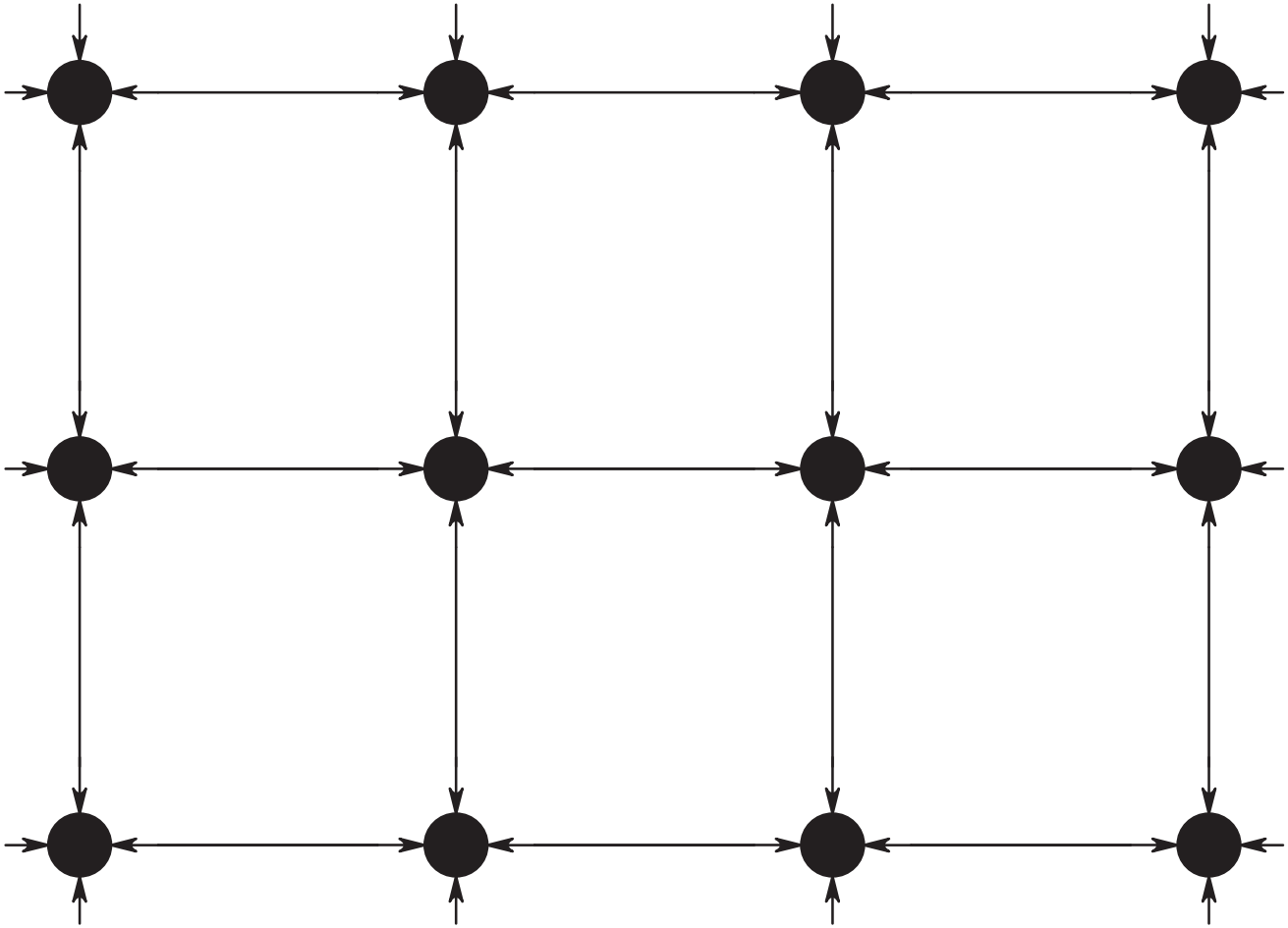
Pattern of interconnections between cells

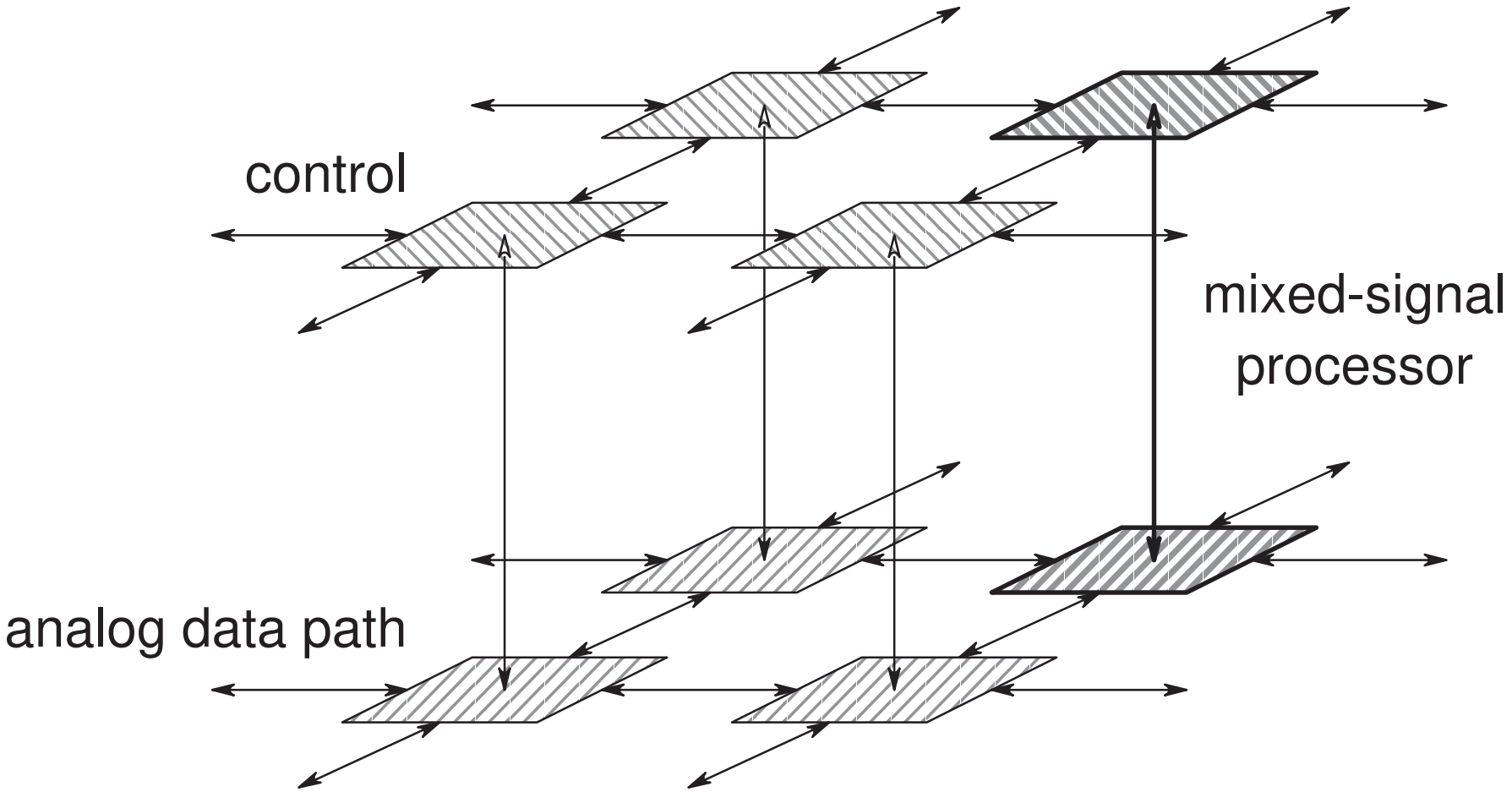
Full (almost full)

- flexibility

Restricted

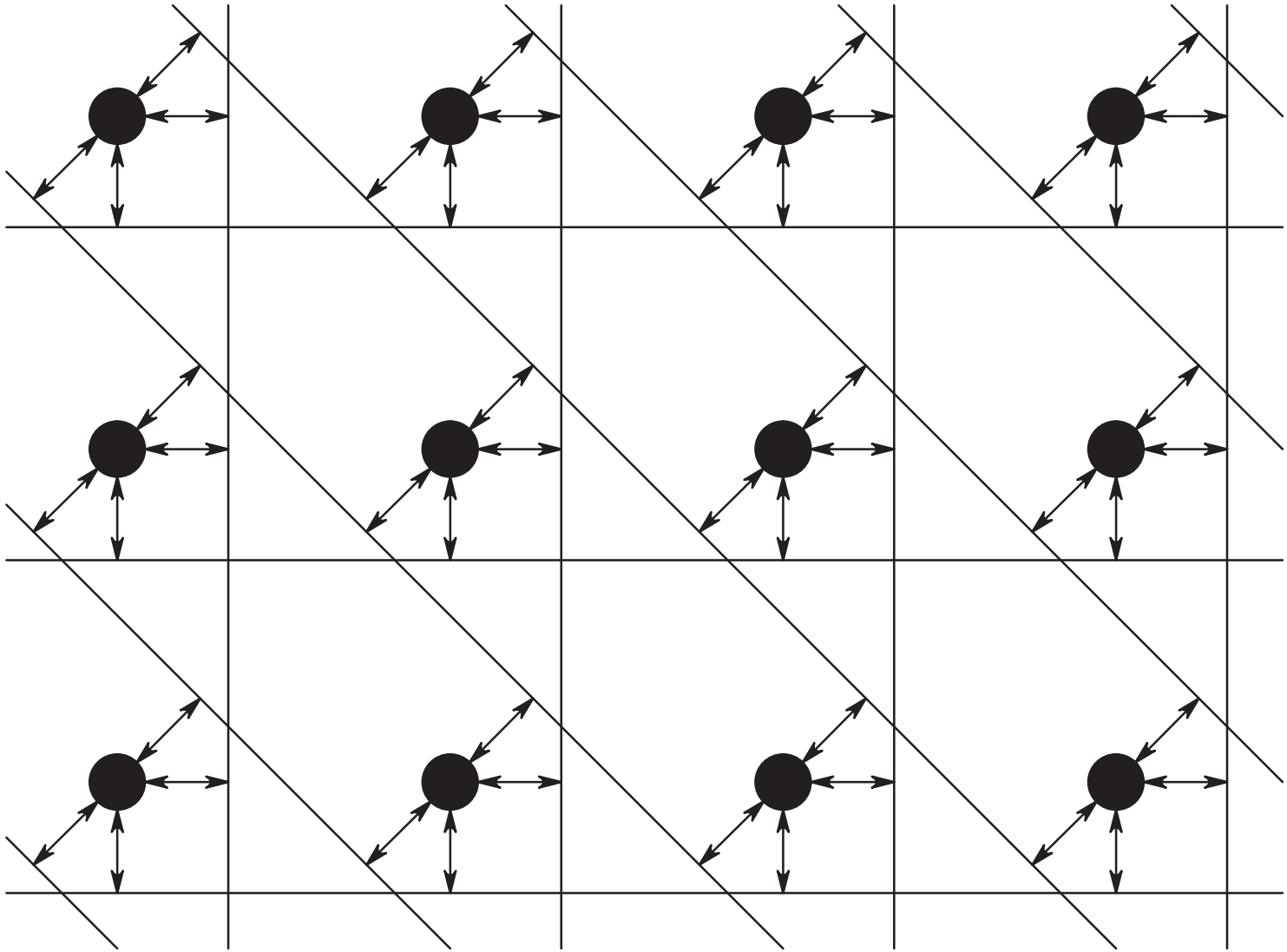
- performance





Dual cellular structure

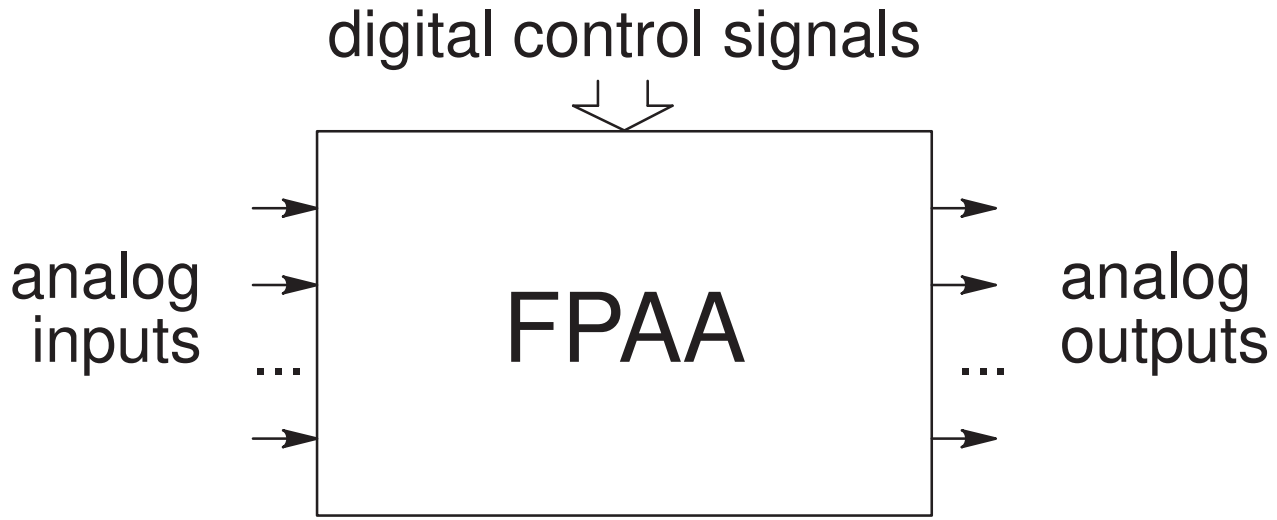
Global interconnections can be used, but only if necessary.



Signals between cells are exchanged in **current form**

- High speed
- Good noise immunity

The chip can be thought of as an **analog processor with digital control**:

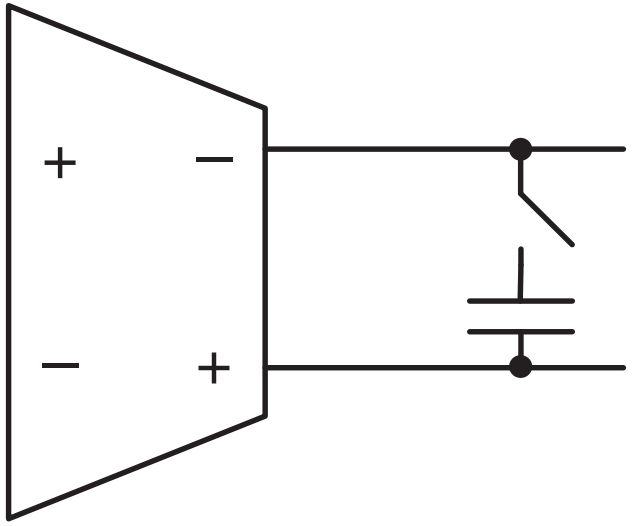


Proposed FPAA “philosophy”:

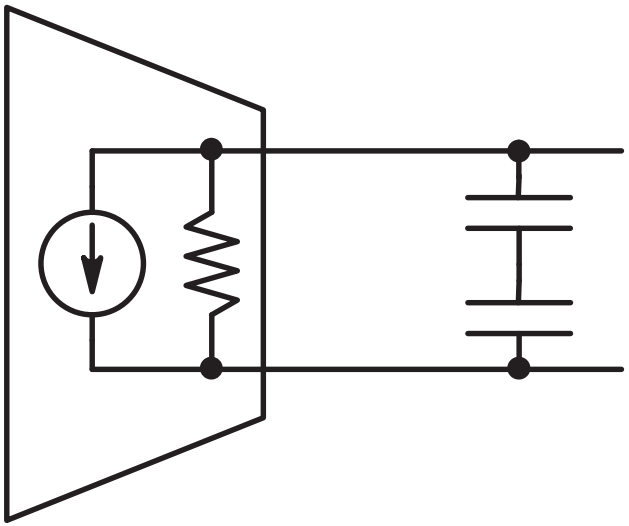
- **Functional analog cells** forming a “data path”
- **Flexible digital control** forming a control layer coupled with the analog “data path”
- **A regular array** of cells with primarily **local interconnections**
- **Digital control interface** between the chip and the outside world

Programming of the cell function without switches in the HF signal path

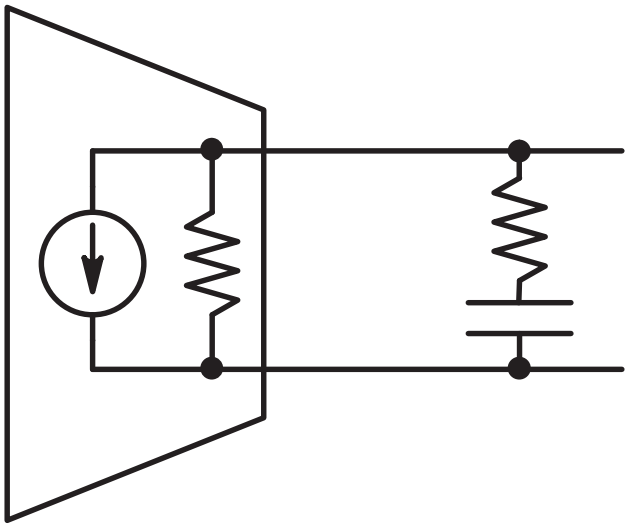
A straightforward implementation of a **programmable amplifier-integrator** in OTA-C technique would lead to a switch in the signal path:



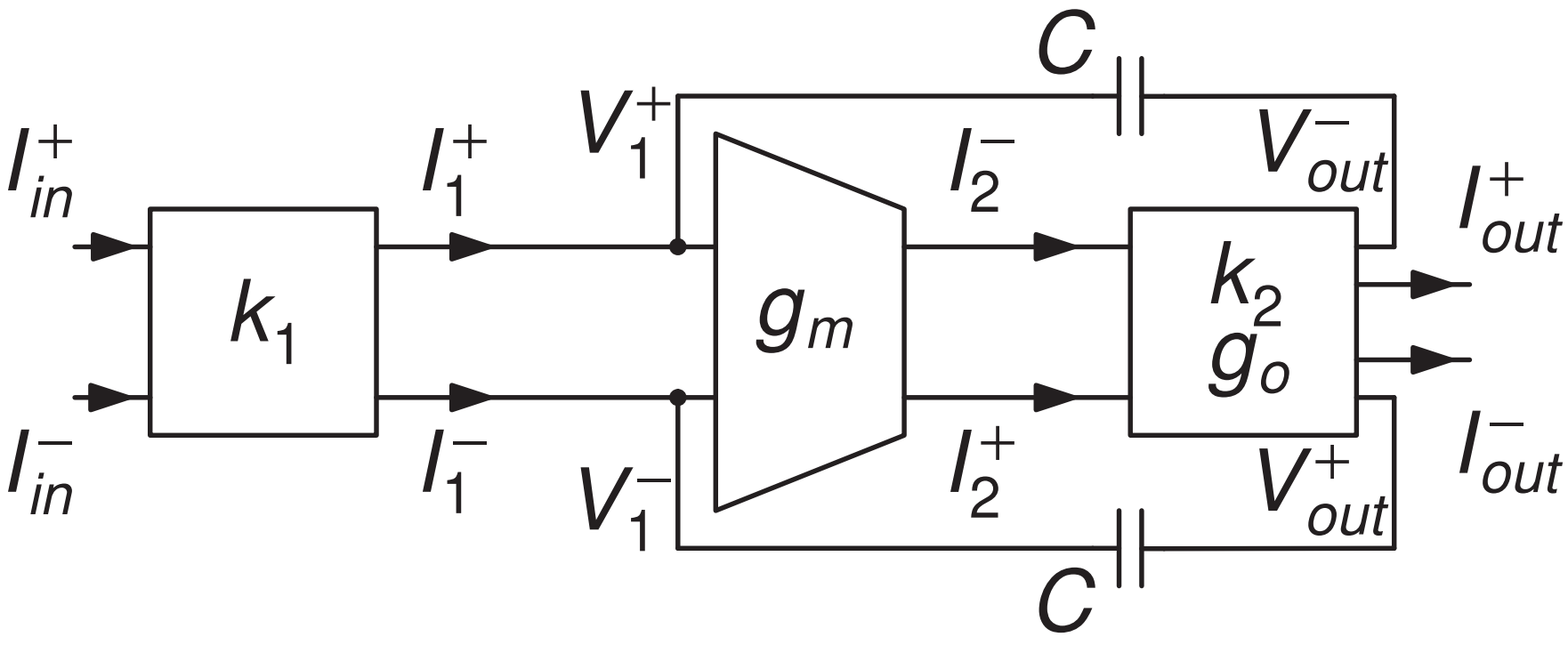
Which would lead to ...

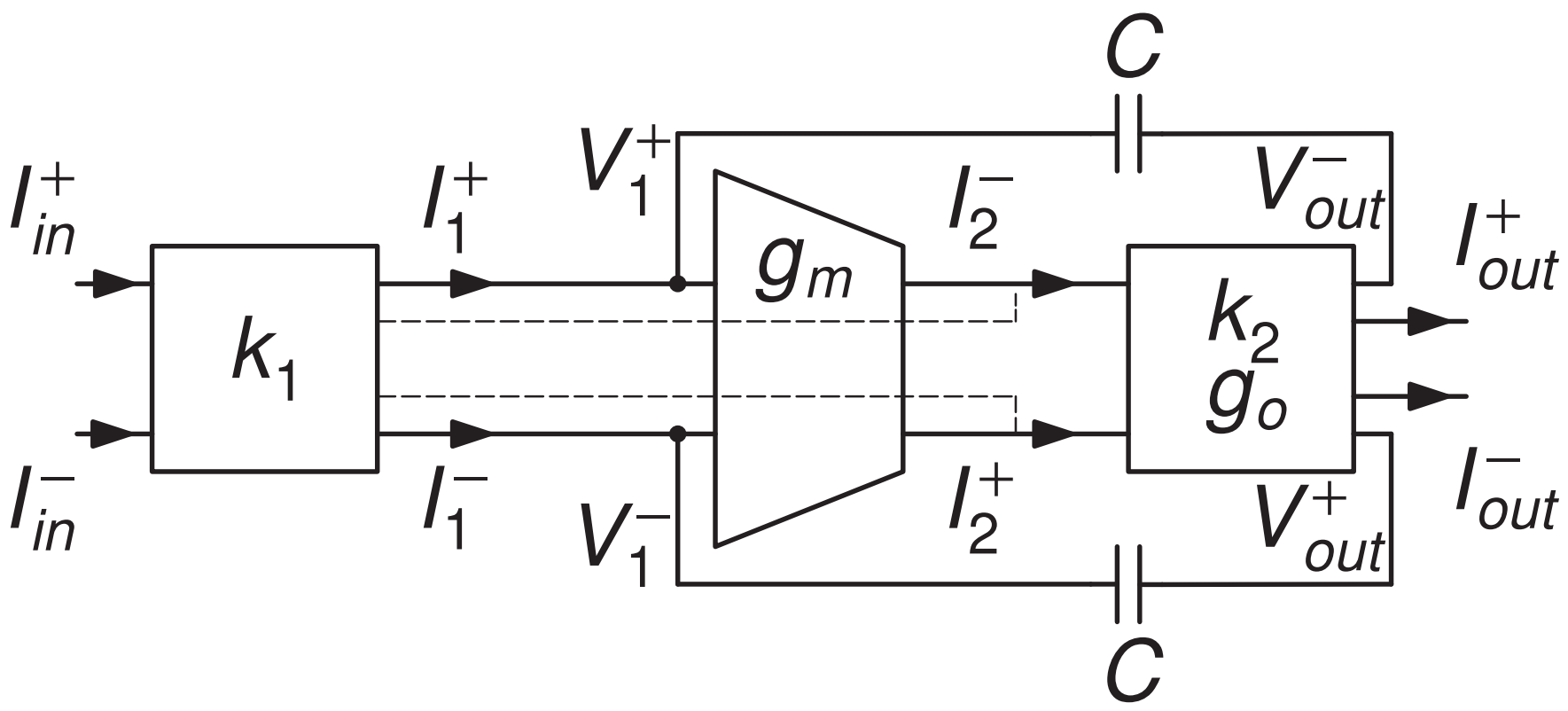


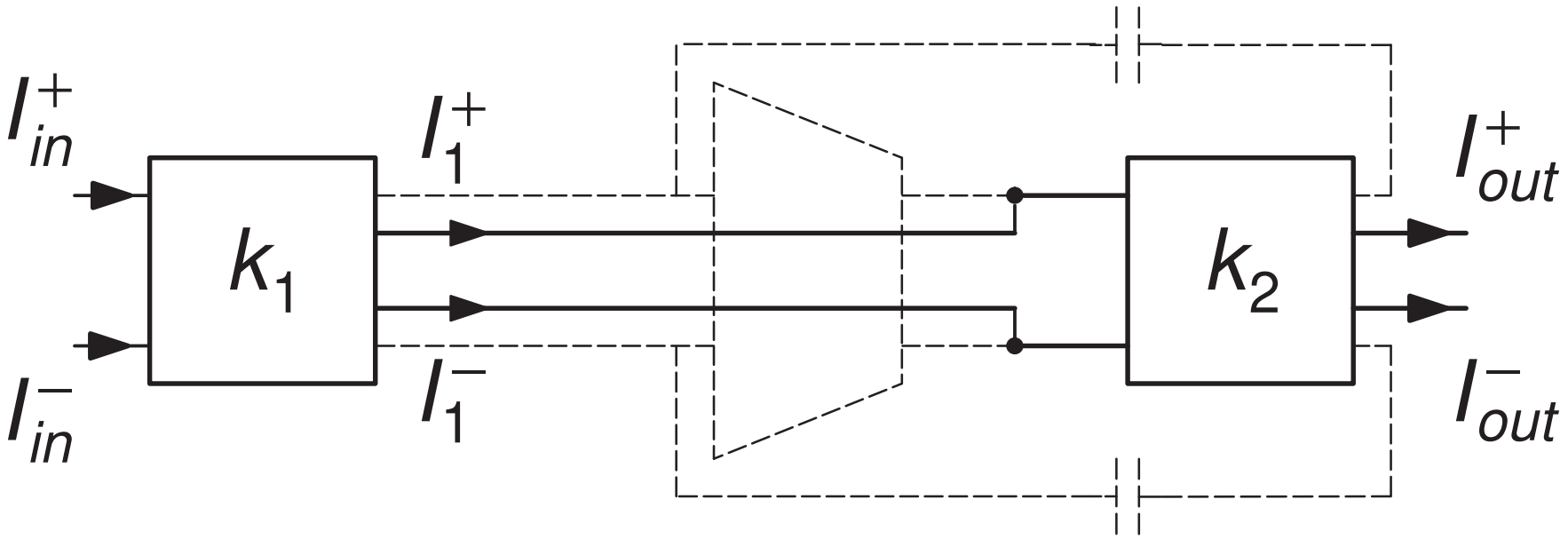
or

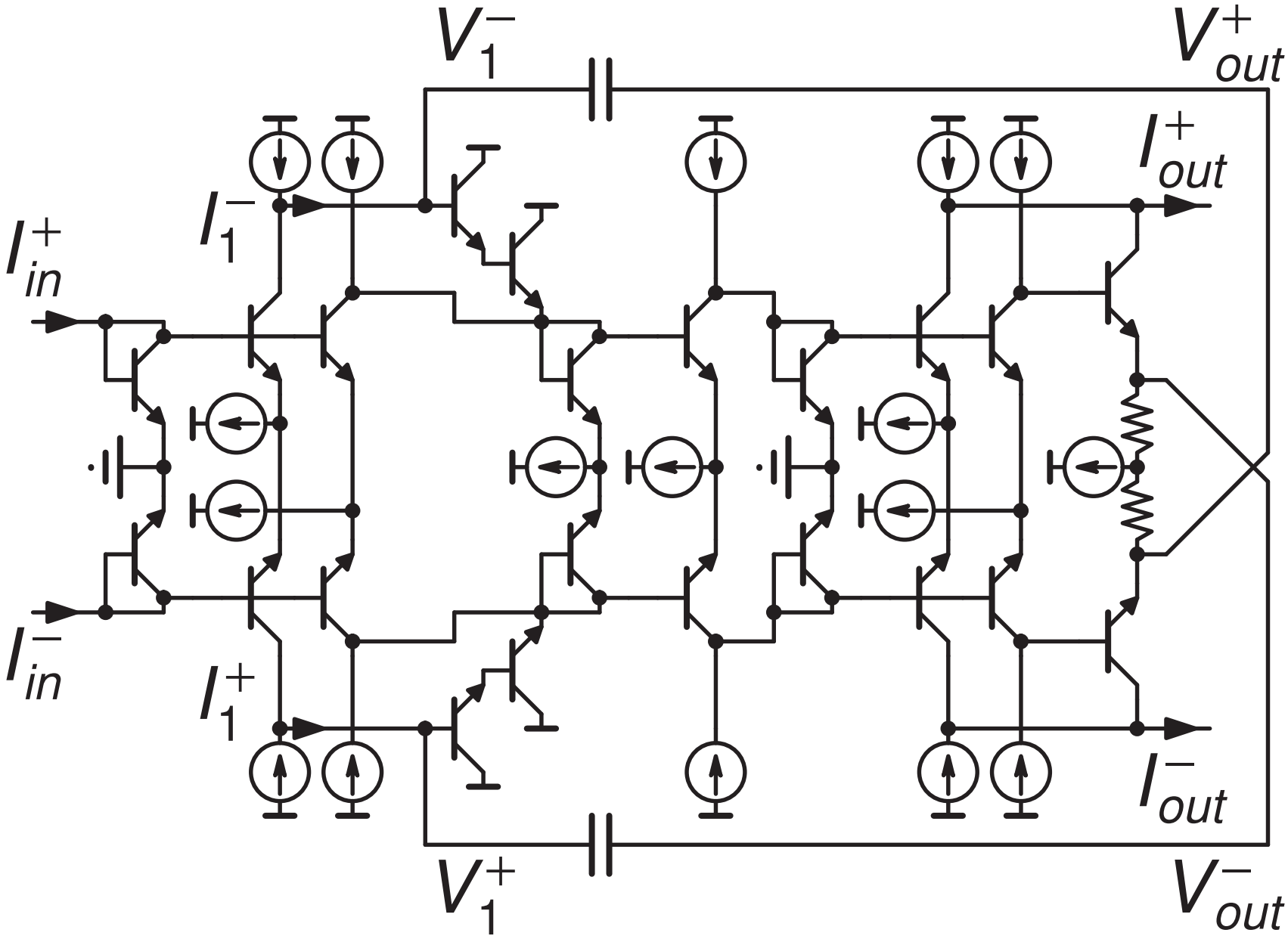


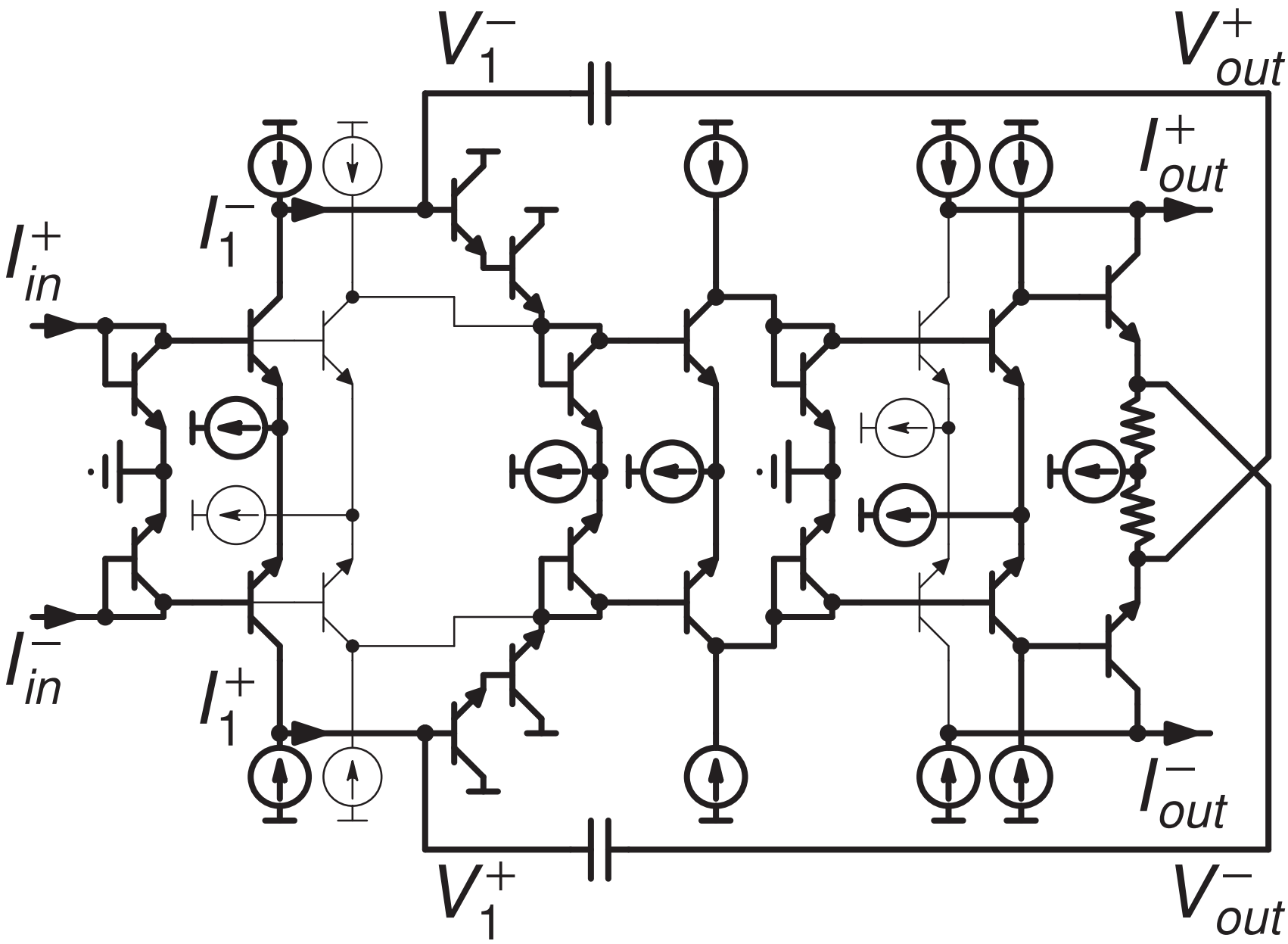
Instead, a **current-mode** implementation of a **Miller integrator** is proposed.

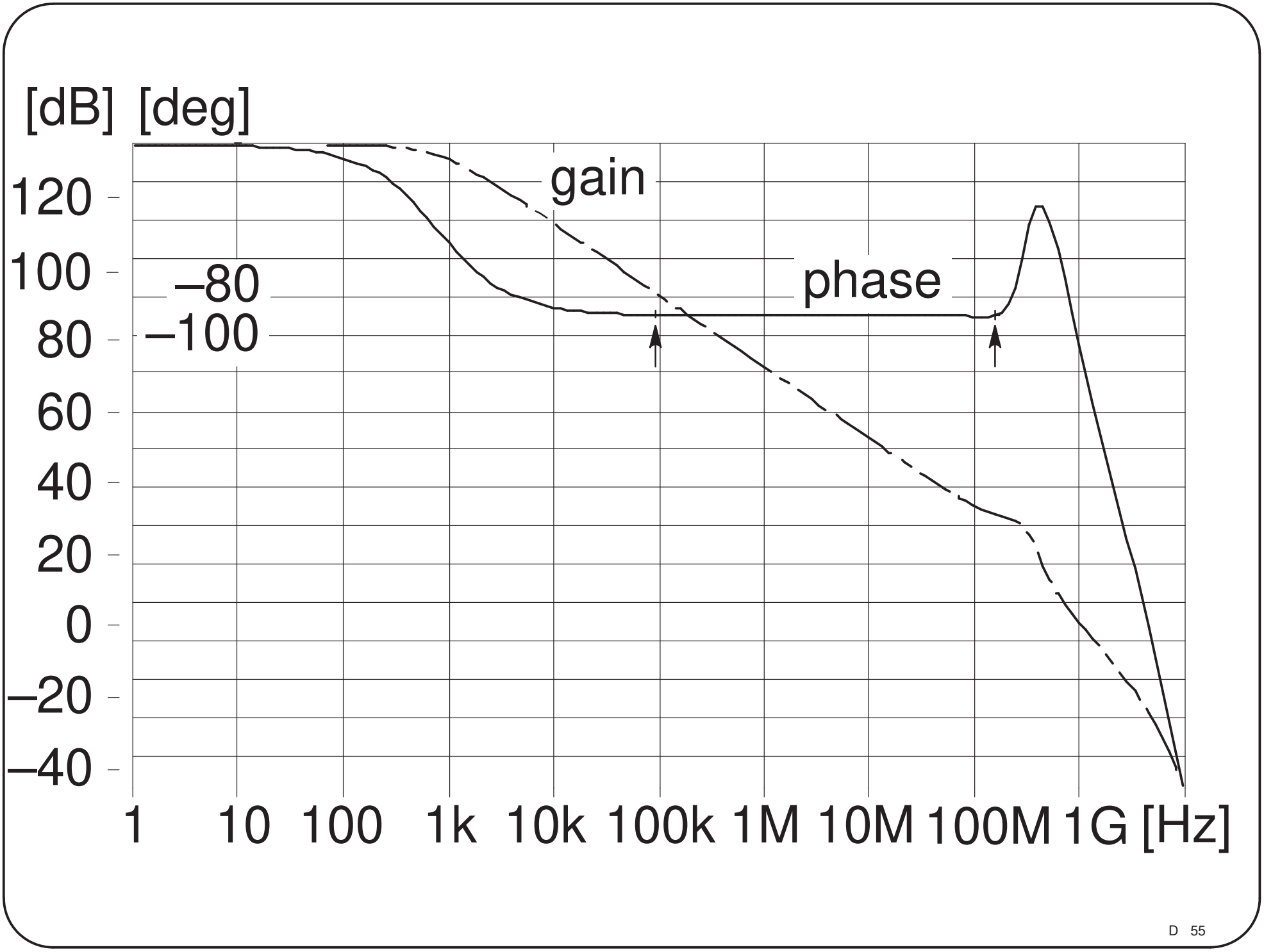


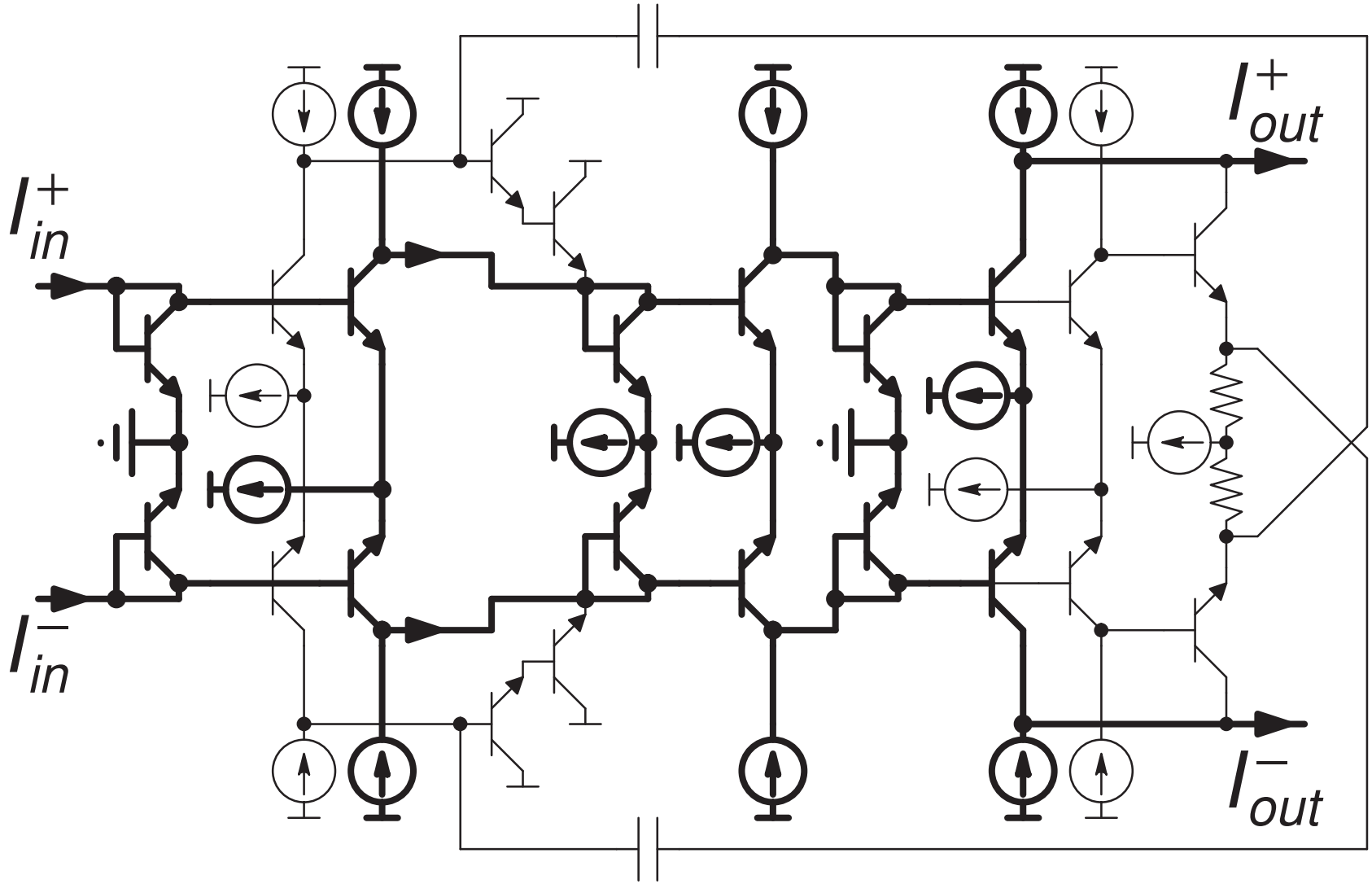

C
I_{in}^{+}
I_1^{+}
V_1^{+}
I_2^{-}
V_{out}^{-}
I_{out}^{+}
k_1
g_m
k_2
g_o
I_{in}^{-}
I_1^{-}
V_1^{-}
I_2^{+}
V_{out}^{+}
I_{out}^{-}
C

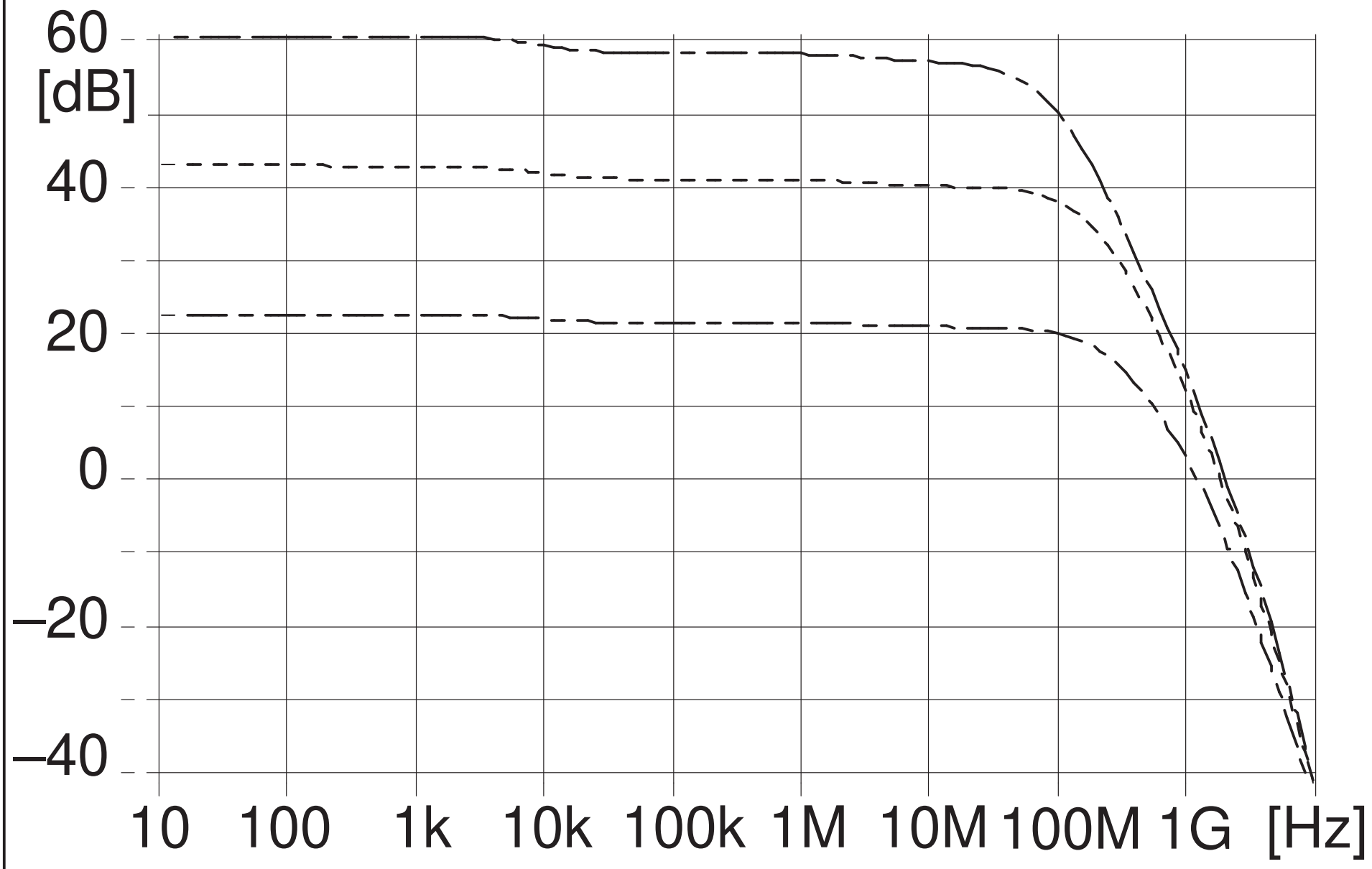

I_{in}^{+}
I_{in}^{-}
k_1
I_1^{+}
I_1^{-}
k_2
I_{out}^{+}
I_{out}^{-}


V_1^-
V_{out}^+
I_{out}^+
I_1^-
I_{in}^+
I_{in}^-
I_1^+
I_{out}^-
V_1^+
V_{out}^-


V_1^-
V_{out}^+
I_{out}^+
I_1^-
I_{in}^+
I_{in}^-
I_1^+
I_{out}^-
V_1^+
V_{out}^-


[dB]
[deg]
120
100
80
60
40
20
0
–20
–40
–80
–100
gain
phase
1
10
100
1k
10k
100k
1M
10M
100M
1G
[Hz]


I_{in}^{+}
I_{in}^{-}
I_{out}^{+}
I_{out}^{-}


60
[dB]
40
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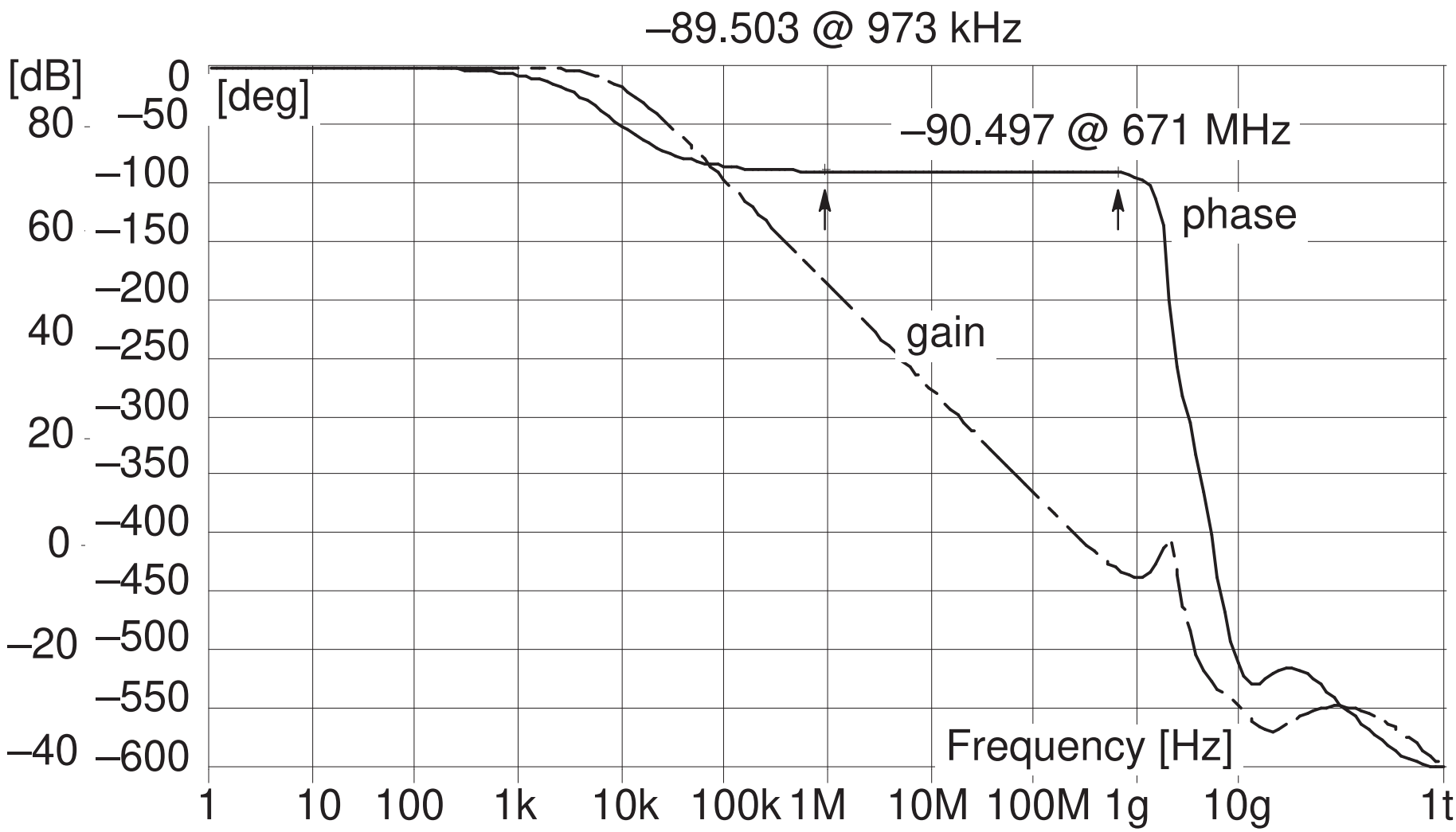
100
1k
10k
100k
1M
10M
100M
1G
[Hz]


–89.503 @ 973 kHz
–90.497 @ 671 MHz
[dB]
[deg]
80
60
40
20
0
–20
–40
0
–50
–100
–150
–200
–250
–300
–350
–400
–450
–500
–550
–600
phase
gain
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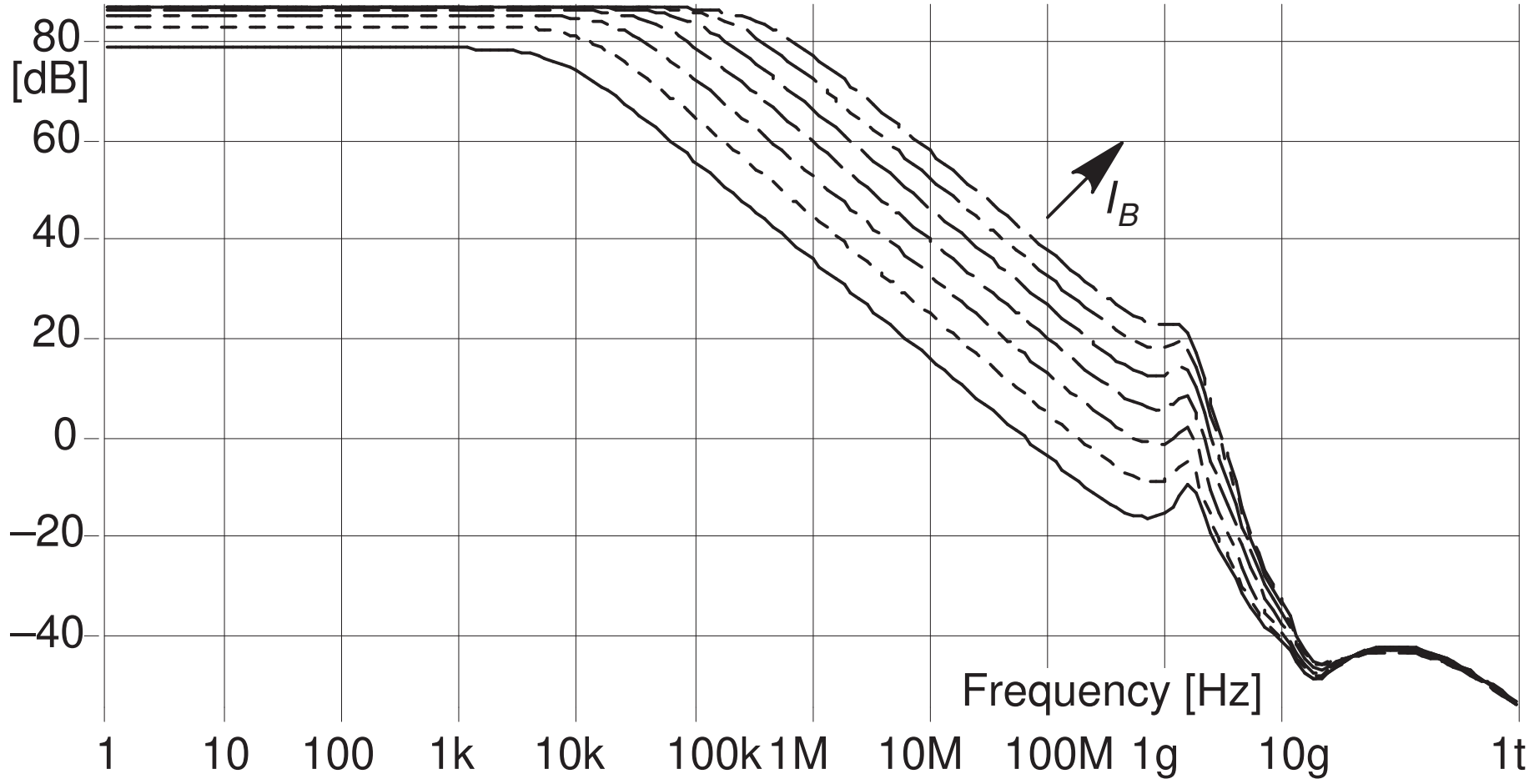
100M
1g
10g
1t


80
[dB]
60
40
20
0
–20
–40
1
10
100
1k
10k
100k
1M
10M
100M
1g
10g
1t
Frequency [Hz]
I_B

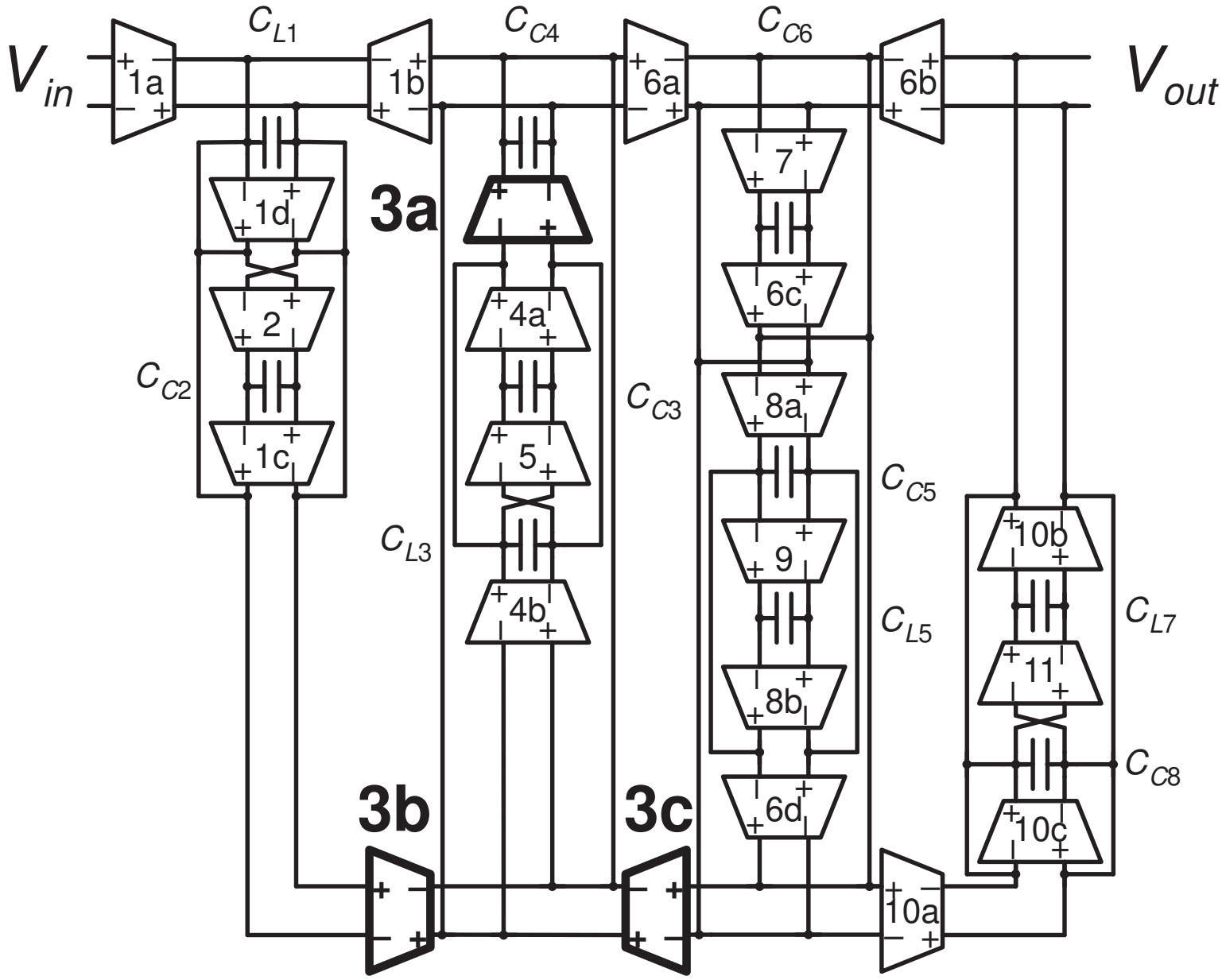
Flexibility of the proposed architecture—examples

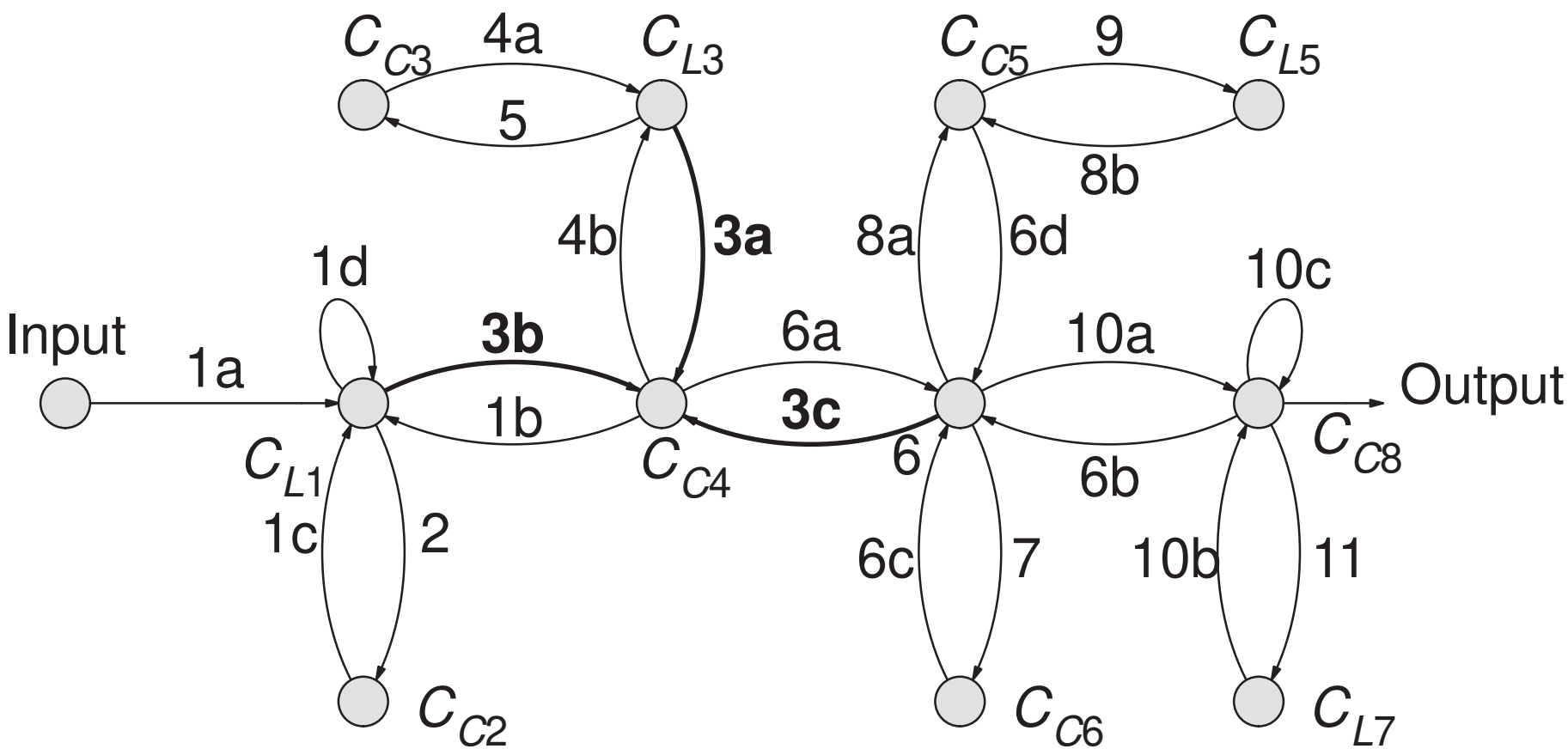
1. Continuous-time linear filter
2. Rank filter cell
3. Matrix multiplication circuit
4. Circuit for solving a system of linear equations
5. Circuit for solving a nonlinear programming problem
6. Fuzzy controller

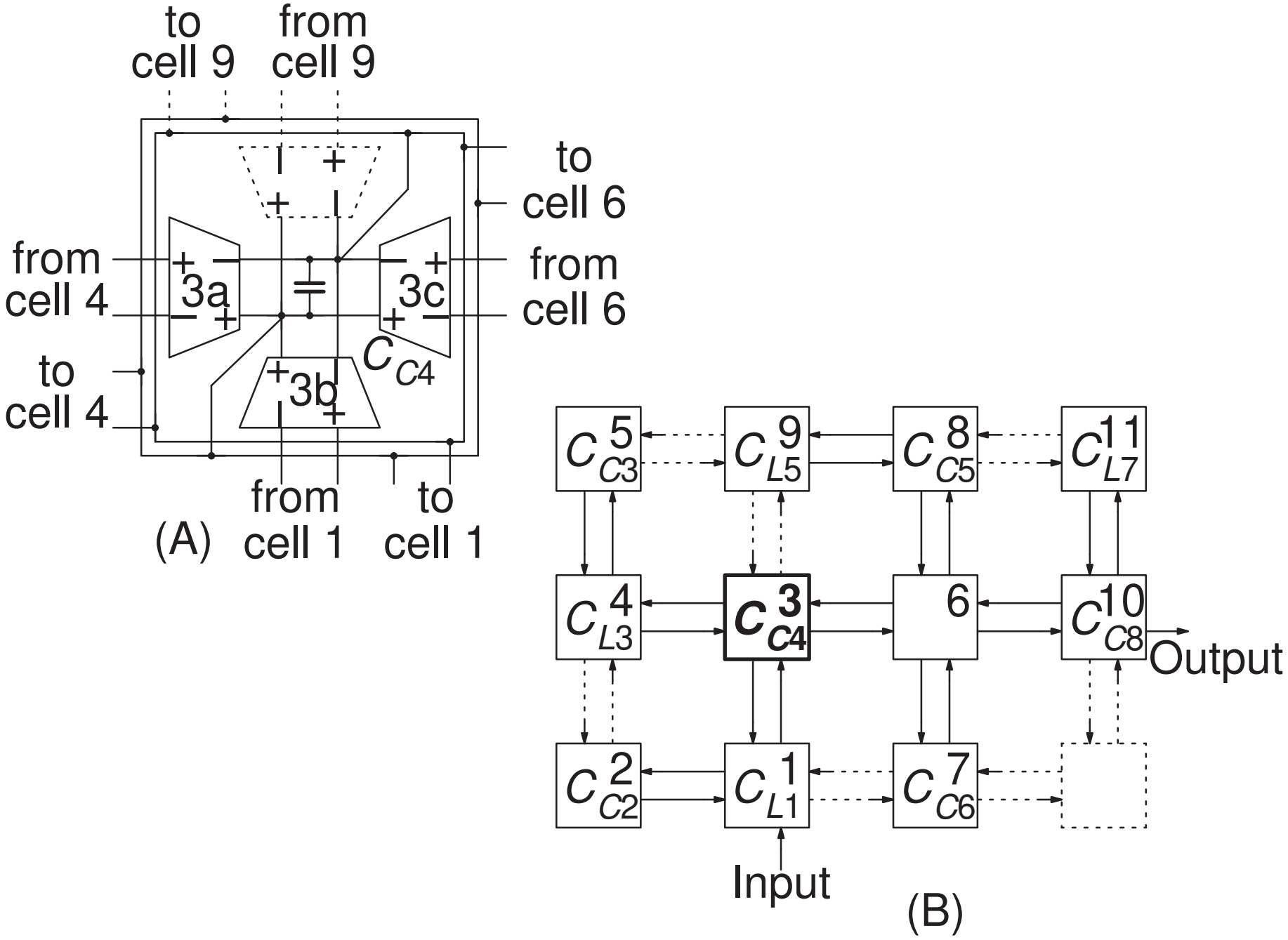
1. **Eighth-order elliptic band-pass filter**

Applications of linear filters:

- Video and voice communication
- Wireless communications
- Signal conditioning in computer disk drives
- Modems
- Voice recognition, speech systems


V_{in}
V_{out}
C_{L1}
C_{C4}
C_{C6}
1a
1b
6a
6b
1d
2
1c
C_{C2}
3a
4a
5
4b
C_{L3}
C_{C3}
7
6c
8a
9
8b
6d
C_{C5}
C_{L5}
10b
11
10c
C_{L7}
C_{C8}
3b
3c
10a

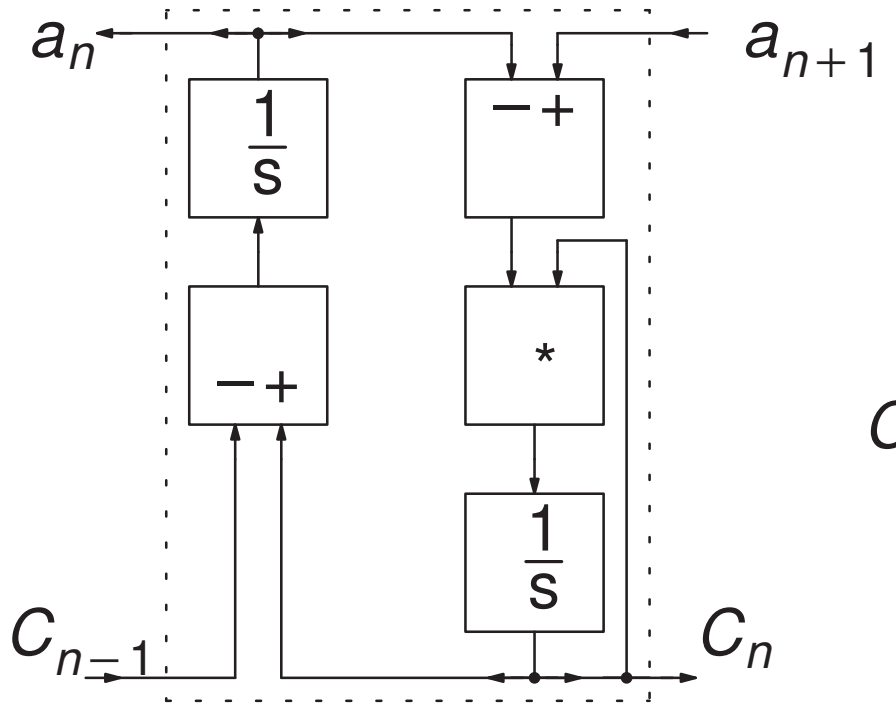

C_{C3}
4a
C_{L3}
5
C_{C5}
9
C_{L5}
8b
4b
3a
8a
6d
1d
10c
Input
3b
6a
10a
1a
Output
1b
3c
C_{L1}
C_{C4}
6
C_{C8}
6b
1c
2
6c
7
10b
11
C_{C2}
C_{C6}
C_{L7}


to
cell 9
from
cell 9
to
cell 6
from
cell 4
3a
3c
from
cell 6
C_{C4}
to
cell 4
3b
from
cell 1
to
cell 1
(A)
C_{C3}^{5}
C_{L5}^{9}
C_{C5}^{8}
C_{L7}^{11}
C_{L3}^{4}
C_{C4}^{3}
6
C_{C8}^{10}
Output
C_{C2}^{2}
C_{L1}^{1}
C_{C6}^{7}
Input
(B)

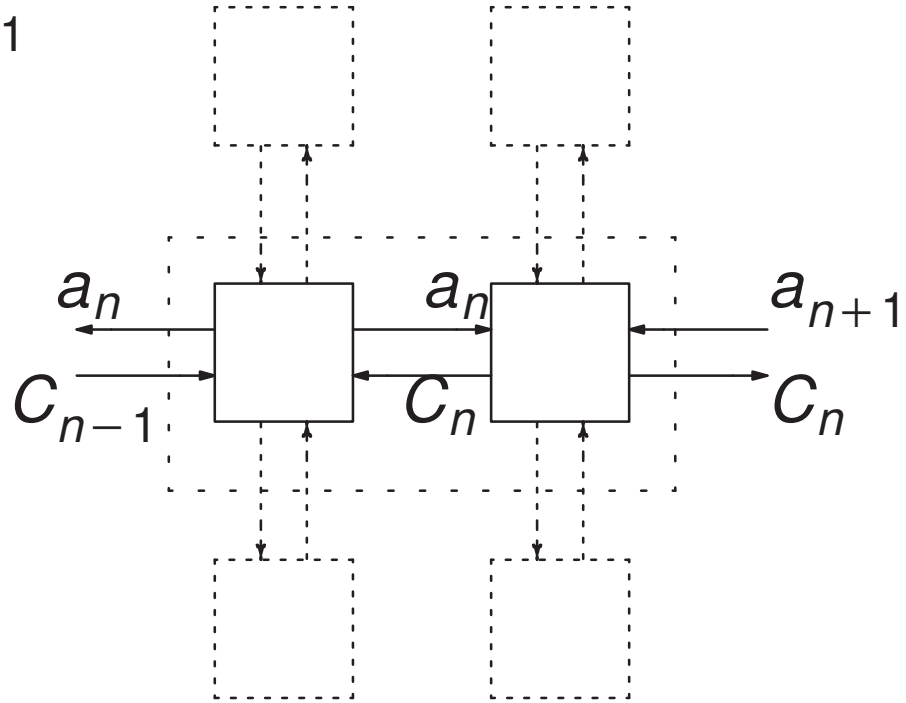
2. **Rank filter cell**

Applications:

- Image processing



(A)

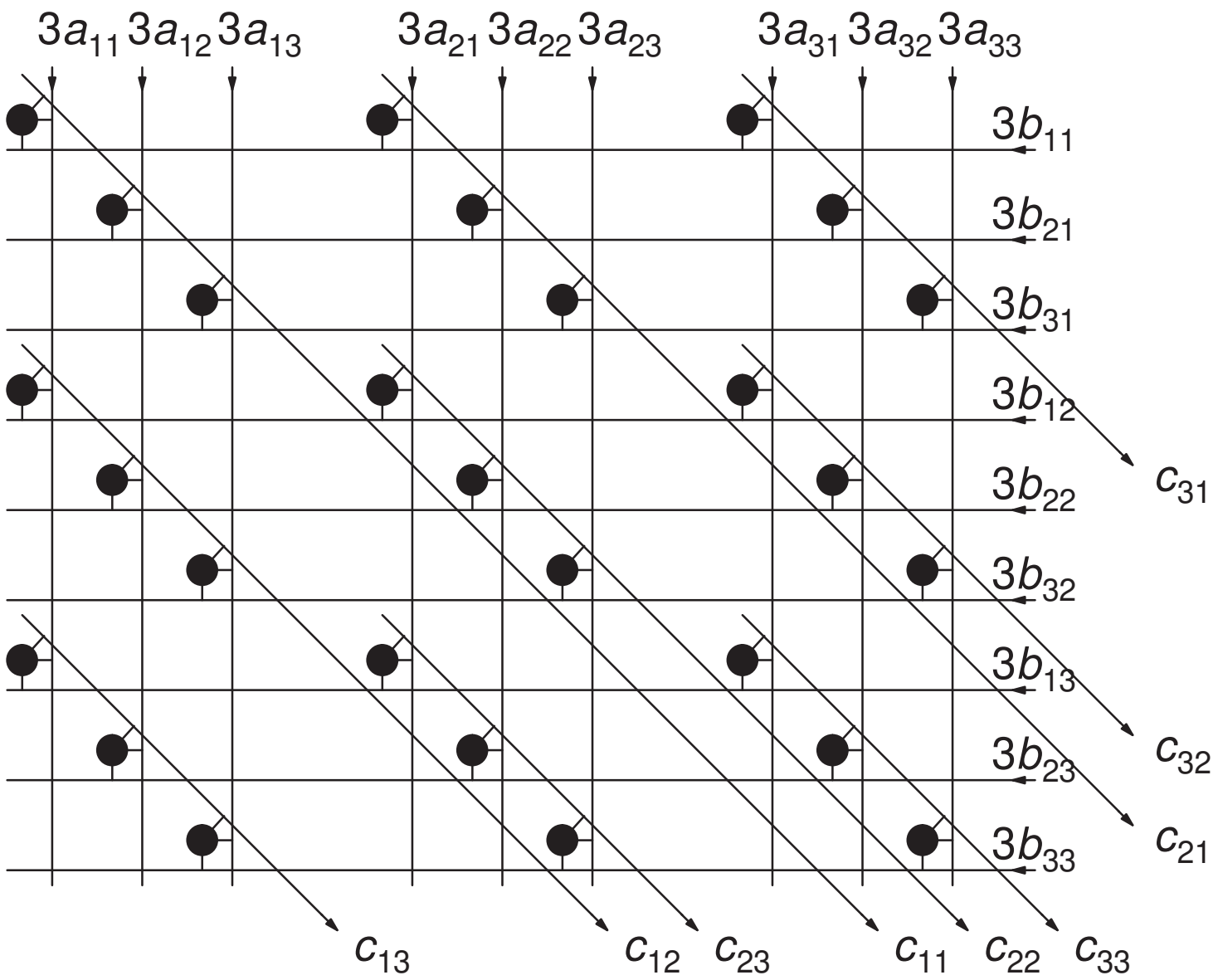


(B)

3. **Matrix multiplication circuit**

Applications:

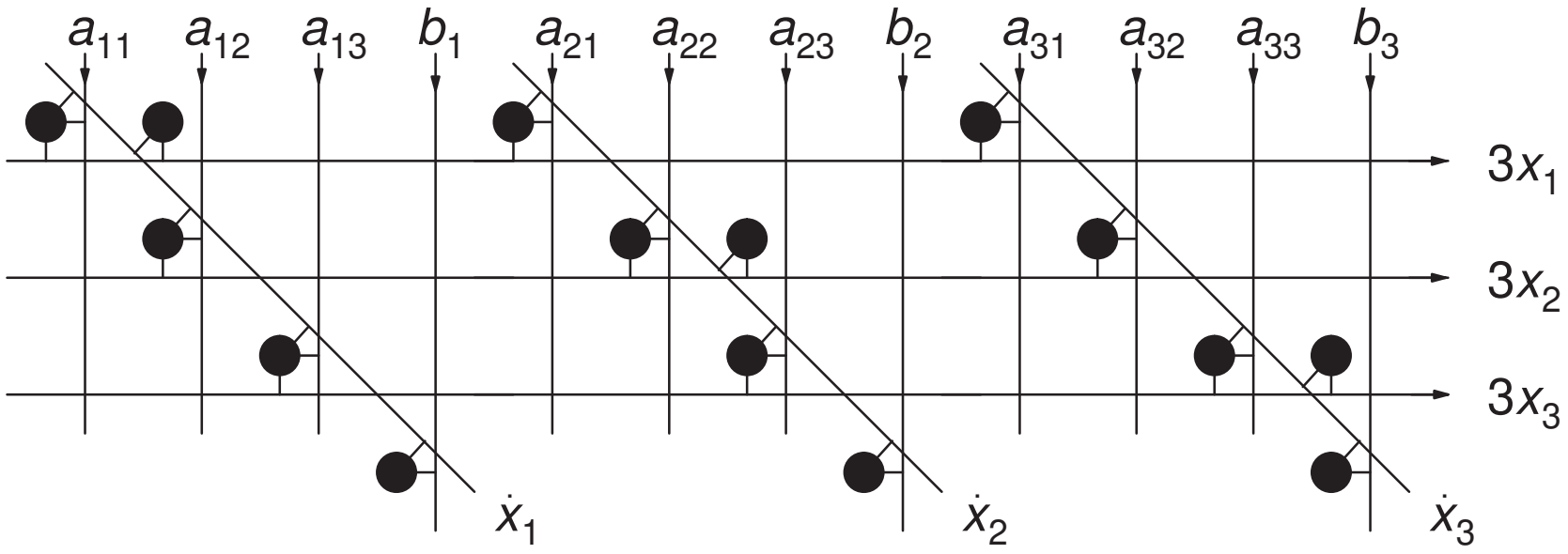
- Control (*e.g.* for robots)
- Artificial neural networks


$3a_{11}$ $3a_{12}$ $3a_{13}$
$3a_{21}$ $3a_{22}$ $3a_{23}$
$3a_{31}$ $3a_{32}$ $3a_{33}$
$3b_{11}$
$3b_{21}$
$3b_{31}$
$3b_{12}$
$3b_{22}$
$3b_{32}$
$3b_{13}$
$3b_{23}$
$3b_{33}$
c_{31}
c_{32}
c_{21}
c_{13}
c_{12} c_{23}
c_{11} c_{22} c_{33}

4. **Circuit for solving a system of linear equations**

Applications:

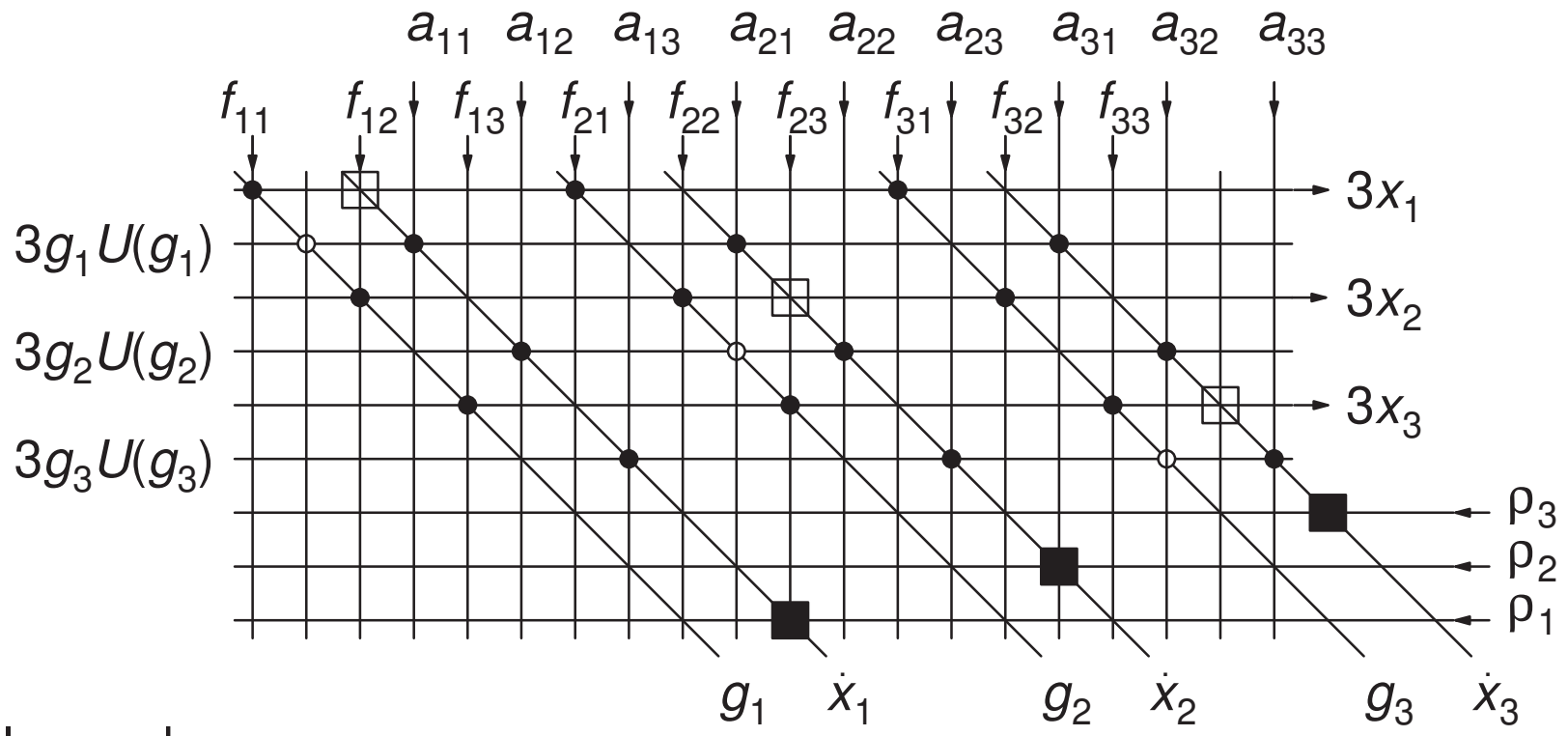
- Matrix operations
- Circuit simulation
- Combinatorial optimization


a_{11} a_{12} a_{13} b_1 a_{21} a_{22} a_{23} b_2 a_{31} a_{32} a_{33} b_3
$3x_1$
$3x_2$
$3x_3$
$\dot{x}_1$
$\dot{x}_2$
$\dot{x}_3$

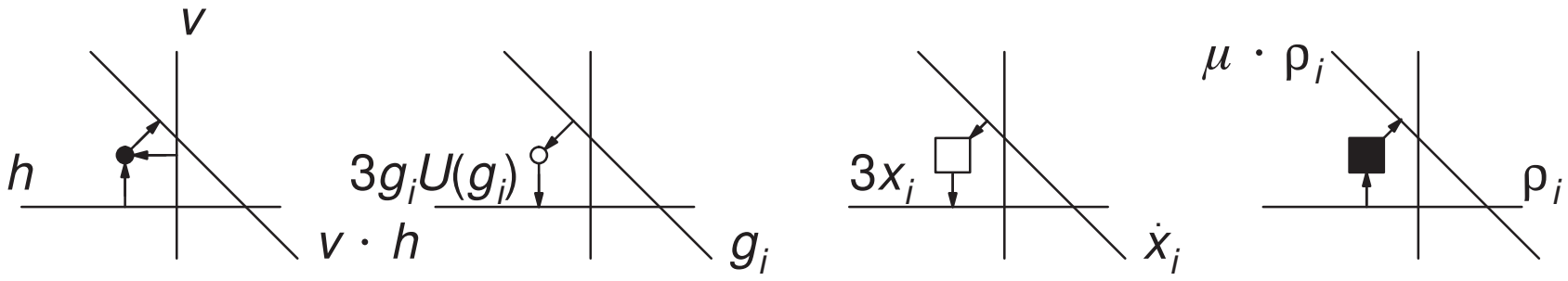
5. **Circuit for solving a nonlinear programming problem**

Applications:

- Combinatorial optimization problems
- CAD accelerator


a_{11} a_{12} a_{13} a_{21} a_{22} a_{23} a_{31} a_{32} a_{33}
f_{11} f_{12} f_{13} f_{21} f_{22} f_{23} f_{31} f_{32} f_{33}
$3g_1U(g_1)$
$3g_2U(g_2)$
$3g_3U(g_3)$
$3x_1$
$3x_2$
$3x_3$
ρ_3
ρ_2
ρ_1
g_1 $\dot{x}_1$ g_2 $\dot{x}_2$ g_3 $\dot{x}_3$

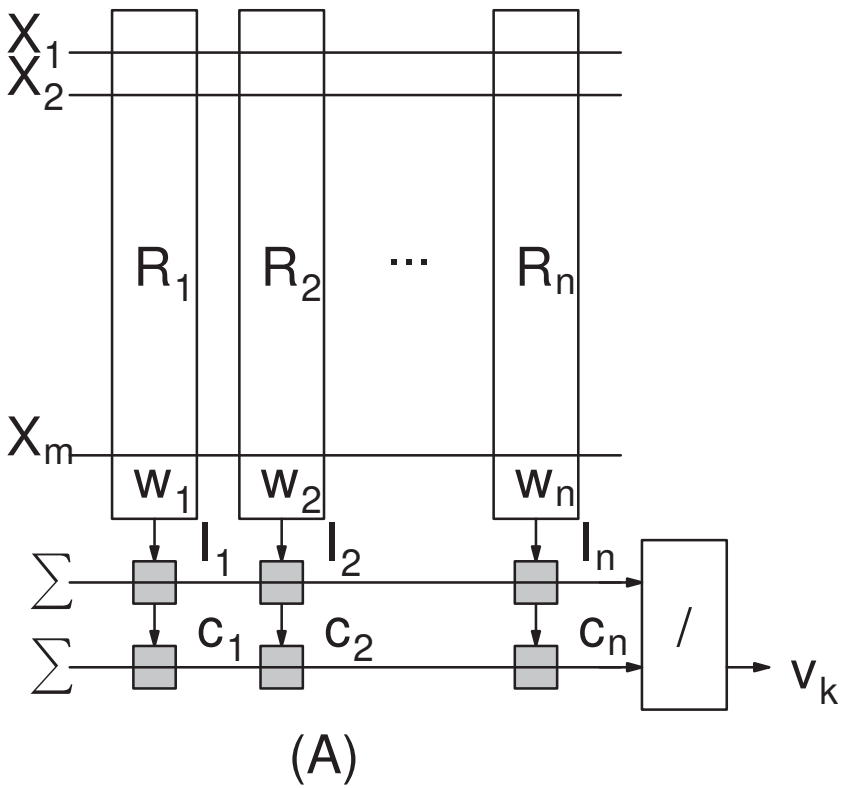
Legend:


v
h
$v \cdot h$
$3g_iU(g_i)$
g_i
$3x_i$
$\dot{x}_i$
$\mu \cdot \rho_i$
ρ_i

6. **Fuzzy controller**

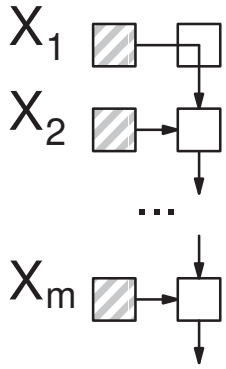
Applications:

- Robot control
- Consumer electronics
- Intelligent toys

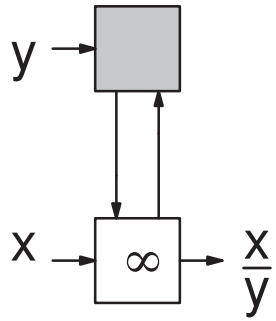


(A)

$$v_k = \frac{\sum_{i=1}^{n} w_i c_i I_i}{\sum_{i=1}^{n} w_i I_i}$$



(B)



(C)

Legend:

- product
- fuzzy set membership
- min

4. Conclusions

- Proposed research systematically addresses bandwidth limitations of the field-programmable analog devices.
- A methodology for creating flexible architectures with predominantly local signal interconnections has been outlined and exemplified. An exemplary architecture also encompasses ANNs and CNNs.
- A method of programming multi-function cells without switches in the HF signal path has been proposed and a programmable amplifier-integrator has been demonstrated.