

Ceramic Tiles Failure Detection Based on FPGA Image Processing

Željko Hocenski

Faculty of Electrical Engineering
University J.J. Strossmayer
Osijek, Croatia
zeljko.hocenski@etfos.hr

Ivan Aleksi

Faculty of Electrical Engineering
University J.J. Strossmayer
Osijek, Croatia
ivan.aleksi@etfos.hr

Robert Mijaković

Faculty of Electrical Engineering
University J.J. Strossmayer
Osijek, Croatia
robert.mijakovic@etfos.hr

Abstract: This paper presents one method about automation of tile surface and texture diagnosis. Final stage of tile manufacturing deals with surface and edge defects detection, and is still not an automated part of production. We used computer visual diagnosis and FPGA-based embedded hardware digital design to classify tiles according to surface and edge defects. In order to reduce computing time, we used tile images from line camera and the FPGA embedded parallel image processing unit designed with VHDL.

I. INTRODUCTION

One of the phases in production process that comes as last is the inspection of product quality and his classification. The most of production phases in today ceramic tiles industry has been automated from raw material preparing process, pressings of biscuits, preparing and deposition of surface texture of tile, icing to packaging and distributions, containing larger or smaller automation level. The visual inspection of ceramic tiles surface quality is performed at this phase based on the presence of the chromatic discrepancies in the tonality of surface, damages of edges and top corners, presence of crack, abrasion marks, dotted and the lob of defects, irregularities in the layout structure and texture anomaly. This phase has still the lowest level of automation in the whole manufacturing process. The inspection of product quality and his classification today in majority of cases is based on human factor because of complexities of problems of inspection and quality and demands for the changeability during decision about the classification of product. Because of the limitation of human resource in the chain of production process as managing element, man becomes the weakest managing chain link [1].

As tile comes from automated production chain to final manufacturing line its surface and edges are inspected by the stuff employed to detect tile defects. In order to avoid human errors in the system, complete automation of tile production is required. Thus, in this work, we presented a tile defect detection based on Field Programmable Gate Array (FPGA) technology. FPGA represents digital integrated components of configurable logic blocks (CLB) with configurable interconnecting blocks. Such devices can be configured for execution of various computationally expensive tasks. Tasks include applications with exhaustive data enumeration as it is the case in the medicine image

analysis, the computer vision, the digital components emulation, etc. One of those applications is the ceramic tile surface and texture diagnosis. Due to large resolutions and dimensions of objects, all calculations included can't be processed on a PC in a predefined time interval [2][3]

After introduction, applied tile diagnosis methodology is proposed in section 2. Ceramic tile manufacturing line with an automated FPGA-based surface and edge defects detection system is presented in Section 3. Section 4 deals with VHDL digital design implementation and its features. Experimental results are presented in section 5. Section 6 concludes this paper.

II. CERAMIC TILE SURFACE DEFECT DETECTION METHODS

In some papers researchers decided to use statistical methods [2] and wavelet transformation [3][4][5] for detecting tile errors. Those are sophisticated methods. However, we decided to use a simple and efficient method that is relatively easy to implement with VHDL. In contrast to [2], higher resolution image is used with 1024 pixels per line. In this way, proposed method is able to find defects with 0.1 mm pixel size. There are different methods for scanning tiles such as putting scanner directly on production line [6], image acquisition with area scan camera [7],[4] and a line scan camera [8]. However, we presented a method with line scan camera [9] and FPGA image processing unit [6][10][11]. Different methods are useful for different kinds of ceramic tiles (plain and textured). Our method is constrained to plain ceramic tiles. Other works include FPGA image processing using convolution kernels that can be well implemented for ceramic tile failure detection [6]. Similar method with simpler algorithm is presented in this work. FPGA implementations are much faster in image processing algorithms than a traditional PC based implementations.

FPGA advantages are in spatial and temporal parallel computing. Reference [10] depicts timing constraints with 40(ns) pixel processing time, limited on-chip block RAM (BRAM) and 256 x 8-bit look-up table constraint. Authors presented point, window and point operations in an embedded system such as FPGAs.

III. CERAMIC TILE SURFACE AND EDGE DEFECTS DETECTOR

Final phase of tile production is the tile surface and edge inspection [12]. This phase of tile production is a human phase where tiles should be sorted according to their quality class. Human based errors are avoidable with complete automation of manufacturing process. Such manufacturing line is illustrated in Fig.1. After ceramic tile is produced and delivered to failure detection line, its image is obtained with a line scan camera that is vertically placed in relation with failure detection line. Line scan camera obtains single line of complete image. As manufacturing line moves with constant speed, lines differ among each other. Line capturing is triggered with tile sensor placed before the line scan camera. Pixels are then sent as the 3.3(V) Low Voltage Differential Signal (LVDS). Complete image is obtained by scanning certain amount of lines. Ceramic tile scanned image line is transferred to the FPGA's on-chip block RAM memory in a line form [13]. As a result, FPGA activates a tile class printer attached near tile sensor. Printer prints marks on tiles according to their quality class [14]. Printed marks are input parameter to a ceramic tile classifier that follows at ceramic tile production line.

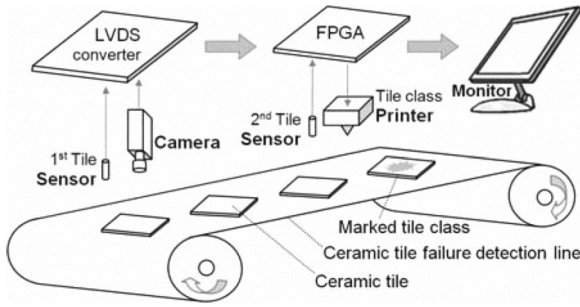


Fig.1. Ceramic tiles failure detection at production line.

We designed LVDS converter that convert signals from LVDS 3.3(V) to unipolar digital level. Latest FPGA chips have integrated LVDS converters, such as Spartan-3E, Virtex-4, Virtex-5, and latest. Since we used older Spartan3 Starter Kit [15], we designed LVDS converter, which has three LVDS Receivers [15] and one LVDS Driver [17], as it is illustrated in Fig.2 (two of three receivers are displayed).

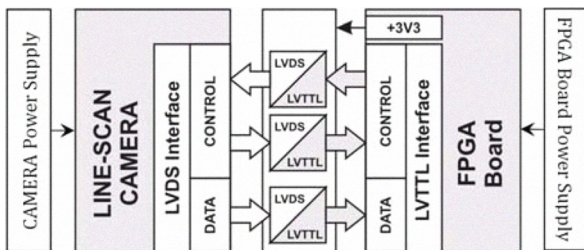


Fig.2. The 3.3(V) LVDS to unipolar digital signal converter.

Fig.3 represents functional block diagram of proposed FPGA digital design. Data sent from camera are converted and saved to FPGA's SRAM memory in 1024x8-bit form for a single scanned line. Since image is gray scaled, pixels are stored as 8-bit data. Data bus is 8-bit long and is used for delivering 8-bit pixel data to SRAM controller and XGA graphic display controller. XGA controller is used for image displaying and as tile image defect detection process monitoring. When a tile image is processed, function controller informs printer controller about tile quality class. According to tile quality class, printer marks tiles with appropriate tile quality class mark. Tile class mark coordinates tile classifier to classify tiles accordingly.

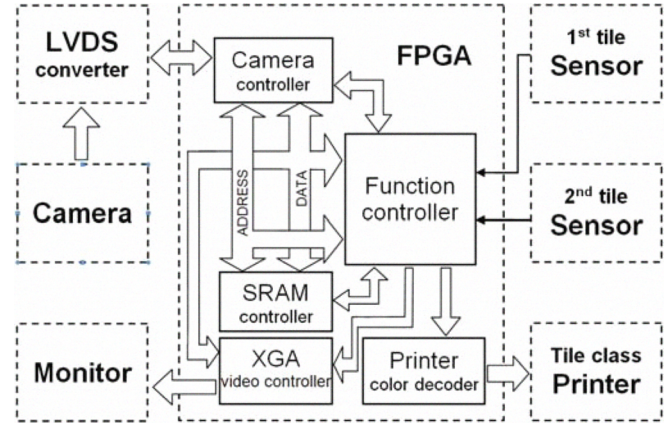


Fig.3. Block diagram of FPGA digital design for tile failure detection with its surrounding environment.

However, good tile has no surface or edge defects. On the other hand, typical tile surface model with texture defects on it is proposed in Fig.4. Tile image is displayed with light pixels, tile background and tile surface defects are displayed with dark pixels. Over proposed tile, scanned pixels are formed in lines, thus representing lines from line scan camera in that way. Such pixel lines are displayed with gray dotted lines in Fig.4. Line is acquired relative to the referent S_0 camera coordinate system. Tile coordinate system S_T is expected to be relatively little slanted in relation to S_0 . However, we assumed that tile manufacturing line has installed mechanical parts which override problems dealing with slanted tile position.

Fig.4 represents white and black ceramic tile image [3] Detected white and black pixels along scanned lines are illustrated in Fig.4. White pixel corresponds to number 255, while black corresponds to 0. Real world ceramic tile image pixel intensities are gray scaled, when image is obtained with gray scale line scan camera [9], as it is illustrated in Fig.5. Threshold level must be set in order to determine pixel intensity [18] (Fig.5). Threshold level can be either a fixed or a variable value in accordance to neighbor pixels in the line. Changes in pixel intensity from light to dark are presented in Fig.5 in dependency with x_0 -axis.

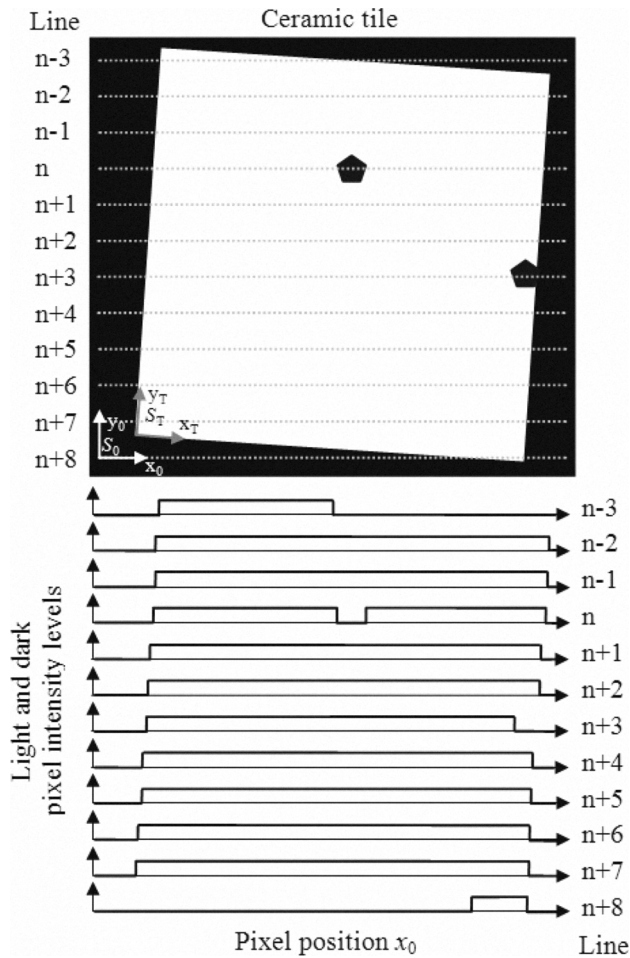


Fig.4. Black and white ceramic tile image model and pixel intensity levels along scanned lines.

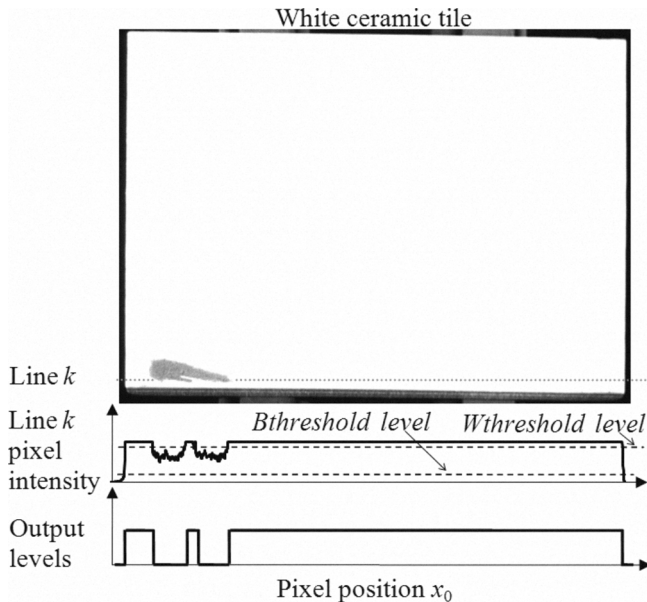


Fig.5. Real ceramic tile image with light and dark pixels (top), pixel intensities (middle) and output levels (bottom).

Ceramic tile surface defects may be determined by malfunctions in output pixel intensity levels. Fig.4 illustrates pixel intensity levels along scanned line. When light pixel occurs, it is denoted with *High* (H) output level and when dark pixel occurs it is denoted with *Low* (L) pixel in the output level along scanned line. With black and white ceramic tile image model (Fig.4.), it is easy to differentiate light from dark pixels. However, with real ceramic tile images light and dark pixels differs in certain pixel intensity amount, as it is illustrated in Fig. 5. In order to differentiate light and dark pixel intensity levels, a threshold levels must be set. If pixel intensity value is higher (lower) than the threshold level, then the light (dark) pixel is detected. Fig.5 illustrates single threshold level value, while several threshold values may be defined. One threshold level may be defined for light, and one for dark pixel intensity levels, forming pixel intensity hysteresis in that way.

IV. DIGITAL DESIGN IMPLEMENTATION

In this section we described our digital design implemented into Xilinx Spartan3 developer board with the XC3S200 FT256 FPGA chip included. We used XilinxISE 10.1 WebPack for synthesis and ModelSim 6.2 for simulation, with its VHDL designing environment. Main part of proposed digital design is finite state machine (FSM) [10][11], which state diagram for ceramic tile failure detector is proposed in Fig.6. The FSM states are presented with bold caps letters inside a circle, while conditions for switching between states are displayed with regular letters beside a directed line [11]. The FSM states (Fig.6) are proposed in following text in accordance with the FSM's analogous algorithm Alg.1.

A. Image acquisition

During the *INIT* initial state (Fig.6), image line is captured from line scan camera in form of 1024 pixels. Image line is sent from line scan camera in bytes of 8-bit gray scaled pixels and is stored in FPGA's on chip block RAM. While tile image line is scanned, all processing is done for previously scanned tile image line, since t_p image processing time is shorter than t_A image acquisition time.

B. Threshold level adjustment

In *INIT* state all variables (signals) are set to its appropriate value according to the number of current image line. Image line counter resets externally when 1st *tile sensor* (Fig.1) detects a new tile. Line counter counts for 1024 lines and then halts until the new line signal from 1st *tile sensor* appears. In *INIT* state, two threshold levels are set to default levels that are the same for all pixels along the scanned line. Threshold level for light pixels, denoted with *Wthreshold*, and *Bthreshold* for dark pixels. Threshold level is calculated (Alg.1 line 3) according to average levels of neighbor pixel intensity levels, even though it can be set to a fixed value.

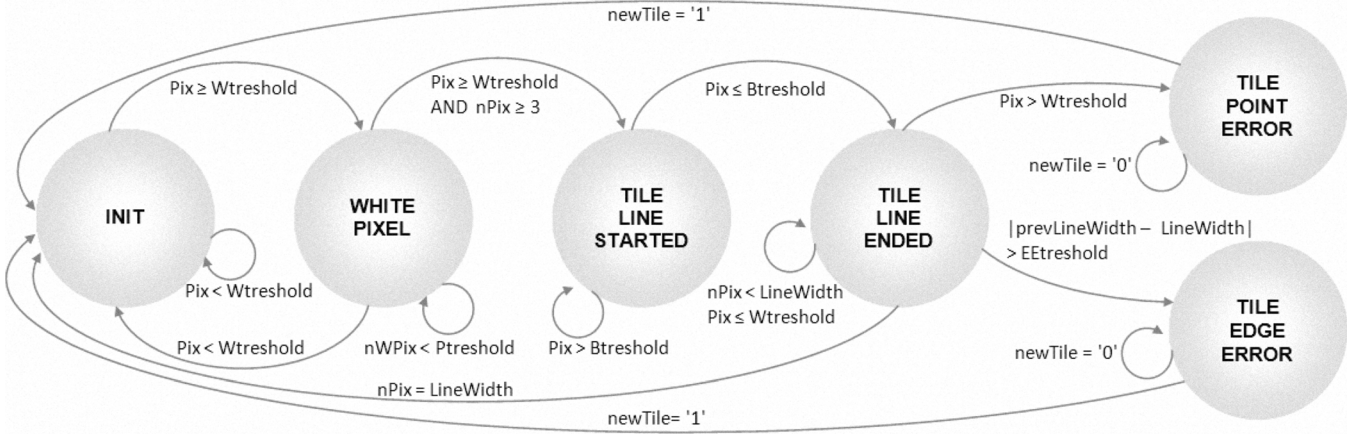


Fig. 6. State diagram of finite state machine (FSM) for proposed ceramic tile surface and edge defects detector.

C. Surface defect detection

This section deals with grayscale ceramic tile image surface defect detection. Surface defect detection is used to detect tile surface texture defects [5][19]. Method is based on comparison of pixels in a single line with threshold value of pixel intensity enumerated for each line individually [2].

In preprocessing *INIT* state, one line of pixels is stored in FPGA's on-chip RAM. At the same time, a line's average pixel intensity value is calculated and stored into the *Function controller* (Fig.3) registers. Threshold value is enumerated from average value of pixels intensity along stored line according to following rules (Alg.1, line 3). There are two registers storing value of threshold levels, *Wthreshold* and *Bthreshold* and are used for higher boundary levels and their values are calculated as an average value with fixed offset. It is true that threshold levels satisfy equation $Wthreshold > Bthreshold$.

Subsequently, (Alg.1, line 4) pixels are compared with *Wthreshold* value that is stored in *Function controller register*. When there is a pixel with higher intensity than *Wthreshold*, the FSM goes to state *WHITE PIXEL* from state *INIT*. This state means that tile line started. Delay is required in order to avoid pixel intensity bouncing. Thus, the proposed FSM is designed to go to state *TILE LINE STARTED* when more than three pixels with intensity value higher than *Wthreshold* occurs (Alg.1, line 4). *TILE LINE STARTED* state leads to *TILE LINE ENDED* state when there are more than three pixels with intensity levels below *Bthreshold* (Alg.1, line 5). After this FSM's state sequences, all of the following pixel intensity values are required to be below *Bthreshold* value. Otherwise, either *TILE POINT ERROR* or *TILE EDGE ERROR* occurs. If any of those pixel intensity values goes over *Bthreshold* value, the FSM results with the *TILE POINT ERROR* state, meaning that surface defect is detected. Printer marks such tile with appropriate surface defect tile color. This is the case with holes and dirt [18][18].

Algorithm 1. Tile defect detection

```

1: InitializeValues();
2: while(nextLine = GetNextLine())
3:   InitializeTresholdLevels();
   LineStarted = LineEnded = TileError = FALSE;
   LineLength = 0;
   while(nextPixel = GetNextPixel())
4:     if(pixel > WhiteThreshold and nPix > 3)
       nPix++;
       TileLineStarted = TRUE;
5:     if(TileLineStarted and pixel < BlackThreshold)
       LineEnded = TRUE;
6:     if(TileLineStarted and pixel > BlackThreshold)
       LineLength++;
7:     if((pixel > WhiteThreshold and LineEnded) or
       (|prevLineLength - LineLength| > LineTolerance))
       TileError = TRUE;
   end while
8:   prevLineLength = LineLength;
end while

```

D. Edge defects detection

In this work, simple edge defect detection algorithm is considered with white tile surface images on dark manufacturing line background. When maximal tile line length is reached, white pixel part of scanned line is compared with the length of white part of previous line. When those lengths differ more than tolerance *Ethreshold* edge error threshold value, the FSM goes to *TILE EDGE ERROR* state (Alg.1, line 5). From this state the FSM goes to *INIT* state when 1st tile sensor detects a new tile. Printer marks such tile with according color for edge defect tiles.

V. EXPERIMENTAL RESULTS

We used FPGA parallel embedded digital design that is configured to process tile surface image in order to assign tile quality class. Processing time may be evaluated in accordance with eq. (1):

$$t = t_A + t_L, \quad (1)$$

where symbols correspond to:

- t - total time for processing image;
- t_A - time to acquire whole image;
- t_L - time to process last line.

Image processing time t_p is much shorter than the image line acquiring time t_A .

Algorithm 1 is implemented in C++ programming language. The experiment is done on PC with T7300 processor under WindowsXP. On the other hand, expected FPGA performances are calculated on a given frequency of 75(MHz). Image acquisition time t_A is calculated from [9] and t_L is the time for processing last line.

TABLE I
IMAGE PROCESSING EXECUTION TIMES

Tile dimensions	Image resolution	Time	Measured PC application (μs)	Expected XC3S200 FPGA performances (μs)
100 x 100 mm	1024 x 1024 pixels	t_A	117.350,40	117.350,40
		t_L	500.000,00	13,65
		t	617.350,00	117.364,05
100 x 200 mm	1024 x 2048 pixels	t_A	234.700,80	234.700,80
		t_L	984.000,00	13,65
		t	1.218.500,00	234.714,45
200 x 200 mm	2048 x 2048 pixels	t_A	444.416,00	444.416,00
		t_L	2.047.000,00	27,31
		t	2.491.416,00	444.443,31

Results presented in Table I show that this kind of embedded approach downside is only in image acquisition time, while processing time is relatively short. Table I. illustrates line processing time with constant 75(MHz) operating frequency, while Table II illustrates maximal possible operating frequency of proposed design.

TABLE II
MAXIMAL OPERATING FREQUENCY OF THE FSM.

Xilinx FPGA family	Xilinx FPGA device	f (MHz)	t_L (μs)
Spartan 3	xc3s200-5-vq100	91.4	11,20
Spartan 3E	3s1600efg320-5	105.9	9,67
Virtex 4	4vlx15sf363-12	198.5	5,16
Virtex 5	xc5vlx30t-3-ff665	199.8	5,13

The FPGA devices proposed in Table II illustrate that latest FPGA's have better performances. However, the use

of latest technology increases timing performances for approximately 50%. Table II. illustrates line processing times, i.e. time to process last line t_L , which is calculated according to (eq. 2).

$$t_L = \text{Number of pixels per line} / f. \quad (2)$$

The choice of FPGA has impact on maximal operating frequency. However, digital design optimization may improve final results even more [20].

VI. CONCLUSION

The FPGA parallel embedded digital design is used and configured to process tile surface image in order to assign tile quality based on tile surface and texture defects. Analogous C++ algorithm was proposed, and comparison with implemented method is presented. The Xilinx's Spartan-3 XC3S200 FT256 FPGAs simple modeled implementation performances are about 6 times faster than standard PC based algorithm implementation.

ACKNOWLEDGMENT

This work is done under the project with grant number: 165-036-1621 2000.

REFERENCES

- [1] V.Hocenski, Z.Hocenski, S.Vasilic, „Application of Results of Ceramic Tiles Life Cycle Assessment due to Energy Savings and Environment Protection”, *IEEE International Conference on Industrial Technology*, IEEE ICIT 2006, Mumbai, India, pp. 2972-2977, 2006.
- [2] C. Boukouvalas, J. Kittler, R. Marik, M. Petrou, M.:“Automatic grading of ceramic tiles using machine vision”, *Industrial Electronics, 1994. Symposium Proceedings, ISIE '94*. ISBN: 0-7803-1961-3, pp. 13-18, Santiago, 25-27 May 1994.
- [3] Z. Hocenski, S. Rimac-Drlje, T. Keser, “Automatic Inspection of Defects in Plain and Texture Surfaces”, *Proc.5th IEEE Int. Conf. Intelligent Engineering Systems 2001, INES 2001*, On Viking Line m/s Mariella on route Helsinki, Finland - Stockholm, Sweden - Helsinki, Finland, pp.221-227, 2001.
- [4] H.M. Elbehriy, A.A. Hefnawy, M.T. Elewa, "Visual Inspection for Fired Ceramic Tile's Surface Defects using Wavelet Analysis", *ICGST-GVIP Journal*, Vol. 5, Issue 2, 2005.
- [5] H. Elbehriy, A. Hefnawy, M. Elewa, "Surface Defect Detection for Ceramic Tiles Using Image Processing and Morphological Techniques", *Proceedings of World Academy of Science, Engineering and Technology*, Vol. 5, p.p.158-162, 2005.
- [6] I. Bravo, P. Jiménez, M. Mazo, J.L. Lázaro, E. Martín: “Architecture Based on FPGA's for Real-Time Image Processing”, *Reconfigurable Computing: Architectures and Applications*, ISBN: 978-3-540-36708-6, pp. 152-157, Berlin, 03. August 2006.
- [7] D.O. Aborisade, T.S. Ibiyemi, "Ceramic Wall Tile Quality Classification Traing Algorithms Using Statistical Approach", *Research Journal of Applied Sciences*, Vol. 12, p.p.1255-1260, ISSN:1815-932X, 2007.
- [8] Z. Hocenski, T. Keser, A. Baumgartner, "A Simple and Efficient Method for Ceramic Tile Surface Defects Detection", *IEEE International Symposium on Industrial Electronics, ISIE 2007.*, ISBN: 978-1-4244-0755-2, pp. 1606 – 1611, Vigo, 4-7 June 2007.
- [9] Datasheet: UNILINE-2048 CCD Monochrome Line Scan Camera; 031 / CEUNILINE-2048 / October 2000.

- [10] C. T. Johnston, K. T. Gribbon, D. G. Bailey: "Implementing Image Processing Algorithms on FPGAs", http://sprg.massey.ac.nz/pdfs/2004_ENZCON_118.pdf
- [11] S. Heinzle, G. Guennebaud, M. Botsch, M. Gross: "A hardware processing unit for point sets", *Proceedings of the 23rd ACM SIGGRAPH/EUROGRAPHICS symposium on Graphics hardware*, Sarajevo, ISBN :1727-3471 , 978-3-905674-09-5, pp. 21-31, 2008.
- [12] Z. Hocenski, T. Keser, "Failure detection and isolation in ceramic tile edges based on contour descriptor analysis", *Mediterranean Conference on Control & Automation, 2007. MED '07.*, ISBN: 978-1-4244-1282-2, pp. 1-6, Athens, 27-29 June 2007.
- [13] Datasheet: SRAM IS61LV25616AL, 256K x 16 HIGH SPEED ASYNCHRONOUS - CMOS STATIC RAM WITH 3.3V SUPPLY, 1-800-379-4774, Rev. F, February 2006.
- [14] C.E. Costa, M. Petrou: "Automatic registration of ceramic tiles for the purpose of fault detection", *Machine Vision and Applications*, Vol. 11, Num. 5, pp. 225-230, Berlin, 20. September 1999.
- [15] Datasheet: Spartan-3 FPGA Family, DS099, 25. June, 2008.
- [16] Datasheet: DS90LV032A 3V LVDS Quad CMOS Differential Line Receiver, DS100095, July 1999.
- [17] DS90LV031A 3V LVDS Quad CMOS Differential Line Driver, DS100067, July 1999.
- [18] A. Monadjemi: "Towards Efficient Texture Classification and Abnormality Detection", A dissertation submitted to the University of Bristol in accordance with the requirements for the degree of Doctor of Philosophy in the Faculty of Engineering, Department of Computer Science. Bristol, October 2004.
- [19] D. Chetverikov, K. Gede: "Textures and structural defects", *Computer Analysis of Images and Patterns*, Vol. 1296, pp. 167-174, 1997.
- [20] I. Aleksi, Ž. Hocenski, I. Lukić, "CPLD- and FPGA-Based Technology Applications in Embedded Systems Used in Transport and Industrial Control", *26th International Conference Science in Practice (SIP)*, IEEE Croatia Section, Osijek, ISBN: 978-953-6032-62-4, pp. 125-127, 2008.