A Hardware Product Sorter-Absorber Circuit

Pavel Kashubin, Pongthai Sakornsint, Narit Ruangjiratain

EE574FP

Spring 1998

Project Goals

- The goal of the project is to design a product sorter - absorber circuit that will be synthesizable into DEC-Perle architecture.
- Current project is based on last years work that proved this concept.
- The project is currently going through extensive simulation and synthesis targeted for Xilinx 3090 FPGAs.

Design Description

- The project is done using VHDL and schematic capture with the use of OrCAD tool evironment. There are several parts of this project.
- Design a sorter-absorber circuit that can be implemented in a 3090 FPGA.
- Design a pipeline that would allow data to be moved to 4 sorters in parallel
according to constraints of DEC-Perle architecture.

Design Description (cont'd)

- From developed pipeline, produce main controller state machine, memory controller state machine, and sorter shells or configurations. processing pipeline commands.
- Create schematic or VHDL diagram representing FPGA pipeline array.
- Create VHDL models for memory, and test bench incorporating all controllers, memory and FPGA array. Create different input files for processing by testbench.

Design Evolution

- **Project designed last year proved to be inadequate in the following areas:**
  - Design did not take into consideration the configuration of DEC-Perle array and input / output constraints.
  - Skewed pipeline was not realizable as designed.
  - Controllers, switches and memory had to be redesigned for new pipeline.
- **Advantages of current Design.**
- The most important advantage from last years is that the project has been successfully synthesized under OrCAD tools for the given FPGAs.
- The actual sorter-absorber shells use same pin names as the DEC-Perle board and have been simulated as such, in addition to creating a schematic corresponding to actual array.

Technology

- **Applied circuit techniques in this project:**
  - Iterative circuit to compare two data words.
  - *Allows to process two input words spatially instead of synchronously*
  - Two memory controllers that each can operate in master or slave mode.
  - *Allows development of ping-pong data trasfer*
- **New concept**
  - Ping-pong processing of data
  - *Allows to continue processing data in the memory through the pipeline without having to move it.*

Current Status

- **Continuing modifications to project files implementing ping-pong data transfer and reverse sorting.**
- **Implement some overloaded VHDL "+" and "-" functions for std_logic_vector to make controller design easier.**
- **Creating test benches and memory VHDL models that can be used for top-level simulation.**
- **"Webifying" the project including Perl script to create appropriate input files for simulations.**

Project Topics

- Sorting and Absorption Theory
- DEC-Perle Architecture
- Pipeline Function
- Design of Controllers, Switches, and Sorter Shells.
- Iterative Sorter-Absorber Network
- VHDL Code Structure